Journal of Electrical and Computer Engineering Innovations
(JECEI)
Journal homepage: http://www.jecei.sru.ac.ir

Research paper

Performance Analysis of Reversible Sequential Circuits Based on Carbon NanoTube Field Effect Transistors (CNTFETs)

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Article Info

Article History:
Received 22 August 2017
Revised 28 February 2018
Accepted 30 May 2018

Keywords:
Reversible Logic
Sequential Circuit
Carbon Nanotube Field Effect Transistor
Flip-Flop
Power Consumption

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Extended Abstract

Background and Objectives: This study presents the importance of reversible logic in designing of high performance and low power consumption digital circuits. In our research, the various forms of sequential reversible circuits such as D, T, SR and JK flip-flops are investigated based on carbon nanotube field-effect transistors.

Methods: By simultaneous using of the reversible logic gates and carbon nanotube transistors in implementation of various flip-flops and introducing suitable transistor circuits of conventional reversible gates, all reversible flip-flops are simulated in two voltages, 0.3 and 0.5 Volt. The Hspice_H-2013.03-SP2 software is used to simulate these circuits using the 32nm CNTFET technology (the standard Stanford spice model).

Results: The simulation results indicate a significant reduction in the average power consumption of D, T, SR and JK flip-flops, respectively about 99.98%, 82.79%, 60.46%, and 81.53%.

Conclusion: Our results show that the proposed structures have achieved a high performance in terms of average power consumption and PDP.

Introduction

Nowadays, a major problem in the design of large-scale integrated circuits is jointly reduction the power consumption and energy dissipation. In the early 1960s, R. Landauer with the emphasis on the topics of thermodynamics showed that the design of digital circuits using conventional logic known as irreversible logic, causes unwanted loss of electrical energy in the circuit. The reason is that in circuits designed by irreversible logic, the number of circuit inputs is greater than the number of outputs. So, a number of bits containing information are lost during processing and their electrical energy will be released as heat energy. He also proved that the amount of heat generated by the loss of a bit information during processing is measurable by $K.T.\ln 2$, where K is Boltzmann's constant and T is the absolute temperature of the environment (in Kelvin) in which the processing takes place [1]. In 1973, Bennet proved that in order to avoid energy dissipation in digital circuits, the processes should be reversible [2]. On the other hand, given that reducing the scale in CMOS technology is lead to power dissipation, so carbon nanotube field effect transistors are a great option for reducing the size and development of new structures. They have advantages such as transmission ballistic, high mobility, and low power consumption. Therefore, much research has focused on the use of these transistors in the design of the different electronic circuits.

So far, many studies have been done to investigate and introduce reversible gates, in [3] the authors presented a T flip-flop for design of synchronous and non-synchronous digital counters by using the RM reversible gate. Their aim was to optimize the number of reversible gates, delay, quantum cost, and the number

of garbage outputs. As well as, in [4] the authors presented a variety type of reversible flip-flops. Then, they provided a shift register with optimal values of delay, quantum cost and garbage output. In [5], the authors implemented a new T flip-flop design with using of a reversible "SG" gate and a Feynman gate to reduce the power consumption. Then, they presented a reversible non-synchronous counter. In [6], the authors reviewed the commonly reversible gates, they introduced a new reversible gate and designed several examples of D, T, SR, and JK flip-flops by reducing the number of reversible gates, quantum cost and garbage output. In [7], the authors were able to earn better results in terms of quantum cost and the number of garbage outputs by improving the direct feedback method and the use of successive reversible flip-flops. Due to the advantage of using carbon nanotube transistors in design of digital circuits, in [8], the authors used carbon nanotube transistors to implement several circuits such as an inverter gate, 2:1 and 8:1 multiplexers, as well as 1:2 and 1:8 de-multiplexers and compared the results to that of CMOS technology, which show significant improvements in power consumption and delay time. In [9], the authors studied CNTFET and CMOS transistors in 32nm technology for flip-flop circuit design. Then, a new D flip-flop was presented which is used in memory ICs with a carbon nanotube field effect transistor. The results of the simulation showed a CNTFET technology can be a desirable substitute for traditional technology because it has higher speed and lower power dissipation. In [10], the authors presented a design and analysis of CNTFET-based negative edge triggered D flip-flop (DFF) using a pass transistor logic style with single clock phase including reset function. The simulation results show that the proposed DFF-based gray counter and linear feedback shift register (LFSR), as applicative examples of the proposed DFF, have achieved respectively 96% and 97% performance improvement over CMOS designs in terms of power delay product (PDP). In [11], the authors introduced an analysis of low power consumption, positive edge triggered D flip-flop made using CNTFETs and in sleep transistor configuration. The reported circuit has less power dissipation and can be used efficiently with low power circuitry. In [12], the authors reported two CNTFET-based D flip-flop in 32nm CNTFET technology. Flip-flops are simulated with an operating voltage of 1 Volt. The results showed that the second design improves both delay and power consumption 44% and 29%, respectively in comparison with the other CNTFET-based D flip-flop circuits. In [13], the authors presented three different designs of D-latch. The simulation results showed that by using carbon nanotube field effect transistors they have achieved a significant improvement in delay, power and power delay product. The performance of the proposed circuits has been evaluated in different voltages (0.6, 0. 8, 1, 1.2 and 1.6 v). In this paper, we try to show the importance and performance analysis of CNTFET-based reversible logic circuits. For this reason, due to the importance of flip-flops in designing various sequential circuits, we have examined reversible D, T, SR and JK flip-flops. In our study, all structures are simulated with the lowest amount of supply voltage compared to the other works. The simulations confirm the considerable improvement in the proposed structures in terms of the power consumption, delay and PDP. The rest of this paper organized as follows: Section 2 describes a brief description of CNTFETs. Section 3 introduces reversible gates and designs suitable transistor circuits for the implementation of reversible Feynman, Fredkin and Peres gates by using carbon nanotube transistors. In Section 4, we first discuss the flip-flops which are the main elements in the design of the sequential circuits. Then, we introduce the implementation of different types of flip-flops by using reversible gates. At the end, the results are expressed in two parts. In the first part, the performance table of the reversible gates and in the second part, the simulation results of the proposed reversible flip-flops are presented.

The Structure of Transistors Based on Carbon Nanotube

The wonderful electronic properties of transistors based on carbon nanotubes make them the potential candidates for future integrated circuits. The main difference between carbon nanotube field effect transistor (CNTFET) and Si-CMOS is the shape of their channels. In CNTFETs, a single walled carbon nanotube (SWCNT) is used.

The single-walled nanotubes consist of hollow cylinders in which carbon atoms are arranged in a hexagonal network. With the goal of visualization, it is better to say that single-walled nanotubes is a graphene sheet which converted into a tube shape. In Fig. 1, a carbon nanotube field effect transistor is shown with its main parameters. The single-wall nanotube strip structure can also be described using a chiral vector [14]:

$$C = na_1 + ma_2 \quad (1)$$

where n and m are integers that show the chirality of the nanotube, a_1 and a_2 are constant vectors of the graphene network. The values of n and m denote the properties of carbon nanotubes, with semiconducting or metallic properties. So that if $n = m$ or $n - m = 3i$, i is the correct value, the carbon nanotube has a metallic property and if $n - m \neq 3i$, the carbon nanotube has a semiconductor property [14].

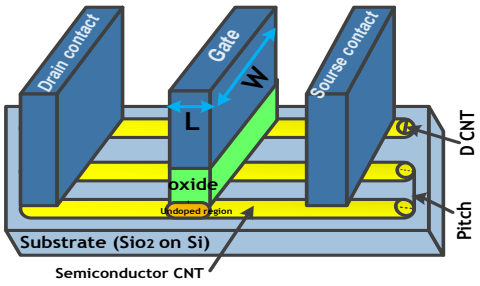


Fig. 1: Carbon nanotubes field effect transistor.

For a single-walled carbon nanotube, the diameter is obtained according to the chiral vector from the following equation [15]:

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + nm + m^2} \quad (2)$$

where $a_0 = 0.142nm$ is an atomic distance between each carbon atom and other adjacent atoms. In semiconducting nanotubes, semiconducting properties of carbon nanotube with its diameter has an inverse relationship, which is the relationship between the two in the following equation [14]:

$$E_g \propto \frac{0.8ev}{d(nm)} \quad (3)$$

E_g Is the energy gap for a carbon nanotube depending on the CNT diameter due to its semi-conductivity. The minimum essential voltage for ON state of a transistor that called threshold voltage, due to the intrinsic nature of the channel and the presence Fermi level in the middle of the barrier, is half the energy gap [14]:

$$V_{th} = \frac{\sqrt{3}a_0}{3e \times d} v_\pi \quad (4)$$

here, v_π is the bond energy of carbon atoms, e is the electric charge of an electron and d is the diameter of carbon nanotube.

Reversible Logic Gates and Circuits

A logical gate is called reversible if and only if there is a peer-to-peer relation between its input and output vectors whereas the number of inputs and outputs is the same [16]. In order to construct a reversible circuit, reversible gates (RGs) should be used. The design of an optimal reversible circuit should be done with the goal of reducing the number of constant inputs, the number of garbage outputs, the number of reversible gates and the quantum cost of this gate. Inputs that are added to a function for constructing it as a reversible gate are called constant inputs (CIs) and the outputs that will not be used in any other computational operation within the circuit are called garbage outputs (GOs). The number of reversible gates that used in a reversible circuit is called the number of gates, these gates are assigned to obtain the expected results in the proposed designs. One of the criteria for evaluation reversible circuits is quantum cost (QC). The basic reversible gates with 1×1 and 2×2 sizes have a quantum value of zero and one, respectively. These basic gates are defined in the design of a reversible gate as the quantum cost. The delay of a reversible gate is defined as the maximum number of reversible gates that are located on the input to output path [17]. In recent years, various 1×1, 2×2 and 3×3 reversible gates have been presented. 1×1 and 2×2 reversible logic gates are the foundations of quantum circuits, the V gate is the square of a NOT gate and V^+ is the conjugate of a V gate, the V and V^+ gates have the two inputs and two outputs. The two V gates in series mode are equivalent to the buffer gate. As well as, the V^+ gates in series mode are equivalent to a NOT gate [18]. So far, many reversible gates are introduced to design low-power logic circuits. In the following, several examples of the known logical reversible gates have been investigated and reported.

A. Reversible Feynman Gate

The Feynman gate is a two-input and two-output (i.e., 2×2) reversible gate, which called the FG gate and is known as an uncontrolled gate. The inputs and outputs of this gate are (A, B) and (A, A⊕B), respectively [12]. The block diagram of the Feynman gate and its quantum structure are shown in Fig. 2. Table 1 shows the truth table of this gate and Fig. 3 shows the transistor circuit of the mentioned gate using the CNTFET transistors. In this structure, by applying different type of transistors such as PCNTFET and NCNTFET, if the inputs are A and B, then the outputs will be generated in accordance with P and Q. A similar example is provided for implementation of this gate using MOSFET transistors in reference [19]. The input and output signals related to the implementation of the reversible Feynman gate using the CNTFET transistors are also depicted in Fig. 4.

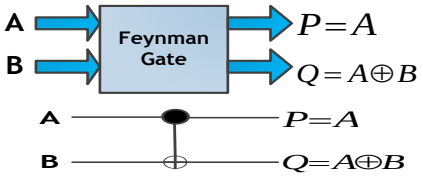


Fig. 2: The block diagram and the quantum dot display of the reversible Feynman gate.

Table 1: The truth table of the reversible feynman gate [20]

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

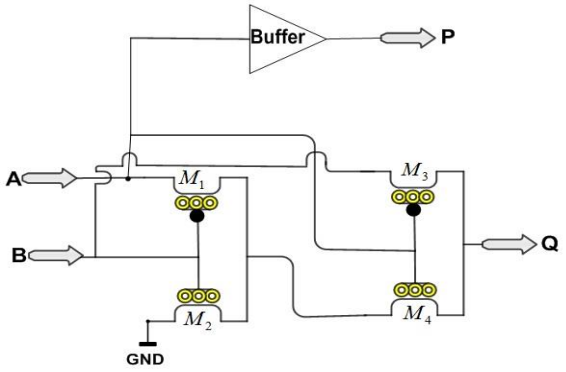


Fig. 3: Realization of transistor structure for reversible Feynman gate.

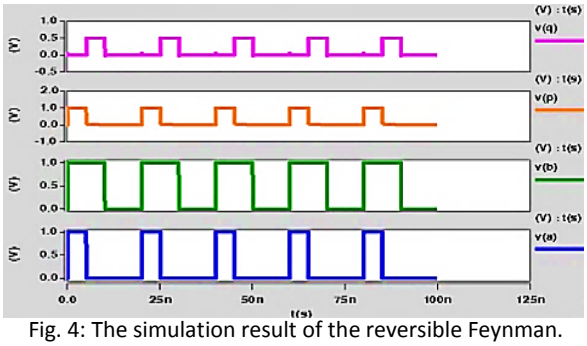


Fig. 4: The simulation result of the reversible Feynman.

B. *Reversible Fredkin Gate*

The Reversible Fredkin gate is one of the important gates that it has three inputs and three outputs (3×3). This gate has been attracting a lot of attention. Fredkin gate is a controlled gate by the control input A and is used for the displacement of two values [17], the block diagram and the quantum dot structure are illustrated in Fig. 5 and the truth table of this gate is shown in Table 2.

For implementation the transistor level of this gate, the circuit based on CNTFET transistors is proposed which shown in Fig. 6. This circuit is similar to the transistor circuit of the Feynman gate to generate the outputs. In references [19, 21], the implementation of the reversible Fredkin gate is shown using 6 and 8 transistors, respectively.

In Fig. 7, the simulation result of the implementation of this gate using CNTFET transistors is provided.

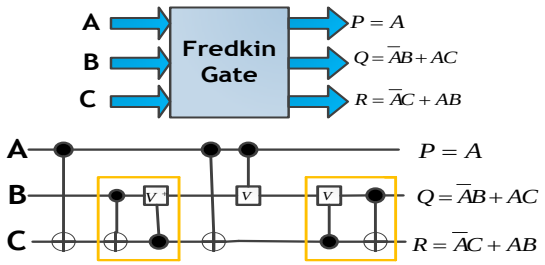


Fig. 5: Block diagram and quantum dot display of the reversible Fredkin gate.

Table 2: The truth table of the reversible fredkin gate [20]

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

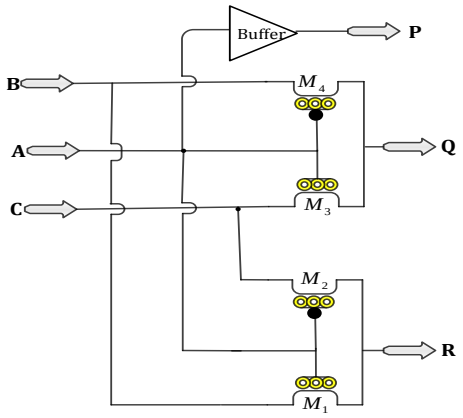


Fig. 6: Realization of transistor structure for reversible Fredkin gate.

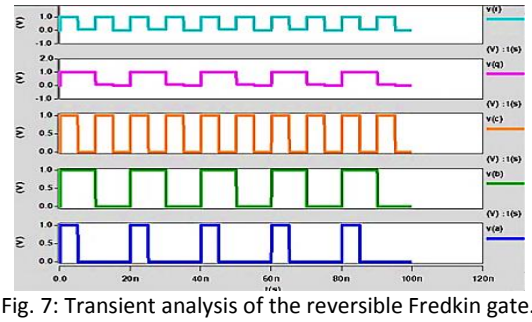


Fig. 7: Transient analysis of the reversible Fredkin gate.

C. *Reversible Peres Gate*

The Peres gate (PG) is a reversible gate by three inputs and three outputs (3×3). In this structure, if the third input is zero, the third output is the logical AND of the first two inputs [17]. The block diagram and the quantum dot structure of this gate are shown in Fig. 8. The truth table and the proposed transistor circuit for this gate using CNTFETs are respectively shown in Table 3 and Fig. 9. In the reference [17], implementation of this gate is provided using MOSFET transistors. The output waveforms of this gate are shown in Fig. 10.

Finally, a summary of the main reversible gate features of Feynman, Fredkin, and Peres, is given in Table 4.

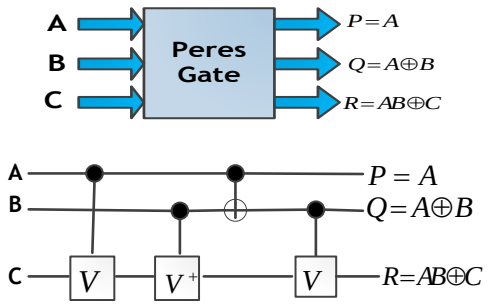


Fig. 8: The block diagram and the quantum dot representation of the reversible Peres gate.

Table 3: The truth table of the reversible peres gate [20]

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Table 4: Comparison of the reversible feynman, fredkin, and peres gates

Reversible Gate	Size	Quantum Cost
Feynman	2×2	1
Fredkin	3×3	5
Peres	3×3	4

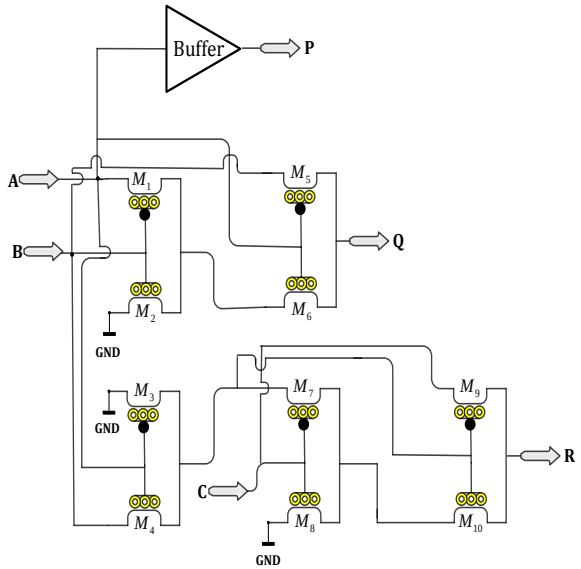


Fig. 9: Realization of transistor structure for reversible Peres gate.

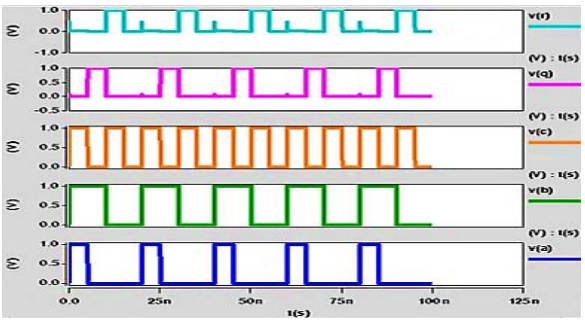


Fig. 10: Transient analysis of the reversible Peres gate.

Sequential Circuits Based on Reversible Logic Gates

The sequential circuit takes samples at certain moments of the output and transmits it to the other parts of the circuit. Therefore, modern computer processing will not be possible without the addition of sequential circuits. The main characteristic of the sequential circuits is that the logic systems have memory and the output of the sequential circuits is generated after a certain delay. Flip-flops are the principal blocks of digital sequential circuits and they have many uses in computers and design of communication circuits. Flip-flops are used to design memory cells that can store a bit of information. In general, these circuits are divided into four main categories of D, T, SR, and JK flip-flops. In the following, we introduce these circuits and show how they are implemented in reversible logic using carbon nanotube transistors.

A. Reversible D –Flip-Flop

This flip-flop has an input D and a clock signal. D-flip-flop is used as a stable cell, because its data input is imported into flip-flop memory after each pulse and is kept until the next clock pulse [22]. In the D-flip-flop, if the clock is on right edge, the same value of the input D will be generated in the output. In Fig. 11, two different structures for D-flip-flop have been proposed using reversible Feynman and Fredkin gates implemented by carbon nanotube field effect transistors. The truth table for this flip-flop is given in Table 5. The comparisons of the reversible D-flip-flops are reported in Table 6.

Table 5: D-Flip-Flop performance [16]

Clk	D	Q
low	X	No Change
High	0	0
High	1	1

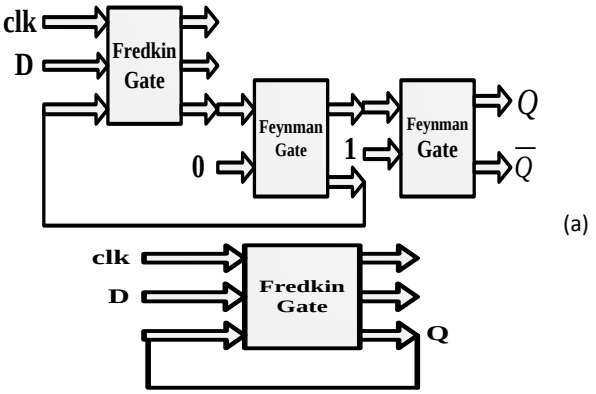
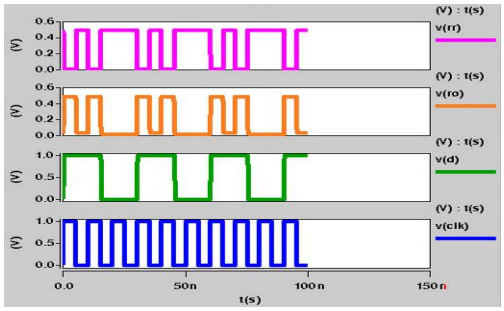


Fig. 11: a) The first proposed reversible D-flip-flop (D FF_1) [11], b) The second proposed D-flip-flop (D FF_2) [18].

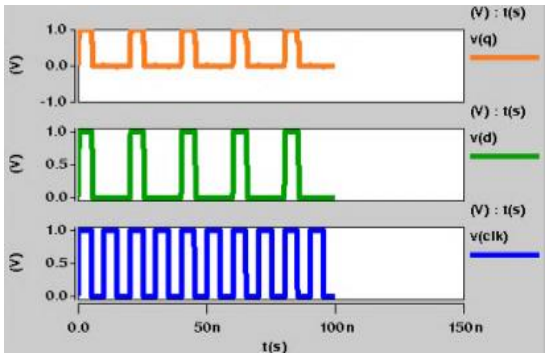
B. Reversible T-Flip-Flop

This flip-flop has one input that called T and another input will be used for the clock. In this flip-flop, if T = 1, it causes a change in output, that is if the output is zero, its value is 1, and vice versa if its output is one, its value is zero [24]. The truth table for this flip-flop is presented in Table 7. As shown in Fig. 13, the T flip-flop can be created using reversible Peres and Feynman gates [25]. In this paper, the structure described in Fig. 14 is used for implementing T flip-flop using reversible gates and carbon nanotube transistors with the goal of significantly reducing the amount of power consumption.

Comparison of the main parameters of this flip-flop with the previous works is presented in Table 8.



(a)



(b)

Fig. 12: Transient analysis of the reversible D-flip-flop, a) D FF_1, b) D FF_2.

Table 6: Comparison of suggested D–Flip-Flop with previous works

D-Flip-Flop	No. of RGs	Quantum Cost	No. of CI	No. of GO	Delay
Ref. [6]	3	12	4	3	3
Ref. [4]	6	22	6	10	6
D FF_1	3	7	2	2	3
D FF_2	1	5	2	2	1
Improvement (%) (D FF_1 compared to Ref. [6])	-	41.66	50	33.3	-
Improvement (%) (D FF_1 compared to Ref. [4])	50	68.18	66.6	80	50
Improvement (%) (D FF_2 compared to Ref. [6])	66.6	58.3	50	33.3	66.6
Improvement (%) (D FF_2 compared to Ref. [4])	83.3	77.27	66.6	80	83.3

Table 7: T -Flip-Flop performance [26]

T	Q_{t+1}
0	Q_t
1	$\overline{Q_t}$

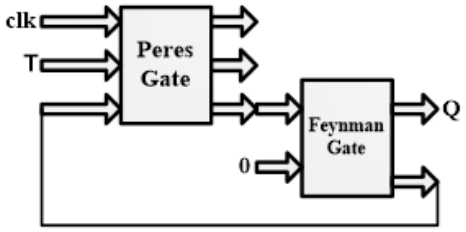


Fig. 13: The proposed reversible T-flip-flop.

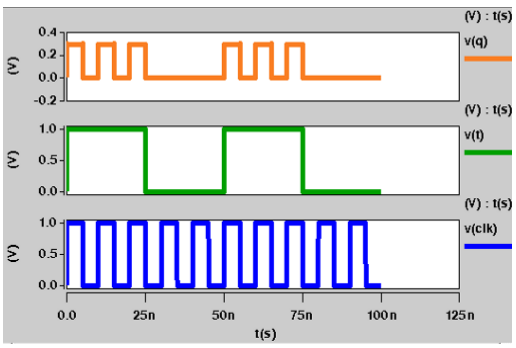


Fig. 14: Transient analysis of the reversible T-flip-flop.

Table 8: Comparison of suggested T–Flip-Flop with previous works

T Flip-Flop	No. of RGs	Quantum Cost	No. of CI	No. of GO	Delay
Ref. [25]	3	19	3	5	3
Ref. [3]	1	-	3	2	1
Proposed T-FF	2	5	1	1	2
Improvement (%) (T-FF compared to Ref. [25])	33.3	73.68	66.6	80	33.3
Improvement (%) (T-FF compared to Ref. [3])	-	-	66.6	50	-

C. Reversible SR -Flip-Flop

The SR flip-flop has two inputs named S and R, and two outputs that are complementary of each other.

According to the Table 9, the performance of this flip-flop is such that when we examine the circuit operation, if S = 1 and R = 0, it is saying that the circuit is set. That is, its output is 1. If S = 0, then the circuit remains in the set mode. But, if R = 1, it is saying that they are reset, the output at this moment is zero, and if at this moment R = 0, the circuit remains in the reset mode. Therefore, R = 0 and S = 0 in the output indicate which of the S or R last time was equal to 1. Also, if R and S are simultaneously in state 1, the circuit will be uncertain. So that in the designed flip-flop, the inputs S and R are not synchronized at the same time, this is a limitation for the SR flip-flop. Fig. 14 shows the proposed circuit for implementing SR flip-flop using the reversible gate. In this circuit, two reversible Peres gates are used for implementing SR flip-flop [25]. The result of CNFET-based flip-flop is shown in Fig. 15. In addition, Table 10 depicts the comparison between the suggested flip-flop and other similar works. It is clear that the proposed flip-flop is more optimal.

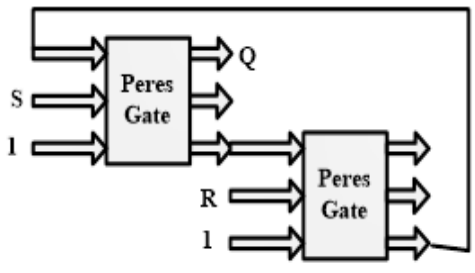


Fig. 15: The proposed reversible SR-Flip-Flop

Table 9: SR-Flip-Flop performance [16]

S	R	Q(t+1)
0	0	Q(t) No Change
0	1	0
1	0	1
1	1	No Prediction

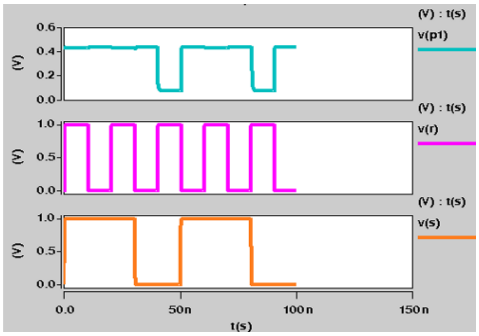


Fig. 16: Transient analysis of the reversible SR- Flip-Flop.

Table 10: Comparison of suggested SR–Flip-Flop with previous works

SR Flip-Flop	No. of RGs	Quantum Cost	No. of CI	No. of GO	Delay
Ref. [4]	6	22	6	8	6
Ref. [6]	3	-	5	3	3
Proposed T-FF	2	7	4	2	2
Improvement (%) (SR-FF compared to Ref. [4])	66.6	68.18	33.3	75	66.6
Improvement (%) (T-FF compared to Ref. [6])	33.3	-	20	33.3	33.3

D. JK -Flip-Flop

This flip-flop has two inputs, called J and K, and two outputs which are complementary to each other. In JK flip-flop, the limitations associated with the SR flip-flop are resolved and two inputs J = 1 and K = 1 are acceptable for this circuit. In this flip-flop, like the SR type, all-zero inputs (J = 0 and k = 0) have no effect on the flip-flop output state and they remain in the previous state, but if J = 1 and K = 1, the state in the output will be changed [27]. In this paper, a structure of CNFET-based JK flip-flop by using reversible Feynman and Fredkin gates (as shown in Fig. 16) is proposed [25]. Fig. 17 shows the simulation results and the truth table for the JK flip-flop is shown in Table 11. Comparison of the proposed flip-flop to the previous work [6], in terms of the number of reversible gates, quantum cost,

constant inputs, the number of garbage outputs and latency are presented in Table 12.

Table 11: JK -Flip-Flop performance [16]

J	K	Q_{t+1}
0	0	Q (t) No Change
0	1	0
1	0	1
1	1	$\overline{Q_t}$

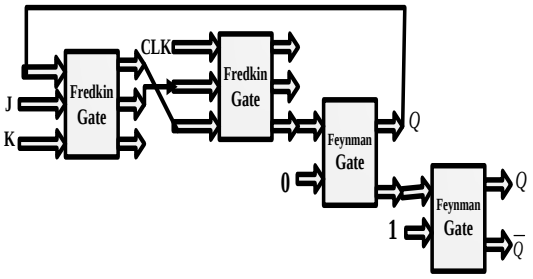


Fig. 17: The proposed reversible JK-Flip-Flop.

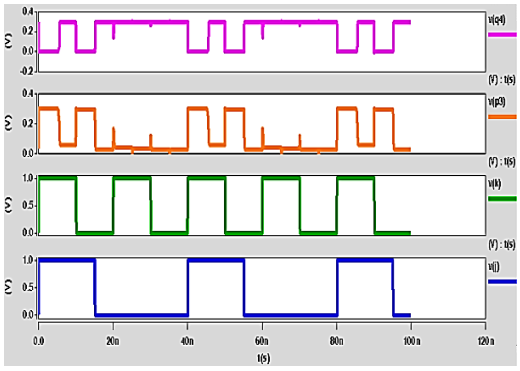


Fig. 18: Transient analysis of the reversible JK-Flip-Flop.

Table 12: Comparison of suggested JK–Flip-Flop with previous works

JK Flip-Flop	No. of RGs	Quantum Cost	No. of CI	No. of GO	Delay
Ref. [6]	5	25	3	4	5
Proposed JK-FF	4	12	3	3	4
Improvement (%) (T-FF compared to Ref. [6])	20	52	-	25	20

Simulation Results

A. Analysis of the operation of the reversible Feynman, Fredkin and Peres gates

In this section, we evaluate the performance of the CNFET-based reversible Feynman, Fredkin and Peres gates. Adjustable parameters of the carbon nanotube transistors which can be used in each of the reversible gates are presented in Table 14. Also, the main design criteria of the digital circuits are reported in Table 13. The results indicate that the values of the supply voltage, the number of transistors, power consumption, delay, PDP and EDP in these gates are desirable. Moreover, the simulation result represent a decrease of 90% in the supply voltage for implementation of reversible Feynman and Fredkin gates by using carbon nanotube transistors compared to that for the reference [27].

Furthermore, the number of transistors in the reversible Feynman gate is decreased about 25% compared to that for the reference [27]. In addition, the power consumption at simulation time from zero to 100 ns for the Feynman and Fredkin gates as compared to Reference [27] has been reduced 99.33% and 98.41%, respectively.

Table 13: Performance evaluation of known reversible gates

Parameter	Feynman Gate	Fredkin Gate	Peres Gate
Technology	CNTFET	CNTFET	CNTFET
Supply Voltage (V)	0.5	0.5	0.5
Number of Transistors	6	4	12
Average Power Consumption (W)	7.964e-08	1.490e-08	7.827e-07
Maximum Power Consumption (W)	1.918e-05	1.416e-06	3.176e-05
Delay(Sec)	2.531e-09	5.045e-09	2.525e-09
PDP (J)	2.016e-16	9.787e-17	1.976e-15
Energy Delay Product (EDP) (J×Sec)	5.102e-25	4.937e-27	4.289e-24

B. Performance analysis of the D, T, SR and JK Flip-Flops

In this section, all flip-flops that have introduced in the previous sections have been compared with the other similar works in terms of supply voltage, the number of transistors, average power consumption, and the type of technology which is required for implementing the proposed structure and design type. The simulation results are presented in Table 15. The results indicate a significant decrease in the amount of the average power consumption. It is clear that for simulation time from zero to 100 ns, average power consumption in the first proposed reversible D flip-flop (DFF_1) and the second reversible D flip-flop (DFF_2) are respectively reduced 99.65% and 99.99% compared to the structures presented in [28] and [28-31]. The improvement for reversible T flip-flop and SR flip-flop compared to references [32] and [34] are 82.79% and 60.46%, respectively. Also, average power consumption for reversible JK flip-flop is reduced 81.53% compared to reference [27].

Table 14: Values of adjustable CNTFET parameters for all proposed reversible structures

Parameter	Feynman gate	Fredkin gate	Peres gate	D FF_1	D FF_2	T-FF	SR-FF	JK-FF
V_{dd} (V)	0.5	0.5	0.5	0.5	0.3	0.3	0.5	0.3
N	3	3	3	1	3	3	1	3
L_g (nm)	32	32	32	32	32	32	32	32
L_{ss} (nm)	32	32	32	32	32	32	32	32
L_{dd} (nm)	32	32	32	32	32	32	32	32
T_{ox} (nm)	4	4	4	4	4	4	4	4
K_{ox}	16	4	16	4	4	16	3	4
Pitch (nm)	20	20	20	-	20	20	-	20
Chiral vector	(34,0)	(43,0)	(43,0)	(173,0)	(173,0)	(53,0)	(73,0)	(73,0)

Table 15: Comparisons of various Flip-Flops circuits

Parameter	Technology	Supply Voltage(V)	Number of Transistors	Average Power Consumption (W)	PDP(j)	Design Type
D-FF [28] Pass Transistor Logic Flip Flop	180 nm CMOS	1.8	18	42.23e-06	1.130e-15	Classic
D-FF [29] Hybrid Latch Flip Flop	45 nm CMOS	1.8	20	5.469e-06	2.83e-15	Classic
D-FF [30]	90 nm CMOS	1	17	15.95e-06	1.58e-12	Classic
D-FF [31]	180 nm CMOS	1.8	16	2.60e-06	4.342e-17	Classic
D FF_1	CNTFET	0.5	16	1.445e-07	3.754e-16	Reversible
D FF_2	CNTFET	0.3	4	1.305e-10	3.711e-19	Reversible
T-FF [32] Design 1	Si-MOSFET	0.9	22	17.5e-06	0.878e-15	Classic
T-FF [32] Design 2	CNTFET	0.9	16	38.00e-06	0.501e-15	Classic
T-FF [27]	0.35 um CMOS	1	24	2.9826e-004	-	Reversible
Proposed T-FF	CNTFET	0.3	18	6.538e-06	1.659e-14	Reversible
SR-FF [33]	90 nm CMOS	1	28	16.976e-06	-	Classic
SR-FF [34] Clocked CMOS Flip-Flop	45 nm CMOS	1.2	12	7.512e-06	-	Classic
Proposed SR-FF	CNTFET	0.5	24	2.970e-06	1.498e-14	Reversible
JK-FF [27] Standard CMOS	45 nm CMOS	0.9	32	2.510e-05	5.02e-12	Classic
JK-FF [27] Standard transmission-gate	45 nm CMOS	0.9	40	1.343e-05	5.37e-12	Classic
JK-FF [27] Modify gate	45 nm CMOS	0.9	16	1.119e-05	2.71e-14	Classic
Proposed JK-FF	CNTFET	0.5	14	4.635e-06	1.268e-14	Reversible

Conclusion

Reducing the energy consumption of electronic chips has been one of the most important concepts in recent years.

Therefore, in this paper with the goal of achieving an optimal circuit, the use of reversible logic gate has been suggested which is a desirable solution to reach an optimal power consumption in quantum computing and Nano technology.

It is due to this fact that the reversible logic naturally prevents energy loss. On the other hand, due to that the flip-flops are the mainstay part of the original digital circuit, this paper presents the reversible Feynman, Fredkin and Peres gates based on carbon nanotube field effect transistors for the provided D, T, SR and JK flip-flops.

In the proposed circuits, we tried to optimize the number of reversible gates, quantum cost, the number of constant inputs, the number of garbage outputs, delay, and the number of transistors. Moreover, the minimum occupied area can be achieved. In addition, the simulation results showed a significant reduction in the power consumption of D, T, SR and JK flip-flops, respectively about 99.98%, 82.79%, 60.46%, and 81.53%. As the results show, the simultaneous use of the reversible logic gates and carbon nanotube transistors in implementation of the proposed flip-flops could reduce the amount of power consumption.

Author Contributions

M. Shaveisi and A. Rezaei introduced the simulations. M. Shaveisi simulated the structures. A. Rezaei performed the results analysis. M. Shaveisi and A. Rezaei verified the results and prepared the manuscript.

Acknowledgment

The authors would like to thank the reviewers for their comments that help improve the manuscript.

Conflict of Interest

The authors express that there is no conflict of interests about the publication of this manuscript. So, the ethical issues such as plagiarism, accuracy of results and double publication have been completely observed by the authors.

Abbreviations

CNTFET	Carbon Nanotube Field Effect Transistor
LFSR	Linear Feedback Shift Register
PDP	Power Delay Product
CI	Constant Input
GO	Garbage Output
QC	Quantum Cost

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How to cite this paper:
M. Shaveisi, A. Rezaei, "Performance Analysis of Reversible Sequential Circuits Based on Carbon Nanotube Field Effect Transistors (CNTFETs)," Journal of Electrical and Computer Engineering Innovations, 6(2): 173-183, 2018.
DOI: 10.22061/JECEI.2019.5015.183
URL: http://jecei.sru.ac.ir/article_1099.html