Research paper

Improvement of Tunnel Field Effect Transistor Performance Using Auxiliary Gate and Retrograde Doping in the Channel

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Article Info

Abstract

Background and Objectives: In this work, a dual workfunction gate-source pocket-retrograde doping-tunnel field effect transistor (DWG SP RD-TFET) is proposed and investigated.

Methods: The dual workfunction gate-source pocket-retrograde doping-tunnel field effect transistor is a Silicon-channel TFET with two isolated metal gates (main gate and auxiliary gate) and a source pocket in the channel close to the source-channel junction to increase the carrier tunneling rate.

Results: For further enhancement in the tunneling rate, source doping near the source-channel junction, i.e., underneath the auxiliary gate is heavily doped to create more band bending in energy band diagram. Retrograde doping in the channel along with auxiliary gate over the source region also improve device subthreshold swing and leakage current. Based on our simulation results, excellent electrical characteristics with ION/IOFF ratio > 109, point subthreshold swing (SS) of 6 mV/dec and high gm/ID ratio at room temperature shows that this tunneling FET can be a promising device for low power applications

Conclusion: In order to increase the ON-current in this device, we utilized several methods including incorporation of high-K material in top oxide, source pocket in channel and a thin auxiliary gate with high workfunction over the source region. Incorporating auxiliary gate over the source also caused a barrier formation in the energy band diagram profile of this device which it leds electron concentration in the channel, subthreshold swing and OFF-current to be reduced.

Introduction

Recently, low power consumption is one of the most important requirements in both digital and analogue circuits [1], [2] and it has become more serious by scaling-down in semiconductor industry. Scaling supply voltage (VDD) down plays an important role in reducing both standby and dynamic power consumptions [3], [4]. For conventional complementary metal-oxide semiconductor (CMOS) devices, VDD scaling is slowing down due to non-scalability of built-in potential and because down scaling of threshold voltage (Vth) leads to increase of OFF-current (I_{OFF}) [5], [6]. In fact, OFF-current increase originates from subthreshold swing limitation of 60 mV/dec in MOSFETs, due to Boltzmann distribution of carriers at room temperature [4], [7], [8]. In order to overcome above-mentioned restrictions, different structures and materials including multi-gate transistors and high-k materials have proposed yet [9]-[16].

In the meantime, Tunnel FET can operate at lower voltage [17]-[20], and it has excellent subthreshold characteristic compared to MOSFET [21], [22]. Unlike MOSFETs in which injection mechanism is because of thermal injection and drift-diffusion, injection mechanism in TFET is based on interband to band tunneling (BTBT) [22]-[24]. TFET transistor has the ability of lower subthreshold swing, lower off-current and they are less influenced by short channel effects than MOSFETs and CMOS process compatible [25]-[27]. Among these advantages, TFET device has its drawbacks too. It suffers from lack of ON-current compared to MOSFET and it has ambipolar current for negative gate voltages [28]-[30]. However, to increase drive-current, various interesting structures have been suggested to satisfy ITRS requests which are mostly based on doping and work function engineering in the channel and gate [31]. These ideas include utilizing strain silicon in the transistor active region [32], or using P-N-P-N doping profile with just source pocket [12], [24], [33]. Other suggestions include using heterogeneous gate oxide with different metal gate or other structures like dual gate or more than two gates [7], [25]. In our study, we use doping engineering by incorporating both pocket in source-channel junction and retrograde doping in the channel to enhance ON-current and reduce OFF-current, respectively. For further enhancement in ON-current, while reducing OFF-current, we utilize a thin isolated auxiliary gate with higher metal workfunction compared to main gate over the source region near the channel. The higher metal workfunction in the auxiliary gate causes a barrier in bandgap of device profile which it leads to reduction in OFF-current at subthreshold voltages and enhancement in ON-current at higher gate voltages. In addition, we use high-k (HfO$_2$) gate dielectric material to uplift the ON current much more. In the following we comparatively study the electrical characteristics of three devices of source pocket tunnel field-effect transistor (SP TFET), dual workfunction gate source pocket tunnel field effect transistor (DWG SP TFET) and dual workfunction gate source pocket retrograde doping tunnel field effect transistor (DWG SP RD TFET) to prove better electrical performance of our proposed device. The remaining parts of this work are divided into three sections. In the Section two we present a schematic cross section view of SP TFET, DWG SP TFET, and DWG SP RD TFET with related parameters. In Section three, the simulated and extracted results are illustrated. In the last section, we explain comprehensive conclusion for the presented study.

Device Design and Parameters

The main approach of this work is enhancing ON-current and reducing OFF-current to achieve high I$_{ON}$/I$_{OFF}$ ratio. In heterogeneous metal gates, the metal gate with

higher workfunction uplift energy bandgap profile [4]. Regarding to this, we incorporate an auxiliary gate with higher metal workfunction to exist a knee joint profile in the minimum of conduction band (E_c) and maximum of valance bond (E_v). This profile will exist barrier in the conduction band and expand band to band tunneling height in valance band in which, E_c and E_v stand more face to face in diagram band. The existed barrier limits minority carriers (electrons) in the source to enter into the channel and this reduces leakage current and subthreshold swing. Expansion in band to band tunneling height causes more ON-current. In order to enhance ON-current furthermore, we utilize High-k material in gate dielectric (for higher gate electrostatic control over the channel [12]), source pocket in the channel and heavily doping near the source-channel junction in the source region (for more band bending in bandgap profile). We also utilize retrograde doping in the channel to reduce OFF-current and subthreshold swing furthermore. Fig. 1 (a-c) illustrates the schematic view of SP TFET, DWG SP TFET, and DWG SP RD TFET, respectively. All geometrical and process parameters related to three structures are presented in Table 1. To simulate the different electrical characteristics of above-mentioned devices, 2-D ATLAS device simulator from SILVACO, Inc. was used. Atlas simulator can predict the electrical characteristics of semiconductor devices associated with specified bias conditions and based on comprehensive sets of physical models including drift-diffusion and quantum models embedded in it. In order to have reliable results, we used FermiDirac distribution function model. SRH and Auger models were used to consider generation/recombination like [23], [34] did. BBT.NONLOCAL model has been applied to consider nonlocal band-to-band tunneling (BTBT) in the lateral direction [8], [35], since it incorporates carriers transfer from one energy band into another in the source-channel junction in this work. BGN model accounted for applying doping dependence of band gap in simulations [35]. In order to have more reliable results, the simulator is calibrated against two simulation results, reference [6] which device simulations were performed using ISE-TCADs DESSIS device simulator (ver.10.0.4) and FLOOPS process simulator, and [12] which device simulations were performed using 2-D ATLAS, as shown in Fig. 2.

It should be noted that in this work we have ignored tunneling through gate oxide as in recent works [23], [33], [36], and our main aim is to enhance ON-current and reduce OFF-current by utilizing a new doping profile (P$^+$-P^{++}-N^{++}-N-N$^+$) and auxiliary gate.

Results and Discussion

Fig. 3 shows transfer characteristics of SP TFET, DWG SP TFET and DWG SP RD TFET at bias V$_{DS}$=1.0 V. It is observed at nonlinear subthreshold region that DWG SP

RD TFET has the lowest OFF-current and point subthreshold swing (I_{OFF}=4 fA and SS=5 mV/dec) compared to SP TFET (I_{OFF}=2 nA and SS=42 mV/dec) and DWG SP TFET (I_{OFF}=0.8 nA and SS=42 mV/dec) at V_{GS}=0 V. The very low OFF current in the DWG SP RD TFET improves its I_{ON}/I_{OFF} ratio compared to other counterparts which is a figure of merit for this device. We can explain this improvement for DWG SP RD TFET with energy band diagram and electron concentration profiles. Fig. 4 shows conduction band and valance band energy profile of three devices at V_{GS}=0 V and V_{DS}=1.0 V. According to this figure, both DWG SP TFET and DWG SP RD TFET devices have a knee joint profile in their conduction band (E_c) near the source-channel junction position.

Table 1: parameters for SP TFET, DWG SP TFET and DWG SP RD TFET structures

Parameter	Values		
	SP TFET	DWG SP TFET	DWG SP RD TFET
Top oxide thickness (Tox)	0.5 nm	0.5 nm	0.5 nm
Silicon channel thickness	10 nm	10 nm	10 nm
Buried oxide thickness (BOX)	60 nm	60 nm	60 nm
Retrograde doping thickness	-	-	6 nm
Channel length	30 nm	30 nm	30 nm
Auxiliary gate length	-	2 nm	2 nm
Retrograde Doping Length	-	-	4 nm
Main gate and auxiliary gate space gap	-	1 nm	1 nm
Main gate workfunction	4.2 eV	4.2 eV	4.2 eV
Auxiliary gate workfunction	-	5.3 eV	5.3 eV
Pocket doping (N^{++})	9×10^{19} cm^{-3}	9×10^{19} cm^{-3}	9×10^{19} cm^{-3}
Channel doping (N)	3e18 cm^{-3}	3×10^{18} cm^{-3}	3×10^{18} cm^{-3}
Source doping (P^{+})/(P^{++})	5×10^{18} /9×10^{19} cm^{-3}	5e18/9×10^{19} cm^{-3}	5×10^{18} /9×10^{19} cm^{-3}
Drain doping (N^{+})	8×10^{18} cm^{-3}	8×10^{18} cm^{-3}	8×10^{18} cm^{-3}
Net retrograde doping (P)	-	-	1.1×10^{19} cm^{-3}

This knee joint profile formation (which is the result of incorporating high workfunction metal in the auxiliary gate,) behaves like a barrier against source minority carriers (electrons) and limits their entrance to the channel due to thermal emission and this leads OFF-

current to reduce in these devices. Fig. 5 which shows electron concentration profile along three devices at V_{DS}=1.0 V, V_{GS}=0 V, confirms our claim. According to this figure, SP TFET (/DWG SP RD TFET) has highest (/lowest) electron concentration in the channel. So we can expect that SP TFET (/DWG SP RD TFET) has highest (/lowest) OFF-current. The lower OFF-current (/electron concentration) in the DWG SP RD TFET compared to DWG SP TFET, is due to retrograde doping in the channel of this device. Indeed, retrograde doping underneath the channel, scatters electrons which tend to pass from depth of the channel, where gate electrostatic control over the channel is lower compared to the surface.
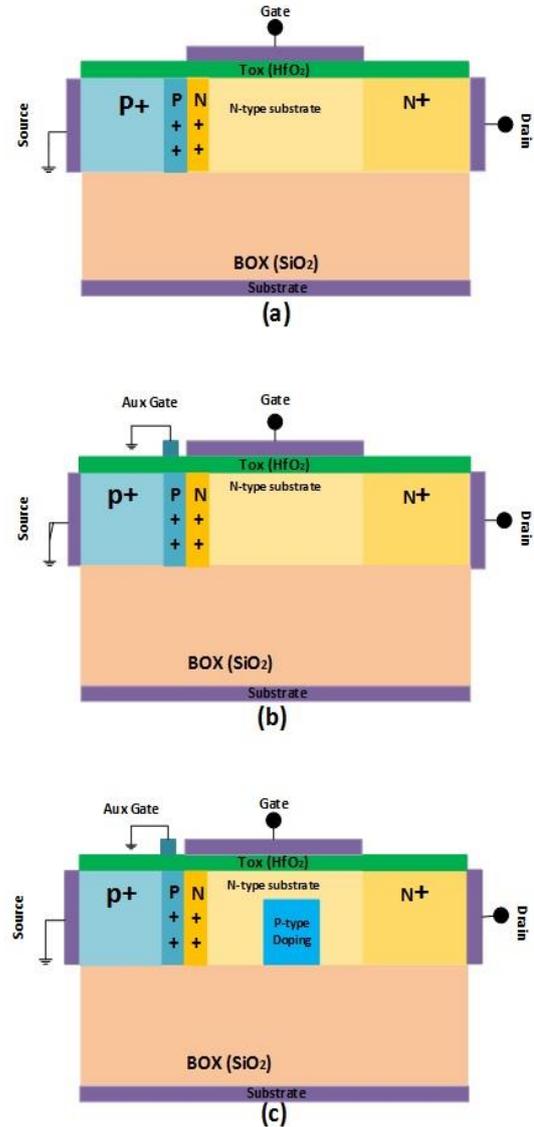
Fig. 1: Cross section view of (a) SP TFET, (b) DWG SP TFET, and (c) DWG SP RD TFET structures.

So, incorporating this doping profile firstly reduces electron mobility in the depth of channel, secondly reduces channel thickness virtually. Therefore, we

expect DWG SP RD TFET has lower OFF-current and subthreshold swing as they are reduced by channel thickness reduction [18]. The lower electron concentration in DWG SP RD TFET due to retrograde doping can also be explained by energy band diagram concept.
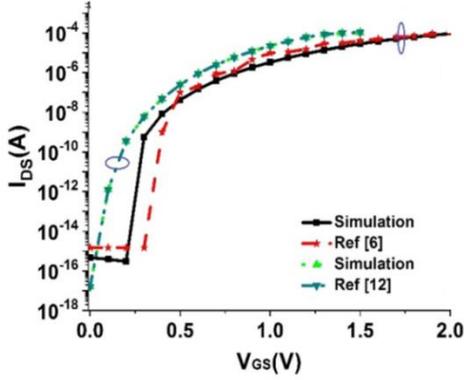
Fig. 2: Calibration of ATLAS simulation results against simulation results of [6] and [12] at V_{DS}=1.0 V.

Fermi-Dirac distribution function which gives the probability that an electronic state at energy E is occupied by an electron, is defined by:

$$f_D(E) = \frac{1}{1 + e^{(E-E_f)/KT}} \qquad (1)$$

where K is Boltzmann's constant, T is absolute temperature (in Kelvin) and E_f is the Fermi level [37].

In fact, p-type retrograde doping can cause the Fermi level distance from valance band to be reduced, and this increases the conduction band energy level distance from the Fermi level.

So, based on Fermi distribution function, this limits electronic state occupation probability in the conduction band of this device and thus electron concentration will be reduced.

It is also observed from Fig. 3 that at higher gate voltages (>1.0 V), ON-current of DWG SP TFET and DWG SP RD TFET become higher than SP TFET. This is due to DWG SP TFET and DWG SP RD TFET have an auxiliary gate with higher metal workfunction. According to the Fig. 6, embedding auxiliary gate in these devices causes firstly, E_c and E_v energy bands slope (i.e. electric field) increase, secondly, E_c and E_v energy bands stands more face to face.

The former sentence means higher electric field in the junction and the later sentence means lower tunneling width in higher energy height. So, tunneling chance in these devices are higher and it is expected they have more ON-current compared with SP TFET.

In fact, ON-current in DWG SP RD TFET is a little lower than DWG SP TFET, because retrograde doping in its channel reduces electron mobility (as a result of impurity scattering) and this leads ON-current to decrease.
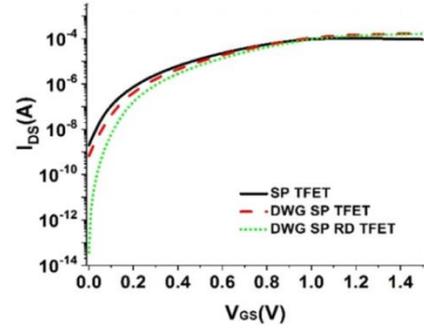
Fig. 3: Transfer characteristics of SP TFET, DWG SP TFET, and DWG SP RD TFET at V_{DS}=1.0 V.
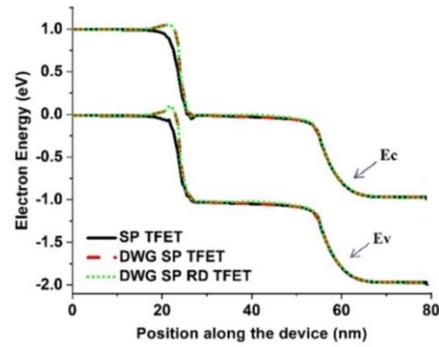
Fig. 4: Energy band diagram profiles of SP TFET, DWG SP TFET, and DWG SP RD TFET at V_{GS}=0 V and V_{DS}=1.0 V.
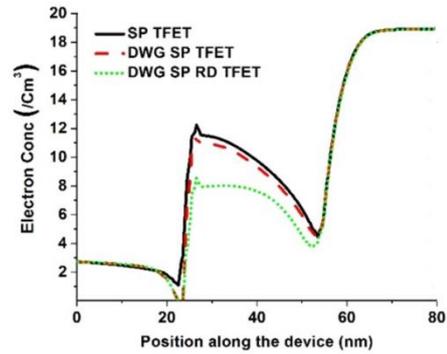
Fig. 5: Electron concentration profile of SP TFET, DWG SP TFET, and DWG SP RD TFET at V_{DS}=1.0 V, V_{GS}=0 V.
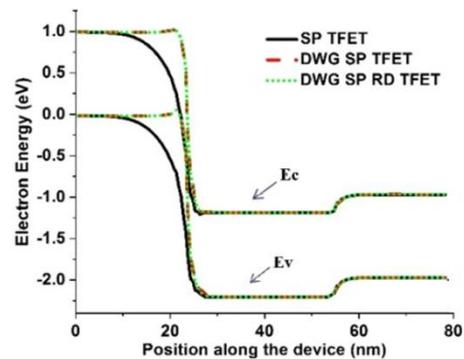
Fig. 6: Energy band diagram profiles of SP TFET, DWG SP TFET, and DWG SP RD TFET at V_{GS}=1.5 V and V_{DS}=1.0.

Transconductance g_m is a figure of merit in both analogue and digital devices and is defined by the following relation [38]:

$$g_m = \frac{dI_D}{dV_{GS}}\bigg|_{V_{DS}=const} \tag{2}$$

Higher g_m in a device means the gate has better control over drain current. The ratio of g_m/I_D in a device represents how much of the energy supplied (I_D) has been consumed for amplification (g_m) [38]. Fig. 7 shows this ratio in the DWG SP RD TFET is more than its counterparts in all gate voltages under study. Indeed, this superiority in DWG SP RD TFET indebted in its better subthreshold characteristics compared to its counterparts.
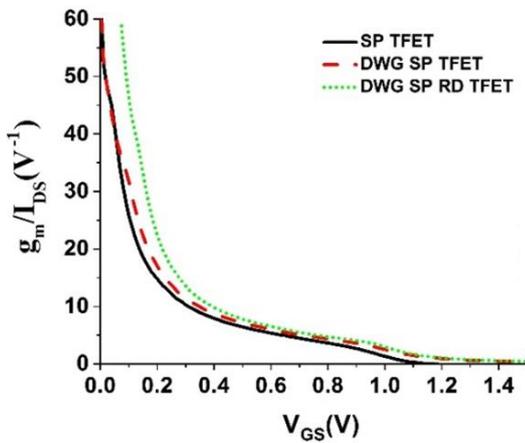
Fig. 7: gm/ID ratio of SP TFET, DWG SP TFET, and DWG SP RD TFET at VDS=1.0 V.

Due to DWG SP RD TFET shows excellent transfer characteristic and energy band diagram profile (because of auxiliary gate with higher metal workfunction), in the following we are going to investigate auxiliary gate workfunction variations effect on ON-current, OFF-current and point subthreshold swing (SS). As Fig. 8 shows, ON-current, OFF-current and subthreshold swing reduce by increasing workfunction value in auxiliary gate. Fig. 9 can help us to explain the reason. According to this figure, increasing the workfunction value causes the valance band to stay further from quasi-Fermi level at the source region.

Based on Fermi-Dirac distribution function, it is expected that the concentration of electrons with the energy higher than Fermi level to be reduced at room temperature and this causes ON-current to be decreased as indicated in Fig. 8(a). It seems WF$_{aux}$= 5.3 eV is the optimum for drive current which it can be Copper (Cu) or Nickel (Ni) metals 0. Increment in auxiliary gate workfunction also causes the height of knee joint profile in source-channel junction position to increase (both in Ec and Ev) and the barrier against minority carriers (electrons) in the p-type source raises.

In this case, lower lucky electrons can enter to the channel due to thermal emission mechanism and this leads OFF-current to reduce (Fig. 8(b)) and they can be much better controlled by gate. So, it is expected subthreshold swing (SS) to be reduced according to the Fig. 8(c).
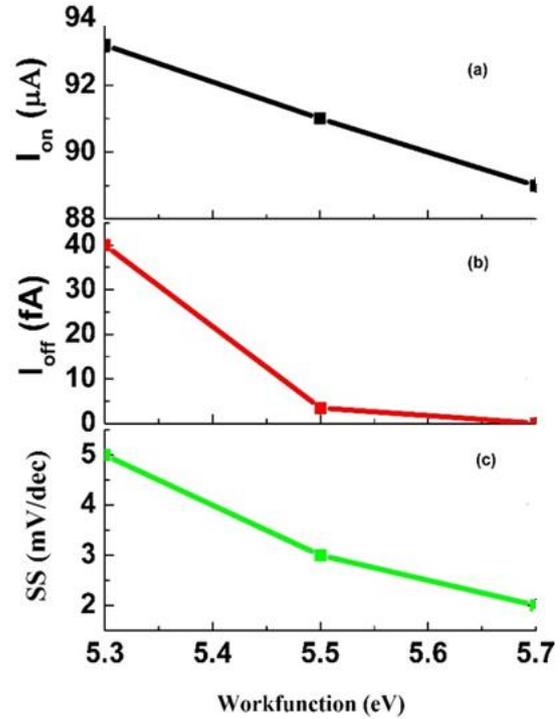
Fig. 8: (a) ON-current at $V_{GS}= V_{DS}$=1.0 V, (b) OFF-current, (c) point subthreshold swing of DWG SP RD TFET versus auxiliary gate workfunction variations at V_{GS}=0 and V_{DS}=1.0 V.
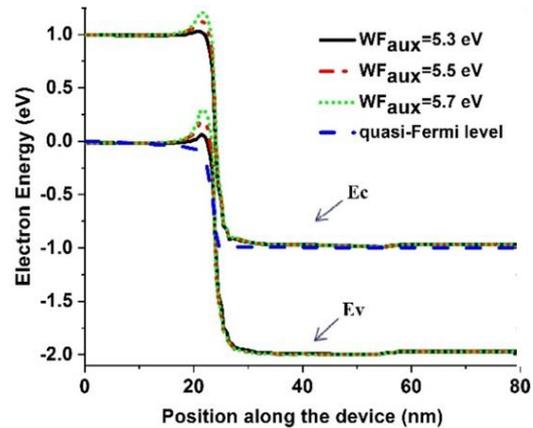
Fig. 9: Energy band diagram profiles of DWG SP RD TFET at different workfunction values in auxiliary gate at $V_{GS}=V_{DS}$=1.0.

Finally, Table 2 compares some figures of merits in this work (DWG SP RD TFET) with other published works in the TFET domain at the same technology node. I$_{ON}$/I$_{OFF}$ ratio and subthreshold slope are presented in this table. It is seen that our proposed device has steep subthreshold slope while maintaining high value of

I_{ON}/I_{OFF} ratio compared to other published works.

Table 2: Comparison of Ion/Ioff Ratio and subthreshold slope of DWG SP RD TFET with other published works

parameter	This work	[4]	[41]	[42]	[43]
I_{ON}/I_{OFF}	4.38×10^9	2×10^9	2.7×10^{12}	2×10^5	1×10^7
SS (mV/dec)	6	48	35	45	2.8

Conclusion

In this work we proposed dual workfunction gate source pocket retrograde doping tunnel field effect transistor (DWG SP RD TFET). In order to increase the ON-current in this device, we utilized several methods including incorporation of high-K material in top oxide, source pocket in channel and a thin auxiliary gate with high workfunction over the source region. Incorporating auxiliary gate over the source also caused a barrier formation in the energy band diagram profile of this device which it leds electron concentration in the channel, subthreshold swing and OFF-current to be reduced. We also embedded a retrograde doping underneath the channel to virtually decrease channel thickness for further reduction in OFF-current and subthreshold swing. Based on excellent I_{ON}/I_{OFF} ratio (> 10^9), low point subthreshold swing (SS<=6 mV/dec) and high gm/ID ratio which achieved in our simulations, this device can be among promising candidates for future technology nodes.

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