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Research paper

Design of High Frequency Single and Double Gate Laterally-Contacted InGaAs/InAlAs HEMTs

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Abstract

Background and Objectives: High electron mobility transistors (HEMTs) are designed so that they are able to work at higher frequencies than conventional transistors and this has made them an attractive topic of research.
Methods: Two developed designs of InGaAs/InAlAs high electron mobility transistors have been studied. The proposed laterally contacted HEMTs satisfy the desired high frequency characteristics and are good candidates for high frequency applications. Two kinds of HEMTs have been designed and simulated: single-gate laterally contacted HEMT (SGLC-HEMT) and double-gate laterally contacted HEMT (DGLC-HEMT).
Results: The proposed SGLC-HEMT exhibits 111 GHz current-gain cut-off frequency. By using double-gate design, the current-gain cut-off frequency has been increased to 256 GHz. The simulation results show that the maximum oscillation frequency for the proposed SGLC and DGLC HEMTs, are 410 GHz and 768 GHz, respectively. The maximum value of transconductance (gm) for SGLC-HEMT is obtained 620 mS/mm while it is 1130 mS/mm for DGLC-HEMT.
Conclusion: In order to increase the f_T and f_{max}, instead of decreasing the gate length which is a restricted solution because of short channel effects, a very efficient structure was proposed. The designed HEMT benefits from laterally source and drain contacts. The results showed superior performance of the laterally contacted HEMTs compared to top contacted ones. The best frequency response was obtained for DGLC-HEMT. The proposed DG-HEMT design could improve the current-gain cut-off frequency and maximum oscillation frequency to 256 GHz and 768 GHz, respectively. The comparison of the performance of the DGLC-HEMT with SGLC-HEMT and with previously reported double gate HEMTs, verified the significant improvements in DC and AC characteristics of the HEMTs caused by the proposed design.

Introduction

Nowadays, high electron mobility transistor (HEMT), due to its attractive characteristics is one of the inseparable elements in electronics. They have high transconductance (g_m), low saturation voltage and are able to work at higher frequencies than conventional transistors [1, 2]. By developing the fabrication technology to sub-micron, HEMTs with gate lengths equal to 100 nm and less, exhibit good characteristics such as high g_m, high current-gain cut-off frequency (f_T), and large maximum oscillation frequency (f_{max}). Though f_T is of great interest for digital circuits, enhancement in

f_{max} is also required for analog and power applications [3]. The main cause of reduction in g_m with increasing L_g is its inability to maintain the desired aspect ratio ($\alpha=L_g/d$) [4], where d is the distance between the gate electrode and hetero-interface. For a SG-HEMT with 300 nm gate, f_T and f_{max} have been reported as 108 GHz and 349 GHz, respectively [5]. Also, for a DG-HEMT with 50 nm gate length, the f_T and f_{max} have been reported as 162 GHz and 417 GHz, respectively [6]. Until 2014, the fastest HEMTs with f_T = 664 and f_{max} = 681 GHz have been fabricated based on InAlAs/InGaAs/InAlAs heterostructures [7]. These large values of frequencies can be obtained due to the high electron mobility (μ_e) and high saturation drift velocity of electrons in these heterostructures. The electron mobility, μ_e can be increased by reducing the molar fraction of In in a InGaAs quantum well (QW) because of the increase in the effective electron mass [8]. In addition, μ_e in HEMT, PHEMT, and metamorphic HEMT (MHEMT) can be increased by some methods such as improving the structural quality of the spacer layer in the barrier [9], using a well-designed heterostructure [8, 10], and improving the fabrication technology [11]. With the goal of improving the HEMT performance, several researches have been conducted on increasing the maximum oscillation frequency [12, 13], designing and fabricating good contacts [14-16], surface passivation [17, 18], and etc. Engineering of the transistor contacts has always been an attractive topic [19]. In this paper, the effects of the lateral source/drain contacts on the device performance have been investigated. The single gate and double gate HEMTs with lateral contacts have been simulated and their high frequency characteristics have been compared.

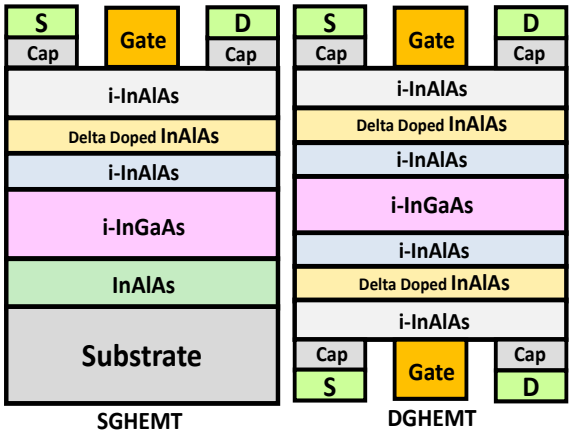

Fig. 1: The conventional top-contacted structures (SG-HEMT and DG-HEMT).

InGaAs/InAlAs single gate laterally contacted HEMT (SGLC-HEMT) and double gate laterally contacted HEMT (DGLC-HEMT) have been designed and studied with the goal of obtaining very high f_T and f_{max}. A brief explanation of InGaAs/InAlAs HEMTs have been presented in Section 2. Designed SGCL-HEMT and DGCL-HEMT structures are introduced in Section 3. Simulation results and discussions are presented in Section 4 and finally the paper is concluded in Section 5.

InGaAs/InAlAs HEMTS

In this paper we focus on InGaAs/InAlAs HEMTs. Two of most important parameters of III-V semiconductors that dictate their functionality in a device are the bandgap and the lattice constant. By exploiting the bandgap difference of III-V materials, it is possible to increase carrier concentration in the channel of transistor. This is done by forming a heterostructure using a doped wider bandgap material (e.g., InAlAs) and an undoped lower bandgap material (e.g., InGaAs). Bandgap of InGaAs and InAlAs are 0.76 eV and 1.48 eV, respectively [20]. Electrons fall into a trap due to formation of quantum well near the junction. Because channel is formed in InGaAs layer and this layer is donor-free, impurity scattering is absent at the channel which causes high mobility of electrons. For lattice matching, the mole fraction of In_x for $In_xGa_{1-x}As$ and $In_xAl_{1-x}As$ compounds should be 0.53 and 0.52, respectively.

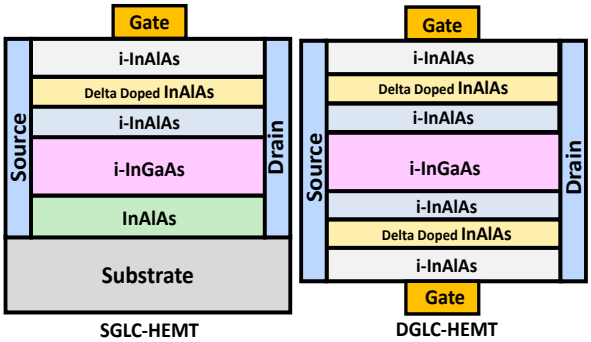

Fig. 2: The proposed single gate and double gate laterally contacted HEMTs.

Proposed Laterally Contacted HEMTs

The conventional structures of the InGaAs/InAlAs HEMTs (SG-HEMT and a DG-HEMT) have been shown in Figure 1. As can be seen in Figure 1, the HEMTs are top contacted and the source and drain electrodes are positioned on the top of the structures. In this paper, we have investigated the effect of the source and drain design on the device performance. If we change the position of the source and drain contacts from top of the device to the sides of the device, new HEMT designs would be achieved. We have proposed laterally contacted source and drain HEMTs as shown in Figure 2.

As illustrated in Figure 2, the proposed InGaAs/InAlAs HEMTs have the same heterostructures as their top contacted counterparts. But, the top contacts have been replaced by lateral contacts which will change the transistors behavior. Simulations show that the lateral

contacts affect the device performance considerably. The structures of the designed SGLC-HEMT and DGLC-HEMT and their dimensions used in simulations are shown in Figure 3. As depicted in Figure 3(a), a 200 nm buffer layer of $In_{0.52}Al_{0.48}As$ on SiC substrate layer has been used to isolate the channel from substrate layer effects in SGLC-HEMT. $In_{0.53}Ga_{0.47}As$ channel layer with 20 nm thickness on the buffer layer forms a two-dimensional electron gas (2-DEG). To supply excess electrons to the channel, a heavily doped (1018 cm^{-3}) 5 nm thick delta-doped layer, has been introduced. In order to reduce the columbic interaction between diffused electrons in channel and the ionized donors of delta-doped layer, a very thin In0.52Al0.48As layer (2 nm) as a spacer has been located between channel layer and delta-doped layer. Schottky layer with thickness of 15 nm has been designed on top of delta doped layer. To avoid the parallel conduction effects, this layer is undoped. Finally, highly doped (1018 cm^{-3}) $In_{0.53}Ga_{0.47}$ as a cap layer with 10 nm thickness has been introduced to make good Ohmic source and drain contacts. The main idea in HEMTs is conduction through an undoped channel with a special heterojunction design to increase the mobility and switching speed of the transistor (electrons in the 2-DEG channel do not undergo impurity scattering and hence exhibit high mobility and velocity). If in addition to the channel, another conduction path exists (parallel conduction), it will slow down the device. That is why the Schottky layer with thickness of 15 nm on top of delta doped layer should be undoped to avoid parallel conduction. Each layer's mission in the proposed HEMT is as follows. The schottky layer is an intrinsic (undoped) InAlAs to avoid the parallel conduction effects. Below that, a thin heavily doped (5nm) layer of InAlAs (delta-doped layer), is introduced to supply excess electrons to the channel. A spacer layer of InAlAs with 2nm thickness is used as a sandwiched between the channel and delta doped layer in order to reduce the columbic interaction between diffused electrons in channel and the ionized donors of delta doped layer. Two-dimensional electron gas (2-DEG) is formed in undoped narrowband InGaAs layer of 20nm. A buffer layer of 200nm was used to isolate the channel from being affected by the substrate effects. AlInAs layers have to be undoped (schottky layer and spacer layer). If an AlInAs layer is doped (delta doped layer), its electrons should fall from doped InAlAs and trap in InGaAs (undoped channel) due to formation of quantum well near the junction. This way the conduction is limited to the channel and parallel conductions are eliminated to avoid slowing down the transistor. In our proposed design, source and drain electrodes has been placed at sides of the structure. The drain-source spacing of 1.5 µm is used for simulation study.

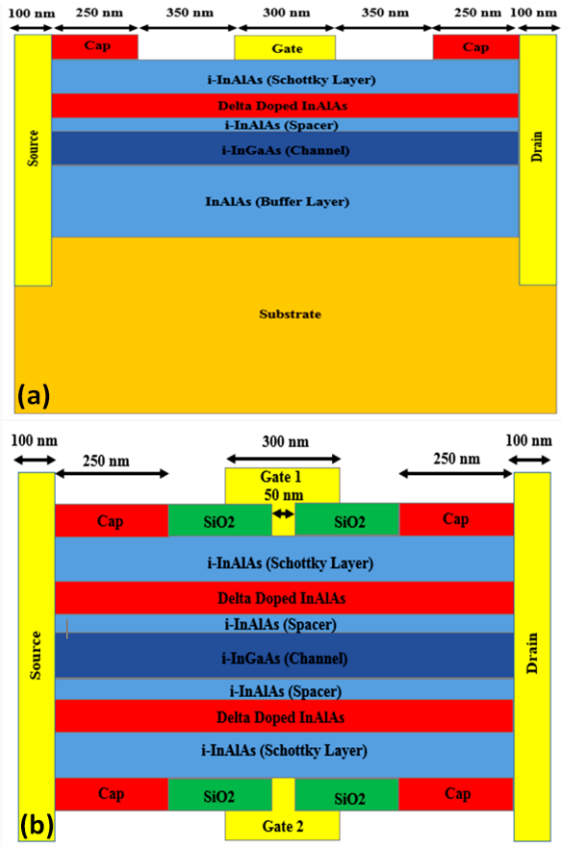

Fig. 3: 2D cross sectional view of a) SGLC-HEMT, b) DGLC-HEMT.

In order to achieve a high frequency InGaAs/InAlAs HEMT, we propose the DGLC-HEMT structure. The high frequency performance of this transistor is verified in the upcoming sections of the paper. As seen in Figure 3(b), compared to SGLC-HEMT, in DGLC-HEMT structure, all layers except buffer layer are duplicated symmetrically around the central channel. In order to fabricate the double gate device, first, like SGLC-HEMT, all layers are introduced. Then, by using transfer substrate technique [21] and removing buffer and substrate layers, all SGLC-HEMT layer are introduced to the back side of the wafer. T-gate contacts are introduced by using SiO_2 insulators. Thickness and doping concentration of different layers of the simulated SGLC-HEMT and DGLC-HEMT are tabulated in Table 1.

Table 1: Parameters of the Designed Structure

Layer	Thickness (nm)	Doping (cm^{-3})
Cap	10	1e18
Schottky	15	-----
Delta-Doped	5	1e18
Spacer	2	-----
Channel	20	-----

Results and Discussions

In this section, the InGaAs/InAlAs SGLC-HEMT and DGLC-HEMT have been simulated. The channel lengths have been chosen so that the results can be compared to other works. The parameters such as the drain current, transconductance (g_m), current-gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) have been calculated and compared. The comparison of the results at the end of the paper proves the efficacy of the proposed designs.

A. SGLC-HEMT

The devices have been simulated by means of SILVACO-ATLAS. Two models have been included in the simulations: field dependent mobility model (FLDMOB) and carrier quantization model (QUANTUM) [20]. Parameters used for modeling the devices are tabulated in Table 2.

Table 2: Parameters Used in Simulations

	$In_xAl_{1-x}As$ (x=0.52)	$In_xGa_{1-x}As$ (x=0.53)
E_g (300 K)	1.48 eV	0.76 eV
Affinity	4.2	4.72
N_C (300 K)	5.3e17	2.18e17
N_V (300 K)	1.09e19	8.44e18
Electron Mobility (cm^2/vs)	4100	10000
V_{sat}	2.1e7	3.2e7
Gate metal Work Function	4.69 eV	
Source and Drain Contacts	Ohmic	

The input current-voltage curve and transconductance (g_m) characteristics at drain voltage of 0.5 V for SGLC-HEMT are presented in Figure 4.

For the purpose of a fair comparison to other works, the channel length of the SGLC-HEMT is 300 nm. The drain current is 365 mA/mm at V_{GS}=1 V. The obtained maximum value of g_m is 620 mS/mm at V_{GS}=0.05 V. The frequencies f_T and f_{max} of the transistors have relations as below:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \quad (1)$$

$$f_{\max} = f_T\sqrt{\frac{R_{ds}}{4R_{in}}} = \frac{f_T}{\sqrt{4g_{ds}R_{in}}} \quad (2)$$

where C_{gs} is gate to source capacitance, C_{gd} is gate to drain capacitance, g_{ds}=1/R_{in} is drain to source conductance and R_{in} is the input resistance.

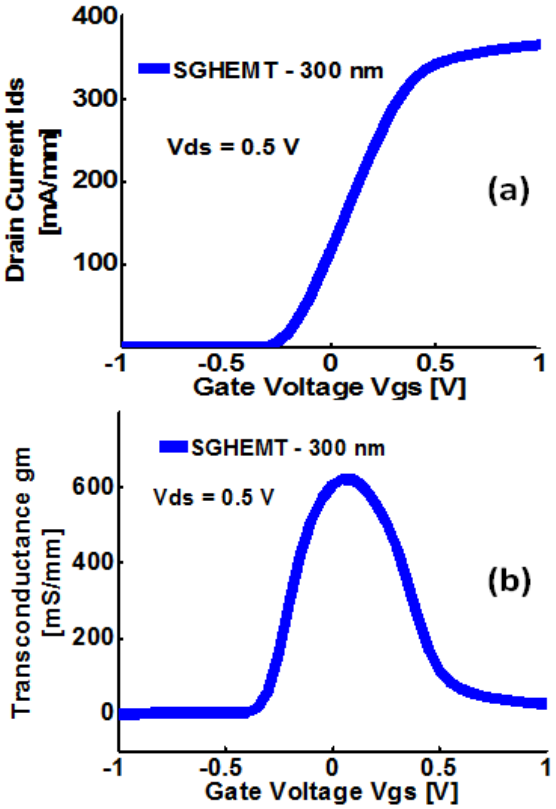

Fig. 4: a) ID-VGS characteristic and b) gm for SGLC-HEMT in VDS=0.5 V.

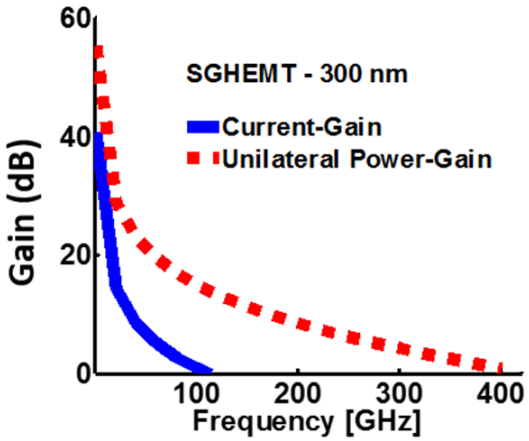

Fig. 5: Current gain and unilateral power gain for calculation of fT and fmax for SGLC-HEMT.

However, these parameters (f_T and f_{max}) can be calculated based on the frequency dependent current gain and unilateral power gain, as well. In order to calculate f_T and f_{max} the current-gain and unilateral power gain versus frequency have been plotted in Figure 5. As it is expected, in high frequencies the gains drop. The frequencies in which the gains reach unity (0 dB) are the critical values. Simulation results show that for the designed InGaAs/InAlAs SGLC-HEMT, f_T and f_{max} have values of 111 GHz and 410 GHz, respectively.

The effect of the gate length on the device performance has been discussed in the following lines.

By decreasing the gate length to 100 nm, the effects of the short gates on the characteristics of SGLC-HEMT have been studied. Drift diffusion equations have been solved again to obtain the input current- voltage (I_D-V_{GS}) and g_m characteristics as shown in Figure 6.

In comparison to 300 nm gate length, I_D and the maximum g_m have been decreased about 11% and 8%, respectively. The values of the drain current at V_{GS}=1 V and the maximum g_m of the 100 nm SGLC-HEMT have been obtained 325 mA/mm and 571 mS/mm, respectively. The values of f_T and f_{max} have been calculated about 231 GHz and 551 GHz, respectively, as shown in Figure 7.

As the gate length decreases, unlike I_D and g_m, frequency characteristics such as f_T and f_{max} are improved.

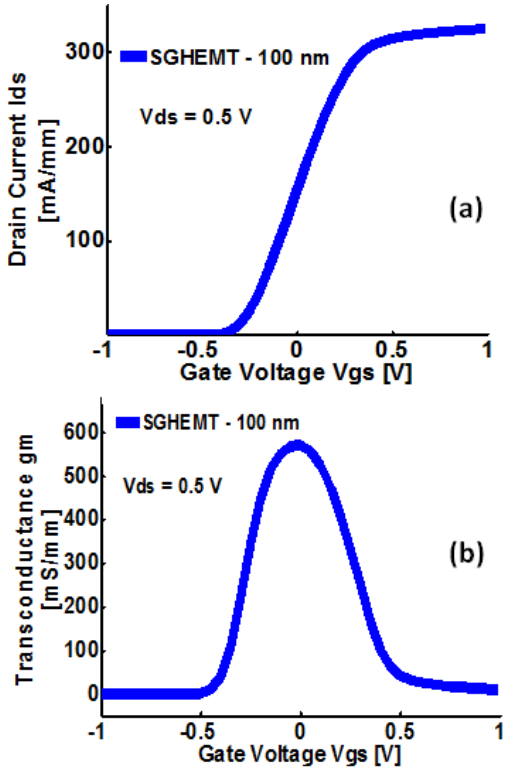

Fig. 6: a) ID-VGS. b) gm for 100 nm channel length SGLC-HEMT in VDS=0.5 V.

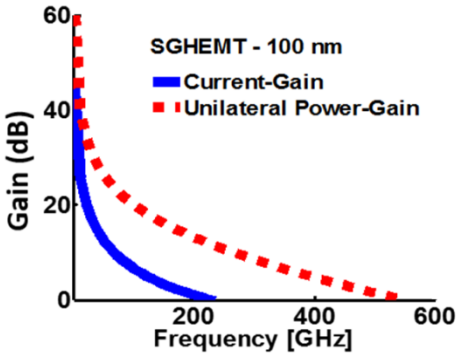

Fig. 7: Current gain and unilateral power gain for calculation of f_T and f_{max} for 100 nm channel SGLC-HEMT.

However, the frequencies of unity current gain and unity unilateral power gain are limited by short-channel effects [22] and the performance enhancement due to device scaling is restricted [23]. That is because maintaining the desired channel aspect ratio (α=L_g/d) is difficult (d is the vertical distance from gate to the channel) [24]. Also HEMT devices may show short-channel effects due to other non-idealities such as gate leakage current, traps, and impact ionization [23].

The short channel effects most are demonstrated in devices with gate length less than 100 nm [5]. In order to improve the HEMT performance in short channels, a second gate can be added to the transistor. This will be explained in the next section.

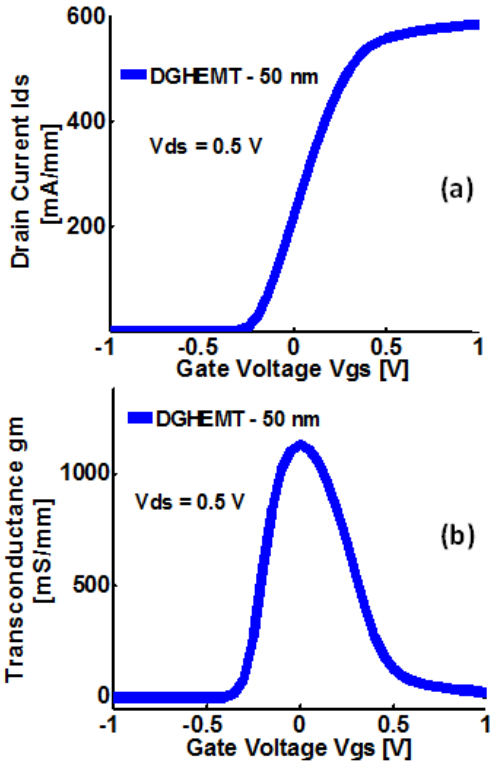

Fig. 8: a) ID-VGS characteristics and b) gm for DGLC-HEMT in VDS=0.5 V.

B. DGLC-HEMT

The solution to degraded characteristic parameters of the HEMTs (such as the decreased g_m) due to short channel is to use double gate HEMT (DG-HEMT) which also provides the benefit of having much larger f_T and f_{max}.

A DG-HEMT can be designed by removing the substrate in SG-HEMT and replacing it with duplicated layers around the channel as shown in Figure 2. DG-HEMTs, due to more control of carriers transfer in channel and also maintaining the desired aspect ratio, are suitable to improve HEMTs characteristics. Our proposed high frequency InGaAs/InAlAs HEMT is double gate and laterally contacted.

The simulations for DGLC-HEMT are presented in the following lines.

The input current-voltage and transconductance curves for V_{DS}=0.5 V are shown in Figure 8. As shown in Figure 8, I_D at V_{GS}=1 V is 583 mA/mm and maximum g_m is 1130 mS/mm which are about 60% and 82% greater than SGLC-HEMT, respectively.

Simulations results show outstanding increases in f_T and f_{max} values. As shown in Figure 9, f_T is about 256 GHz. Also f_{max} is 768 GHz which have significant improvements compared to SGLC-HEMTs.

The results show that the DGLC-HEMT structure is an ideal candidate for high frequency applications. As shown in Figure 9, the current gain and the unilateral gain decrease more slowly than conventional HEMTs and reach unity (0 dB) in much higher frequencies than conventional designs.

This means that the proposed InGaAs/InAlAs DGLC-HEMT is a transistor suitable for high frequency applications.

C. Comparison

In this section by comparing the obtained results to each other and to the previously reported InGaAs/InAlAs HEMTs, the superior performance of the proposed SG and DG laterally contacted HEMTs has been proved.

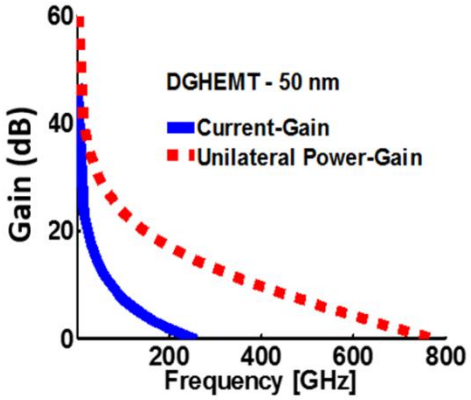

Fig. 9: Current gain and unilateral power gain for calculation of fT and fmax in DGLC-HEMT.

The obtained results for SGLC-HEMT and DGLC-HEMT have been tabulated in Table 3.

As illustrated in Table 3, for SGLC-HEMT, shortening the channel length results in the degradation of the drain current and the transconductance, however, the current-gain cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) have become higher.

This is similar to the gain bandwidth trade off that exist between the gain and the cutoff frequency of the transistors. As discussed previously, the short channel effects limit the performance of the HEMTs and this problem can be solved by using a double gate HEMT.

Table 3: Comparison between the Designed SGLC-HEMTs and DGLC-HEMT

Device Characteristic	SGLC-HEMT		DGLC-HEMT
Channel Length (nm)	300	100	50
I_D (mA/mm) at V_{DS}=0.5 V and V_{GS}=1V	365	325	583
Maximum g_m (mS/mm)	620	571	1130
f_T (GHz)	111	231	256
f_{max} (GHz)	410	551	768

For double gate HEMTs, all of the parameters have been improved compared to the single gate HEMTs. In order to present an illustrative comparison, we have compared the results of gain and frequency characteristics obtained for the proposed SGLC-HEMT and DGLC-HEMT with previous works on InGaAs/InAlAs HEMTs as shown in Table 4.

From the data in Table 4, it is clear that in [5] and [6] all the transistor parameters (transconductance, cutoff frequency and the maximum oscillation frequency) have improved in double gate design compared to the single gate design. As shown in Table 4, the proposed SGLC-HEMT has improved the f_T and f_{max} compared to the previous works. It can also be concluded that the proposed InGaAs/InAlAs DGLC-HEMT which benefits from laterally contacts (compared to top contacts in other works) is a successful design for providing much larger f_T and f_{max} than conventional structures while its g_m is also larger than the single gate HEMTs.

Table 4: Comparison of the Proposed HEMTs with Previous Works

Device	Channel Length (nm)	g_m (mS/mm)	f_T (GHz)	f_{max} (GHz)	Ref.
SGHEMT	300	910	108	349	[5]
	300	840	108	346	[6]
	300	620	111	410	This work
DGHEMT	50	1810	175	448	[5]
	50	1720	179	482	[6]
	50	1130	256	768	This work

Since parallel conductions have been prevented, all the current is conducted through the 2DEG formed in the undoped channel which provides a high mobility. Performance improvement of lateral source and drain contacts can be attributed to two main mechanisms. First, in the laterally contacted InGaAs/InAlAs HEMT, the 2-DEG is in direct connection to the source and drain

contacts. This helps in improving the current conduction. The carriers can run into the source and drain faster and this makes the device appropriate for high switching speed and high frequency applications. Second, the gate-source and gate-drain capacitances are smaller in laterally contacted HEMTS because the distance between gate and source/drain contacts is larger and because of the same reason the parasitic capacitances are smaller than other designs.

As can be seen in the Table 4, the f_T of the DG-HEMT has been increased from 175 GHz and 179 GHz [5, 6] to 256 GHz in this paper. The DGLC-HEMT could also improve the f_{max} from 448 GHz and 482 GHz in previous works to 768 GHz which is a great improvement. Another interesting point is that the improvement in the f_T and f_{max} compared to other works is much larger for DGLC-HEMT than that of the SGLC-HEMT. The obtained results verify that using laterally source and drain contacts in InGaAs/InAlAs DGLC-HEMT improves its high frequency performance significantly. This work proposes this design as a very high frequency HEMT suitable for high frequency applications.

Conclusion

Improved designs of InGaAs/InAlAs HEMTs were presented and studied. In order to increase the f_T and f_{max}, instead of decreasing the gate length which is a restricted solution because of short channel effects, a very efficient structure was proposed. The designed HEMT benefits from laterally source and drain contacts. The results showed superior performance of the laterally contacted HEMTs compared to top contacted ones. The best frequency response was obtained for DGLC-HEMT. The proposed DG-HEMT design could improve the current-gain cut-off frequency and maximum oscillation frequency to 256 GHz and 768 GHz, respectively. The comparison of the performance of the DGLC-HEMT with SGLC-HEMT and with previously reported double gate HEMTs, verified the significant improvements in DC and AC characteristics of the HEMTs caused by the proposed design.

Author Contributions

Zoheir Kordrostami designed the devices, Fatemeh Khalifeh provided the simulation results. Samaneh Hamedi carried out the data analysis. Zoheir Kordrostami, Fatemeh Khalifeh and Samaneh Hamedi wrote the manuscript.

Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancies have been completely observed by the authors.

Abbreviations

HEMT	High electron mobility transistors
SGLC-HEMT	Single-gate laterally contacted HEMT
DGLC-HEMT	Double-gate laterally contacted HEMT

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