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Research paper

A Novel Low-Power FPGA-based 1-1 MASH ΔΣ Time-to-Digital Converter Employing one Counter for both Stages

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Abstract

Background and Objectives: Beside acceptable performance, power consumption and chip area are important issues in embedded systems that should be taken into consideration.
Methods: In this paper, a novel continuous-time 1-1 MASH ΔΣ Time-to-digital converter (TDC) is presented. Since the proposed design utilizes 12-bit quantizer based on Gated Switched-Ring Oscillator (GSRO) for both stages, it has been implemented all-digitally. By using a novel structure, only one multi-bit counter is employed for both stages, therefore the required hardware for implementation of this work is much less than conventional TDCs. As a result, complexity, chip area and power consumption would decrease considerably.
Results: We implemented the proposed design prototype on an Altera Stratix IV FPGA board. Measured results demonstrate that although this work uses less complex architecture in comparison with previous works, it provides appropriate performance such as 60.7 dB SNR within 8 MHz signal bandwidth at 400 MHz sampling rate while consuming 2.79 mW.
Conclusion: Experimental results reveals suitability of the proposed TDC to be incorporated in fast and accurate applications such as ADPLLs and high-resolution photoacoustic tomography. Also, by adjusting the proposed novel structure with more stages higher order of noise-shaping can be attained to enhance SNR and time-resolution further.

Introduction

Time-to-digital converters (TDCs) are basically used to measure a time interval which serves an important role in many applications such as photoacoustic tomography [1], Time-of-Flight (ToF) systems [2], frequency synthesizers [3], [4] and all-digital phase-locked loops (ADPLLs) [5]. So far, various architectures have been proposed which had been trying to improve performance critical parameters of TDCs such as SNR, dynamic range, resolution and bandwidth [6]-[13]. Due to operating in Nyquist rate, the mentioned parameters higher than that of their oversampling counterparts are not achievable by those architectures.

Recently, trends to ΔΣ TDCs have been increased owing to their inherent property of noise-shaping. In the meantime, Voltage-domain ΔΣ TDCs which are commonly implemented using analog circuitries have been introduced [14], [15]. But, time-domain ΔΣ TDCs comprising of digital components such as multi-bit counter and ring oscillator [16], [17] are better choices to benefit from CMOS process scaling. However, limitation of oversampling ratio (OSR) and noise-shaping order prevents these architectures to achieve fine time-resolution. Even though multi-stage noise-shaping

(MASH) TDCs can be formed by cascading identical ring oscillator-based TDCs to obtain finer time-resolution, but discrepancy in oscillators operating frequency leads to systematic error that puts a burden of calibration unit on designer to diminish the error [18]. Reference [19] has presented a 1-1 MASH TDC based on GSRO that can achieve a fine time-resolution while it does not need calibration. By increasing the order of noise-shaping, in-band noise power can be decreased. Therefore, a third-order MASH ΔΣ TDC by cascading three GSRO-TDCs and a fourth-order ΔΣ TDC by increasing the loop order using time-domain error-feedback filter have been introduced in [20] and [21], respectively. Although High-order ΔΣ TDCs can demonstrate higher SNR, but they require stringent design considerations, more implementing hardware and hence consume more power and chip area. In [22], a multirate second-order ΔΣ GSRO-TDC has been proposed. Taking advantage of high-speed FPGA board, it utilizes higher operating frequencies for GSROs and sampling clocks. In addition, it employs multirating technique to improve performance further. As a result, it achieves finer time-resolution and higher SNR. Yet, it can be modified to attain a less complex structure in order to reduce power consumption and chip area. With the advent of high-performance FPGA chips and scaling of CMOS technology, fast and accurate FPGA-based and application specific integrated circuit (ASIC) TDCs have been introduced [23]-[27]. However, advantages of FPGAs attract some of all-digital TDC designers. On the one hand ASIC implementation takes advantage of design optimization, but on the other hand the main benefit of FPGA implementation is flexibility which allows designer to provide a programmable design that can be tailored for a vast range of applications.

In this paper, a novel FPGA-based 1-1 MASH ΔΣ GSRO-TDC is presented. Also, operation principle and FPGA implementation are described in detail. Although this work reveals lower complexity rather state-of-the-art TDCs by employing only one multi-bit counter for both stages, it can achieve acceptable SNR and bandwidth while providing fine time-resolution and superior dynamic range and Figure-of-Merit (FoM).

This paper is organized as follows. A background of MASH ΔΣ GSRO-TDCs is presented in Section 2. The operation principle and implementation details of the proposed all-digital second-order ΔΣ TDC are described in Section 3 and Section 4, respectively. The measured results of the prototype TDC are discussed in section 5. Finally, conclusions are drawn in Section 6.

MASH ΔΣ GSRO-TDC

Inherent property of noise-shaping is the main reason for popularity of ΔΣ TDCs. In addition, by utilizing higher noise-shaping order the noise power in band of interest can be lowered [28]. Thus, higher noise-shaping order is of interest. By adding more stages or incrementing loop order, the order of noise-shaping can be increased but both manners result in more complexity, power consumption and chip area. Therefore, in designing ΔΣ TDCs a trade-off between performance and complexity is inevitable. Hence, to achieve acceptable performance, first, the proper order of noise-shaping must be chosen carefully, then improvement of critical specifications of TDC must be maximized. To develop the idea of the proposed structure, this section provides the theoretical background of ΔΣ GSRO-TDCs. We use [19] as our benchmark to describe this theoretical background.

As noted previously, phase-domain quantization error leakage caused by frequency difference between two SROs degrades performance of a 1-1 MASH SRO-SRO TDC so that it cannot achieve second-order noise shaping properly. This problem can be solved by exploiting a SRO with phase-holding gates added to its supply and ground (SG) that is called GSRO. Keeping phase properly in GSRO suppresses leakage perfectly. Fig. 1 depicts the operation principle of a GSRO. As can be seen, GSRO acts as a Switched-Ring Oscillator (SRO) when the gates are closed and holds its phase when the gates are open. Generally, GSRO has three operating frequencies: f_{max}, f_{min} and 0. The block diagram of the 1-1 MASH GSRO-TDC introduced in [19] where two identical GSROs are exploited in the first and second stages, and also the detailed operation principle of that are shown in Fig. 2 and Fig. 3, respectively. The time interval between Start and Stop pulses (*IN*) is applied to the TDC using an on-chip pulse generator (PulseGen). GSRO1 is configured as an SRO by closing its SG gates. For controlling the SG gates of the GSRO2 and synchronization between GSROs, QEGen produces the pulses of first stage quantization error (Q_1) and frequency synchronization (Q_{IN}) each cycle using *IN*, *CLK*, and output of the GSRO1 (Y_1).

As shown in Fig. 3, benefiting from this approach oscillation frequency of GSRO1 and GSRO2 are the same during sampling period. By comparing output relationships of SRO-TDC and TDC using GSRO, we clarify superiority of GSRO-TDC in quantization error leakage elimination. The z-domain SRO-TDC output is given by:

$$2\pi D_{OUT}=z^{-1}D_1-(1-z^{-1})D_2 \tag{1}$$

$$=z^{-1}\phi_{SRO1}-z(1-z^{-1})^2\phi_{Q2}$$

$$+(1-z^{-1})(1-\frac{\phi_{SRO2}}{\phi_{Q1}})\phi_{Q1} \tag{2}$$

where the first stage quantization error in phase-domain and the second stage phase change are expressed as:

$$\phi_{Q1}=2\pi\int_{T_{Q1}} f_{SRO1}dt \tag{3}$$

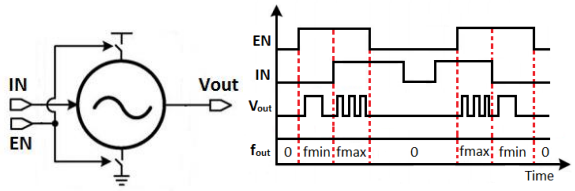
$$\phi_{SRO2} = 2\pi \int_{T_S} f_{SRO2} dt \,. \quad (4)$$

Nonetheless, when we exploit GSRO2 in the second stage, the GSRO2 phase change (ϕ_{GSRO2}) can be given by:

$$\phi_{GSRO2}[n] = 2\pi \int_{T_S} f_{GSRO2} dt$$

$$= 2\pi \int_{T_{Q1}[n]} f_{GSRO2} dt = \phi_{Q1}[n]. \quad (5)$$

From (5), it can be said that equality of (3) and (4) caused by using a GSRO in the second stage results in leakage suppression effectively. Hence, GSRO-TDC can achieve second-order noise shaping properly without gain calibration in contrast to SRO-SRO TDC [19].



(a) (b)

Fig. 1: (a) Block diagram of a GSRO and (b) waveforms [22].

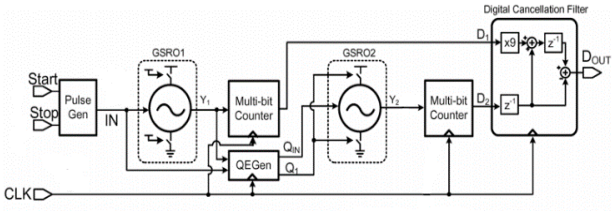


Fig. 2: 1-1 MASH ΔΣ GSRO-TDC architecture [19].

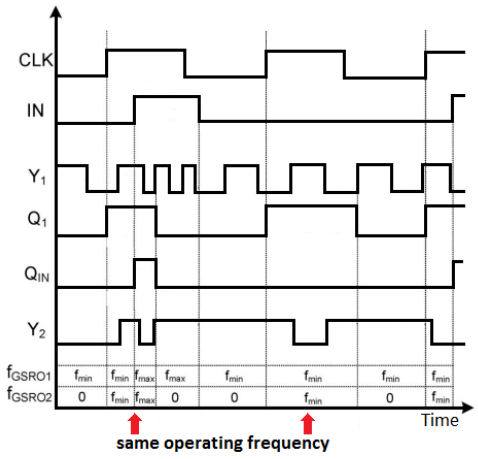


Fig. 3: Detailed operation principle of the 1-1 MASH GSRO-TDC [22].

It is worth noting that as a residue pulse is required every cycle to accomplish second-order noise-shaping, designer must set frequency of the GSRO higher than sampling frequency (f_S) to guarantee existing minimum of one rising edge withing a period of sampling. So, we can say that operating frequency of GSRO puts a limitation on OSR in GSRO-TDC.

In this work, f_{min} and f_{max} of GSROs are set at 2 GHz and 4 GHz, respectively which indicates 2 and 1.6 times increase rather their counterpart in [19]. As a result, we can set f_S up to 2 GHz in this work that allows higher OSRs and achieving time-resolution below 0.5 ps. Moreover, by designing a novel structure, we propose a new 1-1 MASH ΔΣ TDC in which only one multi-bit counter is employed for quantizing the output of both stages simultaneously that leads to reduction of implementing hardware of a second-order ΔΣ GSRO-TDC and subsequently its power consumption.

Proposed Novel Structure

As described in previous section, SRO–GSRO architecture can mitigate leakage significantly. Nevertheless, the main remaining problem is large amount of implementing hardware which causes more complexity and power consumption. In this work, we propose a novel structure to overcome this problem.

The block diagram of the proposed design is shown in Fig. 4. As shown, the main idea is exploiting only one multi-bit counter for both stages rather than one multi-bit counter for each stage. Therefore, by using a few digital logic gates the required hardware for implementing the second-order ΔΣ TDC decreases remarkably. So, it should be noted that, this work focuses on reducing complexity of SRO–GSRO second-order ΔΣ TDC by optimizing architecture design using a novel structure described in this section.

As shown in Fig. 4, in order to employ only one multi-bit counter for both stages their output (Y_1 and Y_2) are merged and fed to the only multi-bit counter used in the proposed TDC. We use a simple XOR gate to merge the pulses of Y_1 and Y_2. According to XOR truth table, the output is HIGH (i.e. logical 1) when inputs are different from each other. So, when one of Y_1 and Y_2 are 1 and another is 0, the XOR output (Y_M) is 1. Therefore, we can see in Fig. 5 that the rising edges number of Y_M is equal to sum of the rising edges number of Y_1 and Y_2. The only error is made when the rising edges of both pulses occur simultaneously. To avoid the mentioned error, as depicted in Fig. 6, pulses of Y_2 are delayed, so that the rising edges of Y_2 occur at falling edges of Y_1. Hence, it would be guaranteed to avoid any coincidence of Y_1 and Y_2 rising edges. As mentioned above, Y_M are fed to multi-bit counter and it counts the number of rising edges. To extract the count number of Y_1 (CNT_1) and Y_2 (CNT_2) from the aggregate counted number (CNT_A), we have proposed a novel solution described as follows.

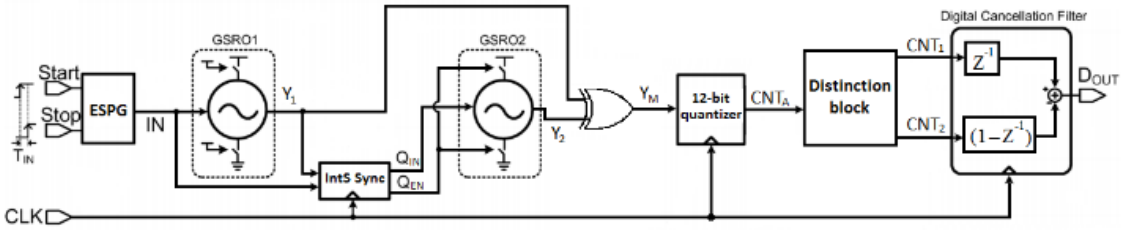


Fig. 4: Block diagram of the proposed 1-1 MASH TDC.

Since f_{max} and f_{min} of GSROs are specified, the number of rising edges belong to them are determined as well. Thus, we can use below algorithm to distinguish the number of CNT_1 and CNT_2.

If $CNT_A > CNT_{max}$ ***then***
$CNT_2 = CNT_A - CNT_{max}$
Eleseif $CNT_A < CNT_{max}$ ***&&*** $CNT_A > 2\ CNT_{min}$ ***then***
$CNT_2 = CNT_A - CNT_{min}$
$CNT_1 = CNT_A - CNT_2$

where CNT_{max} and CNT_{min} are the number of rising edges of Y_1 when GSRO operates at f_{max} and f_{min}, respectively.

The above algorithm is accommodated in distinction block (Fig. 4) to distinguish the number of CNT_1 and CNT_2 from CNT_A. According to the algorithm, it can be inferred that distinction block consists of a simple comparator and subtractor while a 12-bit quantizer which is saved in this work comprises of a 12-bit counter, two registers and a subtractor. It is clear that the latter consumes much more power compared with the first. The only condition that must be held so that we can incorporate the above algorithm is $CNT_2 < CNT_{min}$. As described in section 2, since SG gates of GSRO1 are always closed and it acts as a SRO, it operates even in LOW (i.e. logical 0) state of input signal (*IN*) while GSRO2 is enable only when Q_{EN} comes. As can be seen in Fig. 3, before CNT_2 can exceed CNT_{min}, Q_{EN} disappears and GSRO2 is disabled. Hence, the mentioned condition is always held.

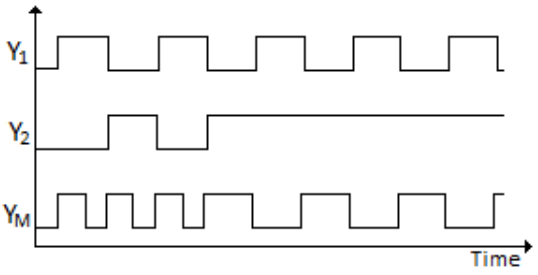
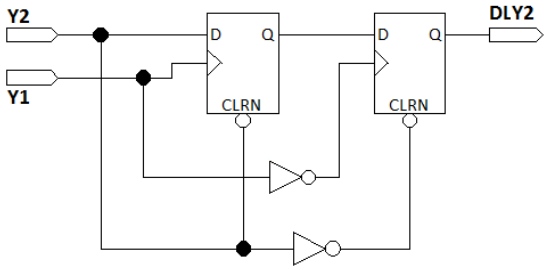


Fig. 5: Merging Y1 and Y2 using XOR gate.

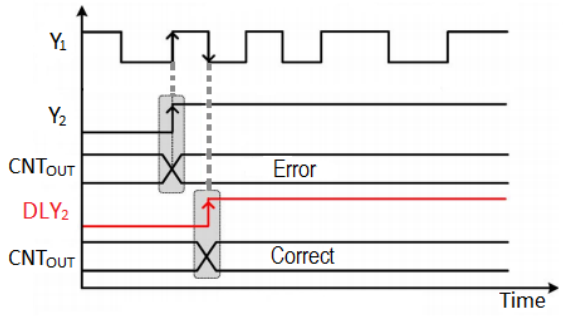
A related point to consider is that as this work utilizes a modified structure, CNT_1 and CNT_2 are fed to digital cancellation filter (DCF) rather than D_1 and D_2 in [17] to obtain digital output of TDC (D_{OUT}). But, distinction block produces CNT_1 and CNT_2 so that they can be considered as counterparts of D_1 and D_2 in [17]. Thus, similar to conventional ΔΣ TDCs, signal transfer function (STF) of the second stage (z^{-1}) and NTF of the first stage ($1 - z^{-1}$) filter CNT_1 and CNT_2, respectively in DCF. Eventually, D_{OUT} is attained by subtraction of CNT_2 from CNT_1 that can be written as:

$$D_{OUT} = z^{-1}CNT_1 - (1 - z^{-1})CNT_2$$
$$= \frac{1}{2\pi}(\phi_{Q1}(z) - z(1 - z^{-1})^2\phi_{GSRO2}(z)) \quad (6)$$

It is obvious from (6) that the proposed ΔΣ TDC achieves second-order noise-shaping as expected. Also, another positive aspect of this work is taking advantage of all-digital designing and implementing on high-performance Altera Stratix IV FPGA board which allow us on-chip implementation of DCF incorporating built-in logic and arithmetic units of FPGA board.



(a)



(b)

Fig. 6: Delaying rising edge of Y_2 to prevent error, (a) schematic of delay generator unit, (b) timing diagram.

In order to verify operation of the proposed TDC the timing diagram of that in several conditions is shown in Fig. 7. First, at 100 MHz *fc* and 200 MHz f_S, input pulses with 1 ns and 4 ns time intervals are applied to the proposed TDC (Figs. 7(a) and (b)).

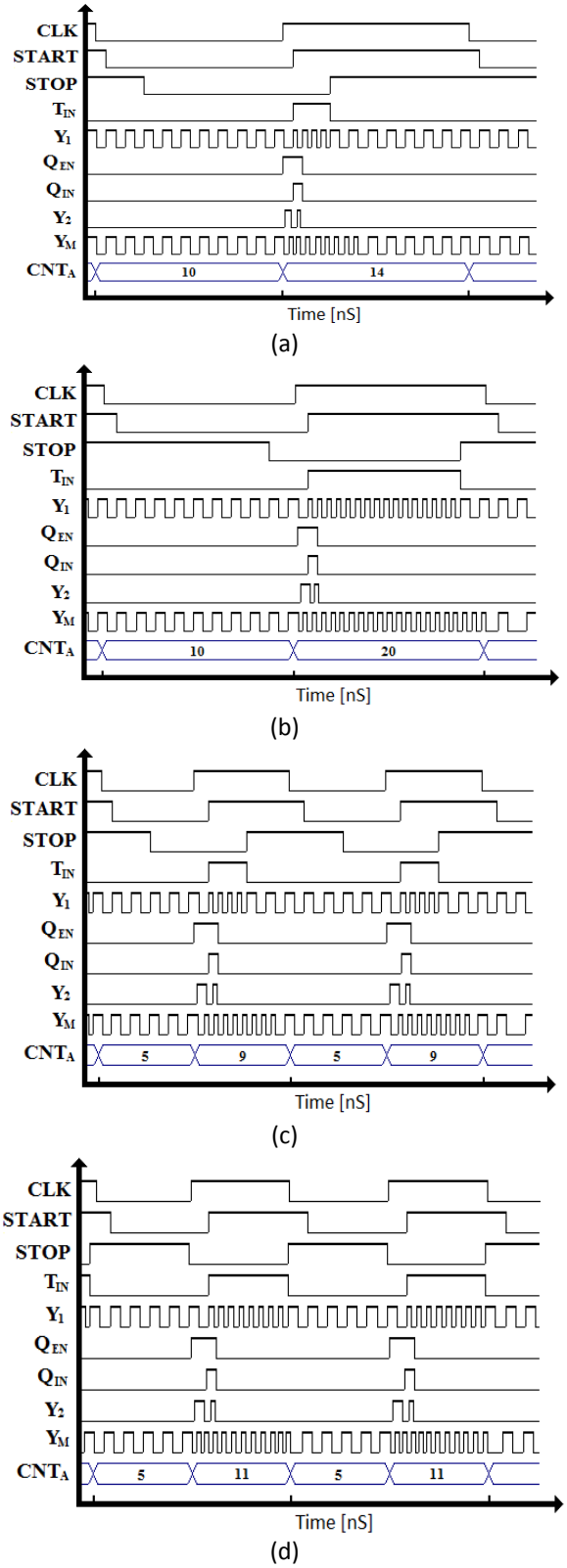


Fig. 7: Timing diagram of the proposed 1-1 MASH TDC. (a) f_S = 200 MHz with T_{IN} = 1 ns, (b) f_S = 200 MHz with T_{IN} = 4 ns, (c) f_S = 400 MHz with T_{IN} = 1 ns, (d) f_S = 400 MHz with T_{IN} = 2 ns.

As can be seen, Q_{EN} and Q_{IN} are generated every cycle to enable GSRO2 and synchronize its operating frequency with GSRO1. So, it can be surmised that any phase-domain quantization error leakage caused by frequency difference between GSROs can be removed efficiently by this approach that results in achieving second-order noise-shaping perfectly. Another case with 200 MHz *fc* and 400 MHz f_S has been provided to assert high-frequency operation of the proposed design. Figs. 7(c) and (d) illustrate the timing diagram of this case for 1 ns and 2 ns input intervals. It is evident from Fig. 7 that the proposed TDC is proved to be a reliable 1-1 MASH ΔΣ TDC that can operate accurately in precise applications such as frequency synthesizers, ADPLLs and range finders. Also, as this work benefits from high-performance Altera Stratix IV FPGA board, it utilizes operating frequencies for GSROs higher than their counterpart in state-of-the-art ΔΣ GSRO-TDCs that allows us to take advantage of higher OSR to gain finer time-resolution. Moreover, unlike other works no external source is needed to provide f_S for TDC operation since built-in clock circuitries of Altera Stratix IV FPGA board provide it properly. Thus, we can claim that the proposed design not only reduces the implementing hardware benefiting from a novel structure, but also facilitates measurements by removing the need of applying f_S to TDC using discrete sources.

Implementation Details

A. Sampling Clock and GSRO

Implementing the proposed design on an efficient FPGA board is a remarkable advantage of this work that allows utilizing built-in oscillator and PLLs of FPGA board to establish required clocks for TDC operation. Hence, we incorporate built-in 100 MHz crystal oscillator and PLLs of the FPGA board to extract different clocks (f_{S1}=200 MHz, f_{S2}=400 MHz, f_{min} and f_{max}). The method of generating different clocks in the proposed TDC is shown in Fig. 8(a) intuitively. As illustrated, f_{S1}, f_{S2}, f_{min} and f_{max}, are obtained by multiplying 100 MHz input clock by 2, 4, 20 and 40, respectively. Also, to emulate GSROs we have designed a control unit using simple logic gates (Fig. 8(b)) such that if Q_{EN} is 0, for each state of Q_{IN} Y is 0. When Q_{EN} is 1 but Q_{IN} is 0 output is f_{min}. If both Q_{EN} and Q_{IN} are 1 the unit passes f_{max} to the output.

B. Inter-Stage Synchronizer (IntS Sync)

Accurate operation of 1-1 MASH ΔΣ GSRO-TDC demands a unit to synchronize operating frequency of two GSROs to prevent leakage. For this purpose, IntS Sync (Fig. 4) is exploited in the proposed TDC to produce Q_{EN} and Q_{IN} every cycle which performs synchronization as appropriated. Figs. 9(a) and (b) show the block diagram and timing diagram of this unit. As shown, this unit consists of an edge-sensitive pulse generator (ESPG), two DFFs and two AND gates. Fig. 9(c) depicts the schematic of ESPG. This block is used to produce a pulse with the width of interval between rising edges of Start

and Stop pulses. The resulted Q_{EN} is fed to GSRO2 to enable it. It should be mentioned that if this pulse is narrower than rising time of the ESPG it would be ignored. Therefore, as switching time of GSRO gates is limited, a narrow Q_{EN} leads to deadzone problem which declines the performance of the proposed TDC. However, the remedy of this problem is adding a static offset of 2π to Q_{EN} using *DFF2*. DCF removes this offset to prevent degradation of proficiency of the proposed 1-1 MASH ΔΣ TDC [19].

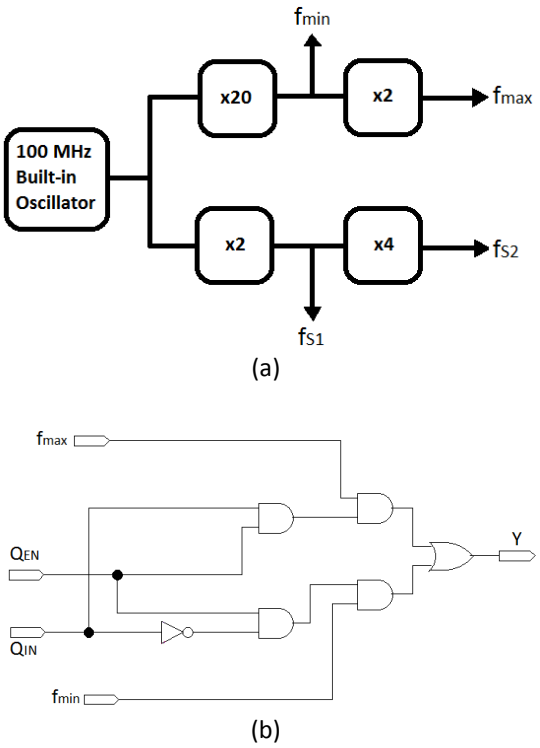


Fig. 8: (a) Utilizing built-in 100 MHz Oscillator in the proposed TDC to generate required clocks, (b) control unit for emulating GSRO.

C. The 12-bit Quantizer

As mentioned in section 2, on the one hand setting f_S lower than f_{min} guarantees a residue pulse to be occurred each cycle, but on the other hand being f_{min} greater than f_S may lead to occurring a number of rising edges during a sampling period which demands employing a multi-bit quantizer rather than a one-bit quantizer. In this way, we exploit built-in counters and logic components of the FPGA board to build a 12-bit quantizer to quantize Y_1 and Y_2 every cycle. It is noteworthy that quantization using such number of bits results in a finer time-resolution in comparison with previous works, although this work employs less hardware taking advantage of a novel structure. However, coinciding the reset time of counter with rising edge of f_S is an error that must be avoided during operation of 12-bit quantizer [29]. Nevertheless, this error can be avoided by employing the delaying unit shown in Fig. 6(a) again to postpone rising edge of f_S after complete transition of counter output (CNT_{out}).

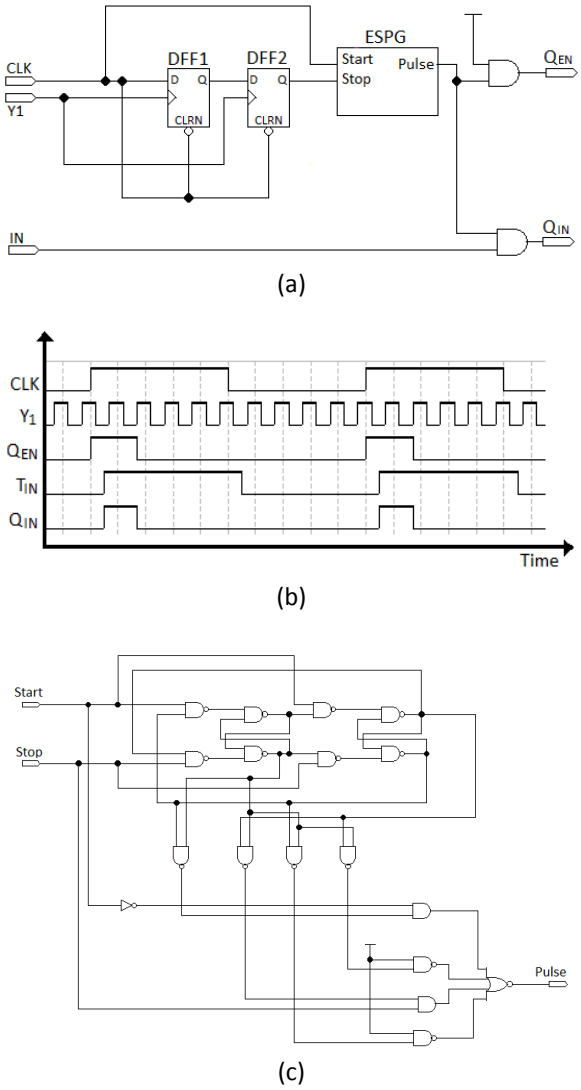


Fig. 9: Inter-stage synchronizer (IntS Sync), (a) block diagram, (b) timing diagram, (c) edge sensitive pulse generator (ESPG) implementation.

Results and Discussion

We implemented the prototype TDC on an Altera Stratix IV FPGA development board. Input pulses (T_{IN}) are applied to general purpose I/O (GPIO) port of FPGA board and digital output (D_{OUT}) is obtained from the same port. Regarding the I/O standard of Altera Stratix IV FPGA board, 3 V 1 MHz input pulses provided by a function generator (Siglent SDG 1050) are applied to the proposed TDC to attain the output spectrum. Then, a mixed-domain oscilloscope (Tektronix MDO 4104) with a Hann window captures 100-k samples. Finally, MATLAB is used for post-processing of samples. Fig. 10 illustrates the measurement setup for the prototype TDC. To demonstrate achieving second-order noise-shaping

dynamic test was induced to the proposed design and measured output spectrum at 100 MHz f_C and 200 MHz f_S is shown in Fig. 11(a). As can be seen, In spite of the fact that the proposed design employs only one counter for both stages, it achieves second-order noise-shaping appropriately and yields 57.5 dB SNR within 8 MHz bandwidth in this case. After the assurance of obtaining second-order noise-shaping we increase sampling clock to improve SNR.

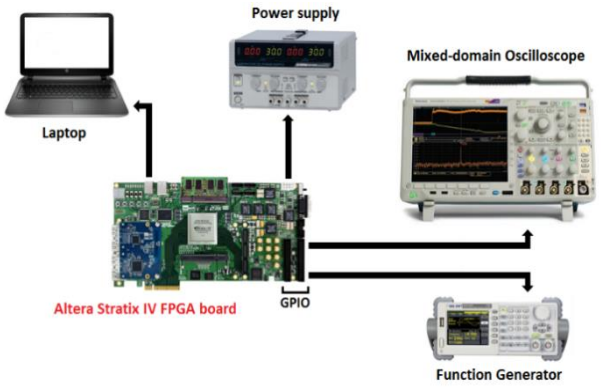
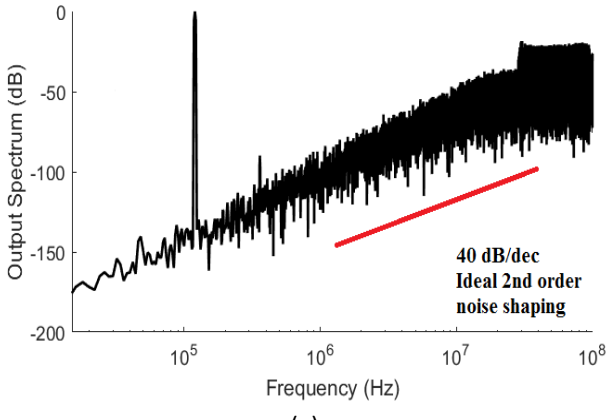
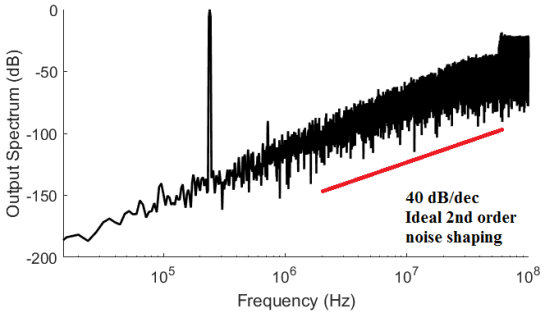


Fig. 10: The measurement setup for the prototype of the proposed TDC.

Fig. 11(b) shows the output spectrum of the proposed TDC at 100 MHz f_C and 400 MHz f_S. As expected, by 2 dB enhancement compared with previous case the measured SNR within 8 MHz bandwidth was 59.5 dB. Moreover, multiplication of f_C results in SNR enhancement even for the same OSR [19]. Thus, to investigate the effect of increasing f_C we examined the prototype of the proposed TDC at 200 MHz f_C and 400 MHz f_S. The measured output spectrum in this condition is shown in Fig. 11(c) which reveals 60.7 dB SNR (a gain of 1.2 dB) that translates to 9.79 effective number of bits (ENOB) and 0.28 ps time-resolution. From Fig. 11(b) and (c), it is clear that increasing f_C leads to SNR improvement even if OSR remains unchanged.



(a)



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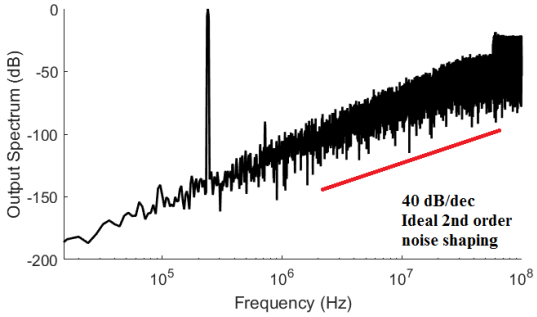

(c)

Fig. 11: Measured output spectrum of the second-order proposed TDC, (a) fS = 200 MHz and fC = 100 MHz, (b) fS = 400 MHz and fC = 100, (c) fS = 400 MHz and fC = 200.

The core of Altera Stratix IV FPGA board consumes 2.21 mW at 100 MHz f_C and 200 MHz f_S. Increasing the sampling frequency enhances time-resolution, SNR and FoM at the price of consuming 0.58 mW more power (2.79 mW core power consumption at 200 MHz f_C and 400 MHz f_S) owing to more switching of GSROs. Also, increasing f_C causes an excessive power consumption due to more ON time of GSROs.

Table 1: Performance summary and comparison with other state-of-the art ΔΣ TDCs

	[26]	[25]	[24]	[19]	[22]	**This work**	
Process (nm)	40	40	40	65	40 FPGA	**40 FPGA**	
Shaping order	4	3	3	2	2	**2**	
f_{BW} (MHz)	50.3	156	50.5	4	9.6	**8**	
T_{range} (ns)	N/A	N/A	N/A	4	4.5	**4.5**	
f_s (MHz)	1000	5000	3000	400	400 - 1600	**200**	**400**
DR (dB)	76.8	70	68.2	79.6	86.2	**84.4**	**85.6**
$T_{int,rms}$ ($f_{s,rms}$)[1]	N/A	N/A	N/A	148	78	**95.5**	**83**
SNR (dB)	75.8	66.6	68	N/A	61.02	**57.5**	**60.7**
Resolution (ps)[2]	N/A	N/A	N/A	0.51	0.27	**0.33**	**٠.٢٨**
Power (mW)	43	233	19	6.72	7.84[3]	**2.21[3]**	**2.79[3]**
FoM (dB)[4]	167	158	162	167	177	**179**	**180**

[1] Estimated integrated noise ($\sqrt{Resolution^2/12}$).

[2] Estimated resolution ($\sqrt{T_{int,rms}{}^2 . 12}$).

[3] FPGA core power consumption.

[4] FoM = DR + 10 $\log_{10}$ (Bandwidth / Power) [dB], where $DR = 20\ log_{10}(T_{range,rms}/T_{int,rms})$.

The performance summary of the proposed 1-1 MASH TDC and a comparison with the state-of-the-art ΔΣ TDCs has been presented in Table 1. Despite the fact that all previous continuous-time ΔΣ TDCs utilize one counter for each stage, the proposed novel structure exploits only one multi-bit counter for both stages and subsequently consists of less hardware. However, the proposed TDC incorporating less hardware not only does not show a degraded performance, but also it yields appropriate second-order noise-shaping with acceptable SNR and bandwidth while revealing least power consumption in the table by a dramatic difference in comparison with other works. Moreover, according to the Table 1 there are two points that should be considered. First, although the proposed design provides SNR less than higher order TDCs in [24]–[26]and close to the same order TDC in [22], but taking advantage of optimum all-digital designing and implementation on a high-performance FPGA board it represents superior power consumption and FoM over them. Second, this low amount of difference in SNR of this work and the state-of-the-art ΔΣ TDCs is promising that by modifying the proposed novel structure and adjusting it with more stages we can expect a high-order ΔΣ TDC that shows higher SNR, dynamic range and fine time-resolution without consuming a considerable power.

Conclusion

A ΔΣ GSRO-TDC with second-order noise-shaping has been introduced in this paper. We have proposed a novel structure to decrease implementing hardware and hence chip area and power consumption. In the proposed structure we employ only one multi-bit counter for both stages. Implementation of the proposed TDC prototype is performed on an Altera Stratix VI FPGA board and proved to be suitable for different applications such as ToF systems and ADPLLs. Although the main concentration of this work is on design optimization of a ΔΣ TDC to show less complexity, the measured results demonstrate that this work provides acceptable performance, say 60.7 dB SNR within 8MHz bandwidth at 400 MHz sampling frequency and 180 dB FoM while consuming 2.79 mW. Finally, it should be noted that by adjusting the proposed novel structure with more stages higher order of noise-shaping can be attained to enhance SNR and time-resolution further.

Author Contributions

A. Mouri Zadeh Khaki and E. Farshidi conceptualized the research. A. Mouri Zadeh Khaki designed the experiments and collected the data. A. Mouri Zadeh Khaki carried out the data analysis. E. Farshidi and K. Ansari Asl validated the results. A. Mouri Zadeh Khaki wrote the manuscript. E. Farshidi and K. Ansari Asl reviewed and edited the manuscript.

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Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

Abbreviations

TDC	Time to digital converter
SRO	Switched-ring oscillator
GSRO	Gated swithched-ring oscillator
FPGA	Field programmable gated array
ToF	Time-of-Flight
ADPLL	All digital phased-locked loop
SNR	Signal-to-Noise ratio
FoM	Figure of Merit
ESPG	Edge-sensitive pulse generator
QEgen	Quantization error pulse generator
ASIC	Application specific integrated circuits
SG	Source and ground
PulseGen	Pulse generator
MASH	Multi-stage noise-shaping
OSR	Oversampling ratio
ENOB	Effective number of bits
DR	Dynamic range
CLK	Clock
f_C	Input pulse frequency
f_S	Sampling clock frequency
f_{max}	Maximum frequency of GSRO
f_{min}	Minimum frequency of GSRO
Q_{IN}	Frequency sync pulse
Q_{EN}	Enable pulse of GSRO2
Y_1	Output pulse of GSRO1
Y_2	Output pulse of GSRO2
D_{OUT}	Digital output code
Y_M	Merged pulses of Y_1 and Y_2
DLY_2	Delayed Y_2
DCF	Digital cancellation filter
CNT_1	Counted number of rising edges of the first stage
CNT_2	Counted number of rising edges of the second stage
CNT_A	Aggregate counted number
CNT_{max}	Number of rising edges of Y_1 when GSRO operates at f_{max}

CNT_{min}	number of rising edges of Y_1 when GSRO operates at f_{min}
D_1	Digital output of the first stage
D_2	Digital output of the second stage
IntS Sync	Inter-stage synchronizer
GPIO	General purpose input/output

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