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Research paper

Low Delay Time All Optical NAND, XNOR and OR Logic Gates Based on 2D Photonic Crystal Structure

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Abstract

Background and Objectives: Recently, photonic crystals have been considered as the basic structures for the realization of various optical devices for high speed optical communication.
Methods: In this research, two dimensional photonic crystals are used for designing all optical logic gates. A photonic crystal structure with a triangular lattice is proposed for making NAND, XNOR, and OR optical logic gates. Using the structure as the intended logic gate is possible without the need to change the structure through the use of the phase difference at the inputs. Line and point defects have been used to propagate light from inputs to output. The logical values "0" and "1", are defined based on the amount of transferred optical power to the output.
Results: The simple structure and the use of line and point defects, instead of ring resonators, reduce the complexity of the design and its use in optical logic integrated circuits. Another advantage of proposed structure, in comparison to the previous structures is the reduction in delay time that increases its speed. The maximum delay time of the proposed optical NAND, XNOR, and OR gates is about 0.1ps.
Conclusion: In this study, one structure is suggested for realizing NAND, XNOR, and OR logic gates. This structure has a small size and low delay time, and is suitable for use in optical integrated circuits.

Introduction

So far, electronic logic gates based on transistors have been used to design logic circuits, which require advanced technology to increase their speed. To increase the speed of these circuits, the dimensions of the transistors must be reduced. Reducing the size of transistors also depends on the advancement of technology in the manufacture of electronic devices. Due to the excessive reduction of the dimensions of the transistors, it seems that further reduction will have many problems [1][2]. Photonic crystals are flexible structures and most circuits that ever designed in electronics can be implemented based on photonic crystals. Therefore, these structures can be used to design integrated optical circuits. Integrated optical circuits are the underlying of reaching high speed optical computers. You can also use a variety of materials and their combinations at different wavelengths to design them. The main challenge in using these structures is their manufacturing technology, which is not currently widely available. But researchers are optimistic that in the future they will be able to build these structures and in practice be able to move towards building optical integrated circuits. Using photonic crystals as a basic structure for designing analog and digital optical devices, has attracted many researchers to the optic areas [3]. Photonic crystals are alternating structures in which this alternation can occur in 1, 2, or 3 dimensions [4]-[5]. Two-dimensional (2D) photonic crystals are used extensively in designing optical devices due to their

flexibility. These structures alternate in two dimensions and are homogeneous in the third dimension. The alternating characteristic of the structure, makes it impossible for wavelengths of lights to propagate through the photonic crystal structure. This wavelength range is called the photonic band gap (PBG) and is a continuous range. This PBG can be obtained by band structure calculations [6]-[7]. In order to transfer light through specific paths, it is necessary to make changes to the paths and to eliminate their alternating characteristic. These changes are called defects. Defect paths transfer light waves from input sources to output routes. This characteristic is used to connect the inputs and the outputs of optical devices. Defects in photonic crystals can be in the form of line or point. These pathways are used as waveguides, because light waves can be directed in these directions [8][9]. Many attempts have been made to realize photonic crystal based logic gates. The design of AND, XOR, and OR logic gates are simpler than other gates. The design of NOR, NAND, and XNOR gates is more difficult due to the fact that when the input is "0", the output should be a logic "1". An additional input, called “the bias”, is also required. In fact, the bias input is an additional source that is used to generate power at the output, when the main inputs are zero (based on the accuracy table) [10][17]. With regard to the design of the NAND and the XNOR optical logic gates, some work has been performed; in most of this work, a ring resonator has been used. This has caused an increase in the size of the circuit and the coupling light in them increases the delay-time and reduces the speed of the gates. The increase in the size of a structure is an important issue. Its reduction and its simplicity make the use of the circuit in integrated optical circuits possible [18]-[36]. In reference 15, a NAND gate is designed using photonic crystals. Although a square lattice is used in this gate, but in the proposed structure, a ring resonator is used, which reduces the speed of the gate. Also, the dimensions of the structure have been slightly enlarged due to the use of resonators. Reference 21 presents a structure for designing an OR gate based on photonic crystals. This structure is designed only for one gate and the use of three resonator rings in this structure has increased the size of the circuit and also reduced the gate speed. Also in this gate, inputs and outputs are considered on one side of the structure, which will be problematic for use in integrated optical circuits. In reference 28, a NAND gate is designed based on a photonic crystal. In this structure, a square lattice is used. The use of two ring resonators increases the size of the circuit and also increases the gate delay. Also, the large displacement of dielectric rods in this structure will make it difficult to build.

In reference 29, a NAND gate is designed that photonic crystal with a square lattice has been used. In this structure, a ring resonator is used, which increases the delay and thus reduces the gate speed. Also in this gate, the output in logic "0" state has a high optical power and the distance between two logic values is close to each other. A small distance between two logical values increases the bit detection error at the output. In addition, the size of the structure is relatively large. In reference 30, the NAND and XNOR gates are designed using photonic crystals. In this structure, because line defects are used and the structure does not have a ring resonator, it has a good speed. But because the length of this structure is a little long, the delay has been slightly increased. Also the size of the circuit is also relatively large. One of the other problems that are seen in most optical logic gates is the proximity of optical power to the two logic states. In other words, optical power is high at a logic "0" and low at a logic "1", and this can increase the probability of error in the output. Therefore, a criterion for the evaluation of the function of the logic gates is this difference. In this study, one structure is suggested for realizing three logic gates (NAND, XNOR, and OR). For using this structure as the intended gate, a phase difference is created. One of the input ports is used as the bias input. When the inputs are equal to zero, this input supplies power to the output and keeps it at a logic "1" (used in the NAND and XNOR gates). Plane Wave Expansion (PWE) method is used to analyze the band structure and calculate PBG, and Finite Difference Time Domain (FDTD) method is used for time calculations of light wave propagation from waveguide paths. In the design of the logic gates, increasing the output power at the "1" state and reducing it at the "0" state is emphasized. Furthermore, the simplicity of this structure and making use of simple defects is another characteristic of these gates which makes it possible to use them in integrated optical circuits. In addition, not using ring resonators in the design reduces the delay-time significantly in a manner which leads to the formation of high-speed gates. The method of presentation in this study is that after the introduction, the NAND, XNOR, and OR logic gates are briefly introduced. The initial structure for realizing these optical logic gates are presented in the next section. After this section, the realization of the NAND, XNOR, and OR optical logic gates are presented (in three sub-sections separately). Finally, conclusion is presented.

Introduction to NAND, XNOR, and OR Logic Gates

NAND, XNOR, and OR logic gates have two inputs and an output. According to the logical values of the inputs, the output of the gates is determined. Figure 1 shows the circuit symbol of these logic gates. The logic value of the outputs of the logic gates are shown in Table 1. The

presented tables are known as accuracy tables.

According to Table 1, the output of the NAND gate is a "1" when at least one of the inputs is a "0". The XNOR logic gate has an output of "1" when the inputs are equal. Finally, the output of the OR logic gate is a "1" when at least one of the inputs is a "1".

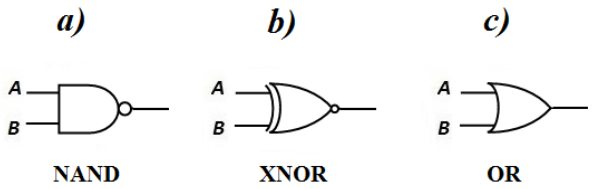

Fig. 1: Circuit schematic for the logic gates in a) NAND, b) XNOR, and c) OR

Table 1: Accuracy table of logic gates in Figure 1

INPUT A	B	NAND Gate	XNOR Gate	OR Gate
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	1	1

Initial Structure for Realizing Logic Gates

In order to obtain the intended logic gates, first, a two dimensional photonic crystal structure is considered. This structure includes a hexagonal lattice with dielectric rods in the air. The refractive index of the rods is 3 (n=3); these rods are placed next to one another in two dimensions and the background material is assumed to be air. In photonic crystals, the working wavelength should be in the PBG range. The PBG range is also a continuous range. That is, a photonic crystal structure can be used in a range of wavelengths. Also, in addition to the material of the rods, the PBG range depends on the material of the substrate as well as the lattice constant of the structure. Therefore, if the refractive index of the material changes slightly, the working wavelength can be adjusted by changing the lattice constant. $Ga_xIn_{1-x}P$ can be used as a material with a refractive index of 3 in the considered wavelength.

The lattice constant in this structure is a=0.64µm and the radius of the rods is selected to be r=0.18a. The number of rods is considered to be 19×19. That is, the number of rods that are placed next to each other in the air background, includes 19 cylindrical rods in the x direction and 19 rods in the y direction.

Figure 2 shows the structure of the original photonic crystal without defects. This structure is used to calculate the band structure. This structure creates a PBG, which does not allow the wavelength of this band to pass through the structure.

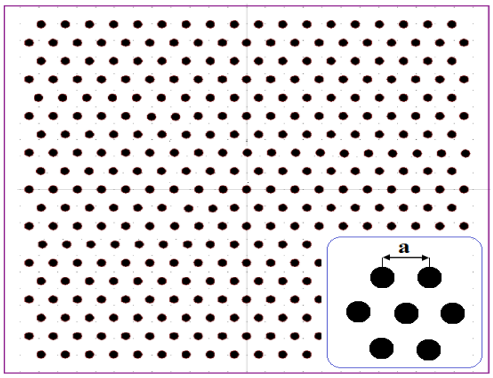

Fig. 2: Photonic crystal structure

For obtaining not-transmittable wavelengths in the structure, band structure calculations are used.

For this purpose, RSOFT software, which is very suitable software for simulating photonic crystal structures, has been used. This software greatly reduces time calculations.

The results of the band structure are shown in Fig. 3. The proposed structure creates a PBG for TM mode. Therefore, the band structure simulation is calculated for this mode.

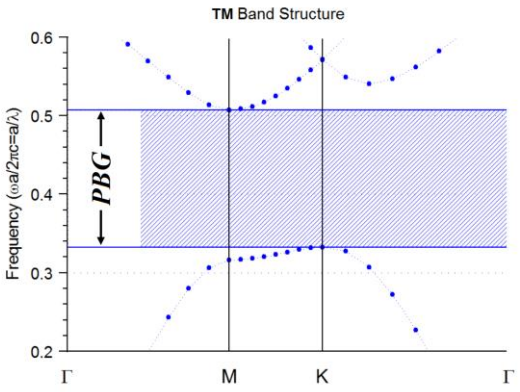

Fig. 3: Band structure of the proposed structure.

Figure 3 shows the PBG range for the intended structure by using band structure calculations. As observable in the normalized wavelength $(\frac{a}{\lambda})$ interval, in the range between 0.33 and 0.51, light is not transmittable in the structure, and these wavelengths are reflected on hitting the structure. The wavelength equivalent with this interval falls in the range from 1.25µm to 1.94µm.

At other wavelengths, light is transmitted in the structure, and cannot be guided in the intended paths of the structure. Hence, in order to transfer light in specific paths in the structure, light-source wavelengths should be in the PBG range. Here, the wavelength considered for the light source is 1.55µm, that is in the PBG range. This wavelength is the third communications window.

Realizing the NAND, XNOR, and OR Optical Gates

In order to create optical gates using the proposed structure, three input paths and one output path have been provisioned. The paths for the passage of light is created by using line and point defects in such a way that all the three paths intersect in one location. Point defects are used at the intersection of the three paths. Point defects include four defects that are a result of the change in the rod radius.

The radius of the three rods a, b, and c are halved and the radius of rod d is multiplied by 1.2. This structure is used for the three NAND, XNOR, and OR optical gates. Line and point defects are shown in Fig. 5, 6 and 7.

When the structure is used as NAND and XNOR gates, one of the input ports is chosen as the bias for supplying power to the outputs when the inputs are "0". To use the proposed structure as an OR gate, two ports are used as input and the third port is not used.

To achieve the desired outputs according to the accuracy table, and the interaction of the waves propagated in the input paths, phase difference has been used for some inputs and bias input relative to each other.

A. Nand optical logic gate

In order to use, the proposed structure as a NAND optical gate, A and B inputs, and the bias source are selected as shown in Fig. 4a. Input B has a phase difference of 110° and the bias source has a phase difference of 75° with respect to input A.

The results of the simulation of the NAND optical gate are shown in Fig. 4b. This diagram shows the normalized output optical power. The results show that under the condition A=B=0, the output is equal to 0.83. This power is supplied by the bias source.

When A=0 and B=1, the optical output power is 0.85; when A=1 and B=0, the output is 0.88.

The phase differences and the point defects are selected in such a way that when the output is in the "1" logic state, the light waves come together at the defects in such a way that they interfere with the bias source and the value of output power is similar in all the three cases. In these three cases, considering that the outputs are high, they can be considered a logic "1". When the inputs A=B=1, the power transmitted to the output is very low (about 0.12), which can be considered a logic "0". In the optical gate described, the interval between the two logic states of "0" and "1" is 0.71. This difference reduces the error in determining a high or a low logic level at the output. Furthermore, Figure 4b shows that the delay time in output response to the input is approximately 0.1ps. Considering the fluctuations in the output when the inputs become active, the time required for the output to become stable is about 0.4ps. One of the reasons for the reduction of delay time relative to previous works is the small size of the structures and the nonuse of the ring resonators.

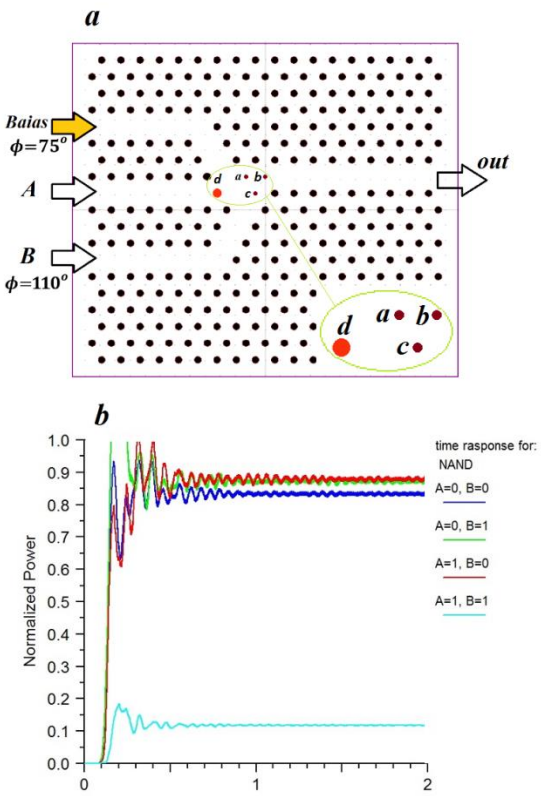

Fig. 4: a) Optical NAND structure and b) Normalized output power.

B. XNOR Optical Logic Gate

Using the suggested structure as an XNOR optical gate is possible without changing the structure and only through the change of phase difference in the inputs. To achieve this, the phase difference of the bias source with respect to the two main inputs A and B is considered to be 65°. Fig. 5a shows the placement of the inputs and the bias source for use as an XNOR optical logic gate. Fig. 5b shows the normalized output power for various inputs to the optical XNOR gate. According to the figure, the output is high (a logic "1") when the inputs A and B are equal; when the inputs are not equal, however, the output has little power (a logic "0"). This is similar to the XNOR gate. The results of the simulation show that the normalized output power is about 0.61, when the inputs A=B=0. This amount of optical power is equivalent to logic "1". Also, the output power is about 0.64 (a logic "1") when A=B=1.

The output power, when A=0 and B=1, and A=1 and B=0 are 0.06 and 0.12, respectively which are equivalent to logic "0". Considering these values, the interval between the two logic states of "0" and "1" is 0.49. In the XNOR optical gate, the input bias is active, and when the inputs are off, it supplies power to the output.

When both inputs are on, the paths taken by the light waves from the sources and the phase difference of the bias source are chosen such that the point defects and the light interferences cause the power transferred to the output to be equal to the "1" logic state.

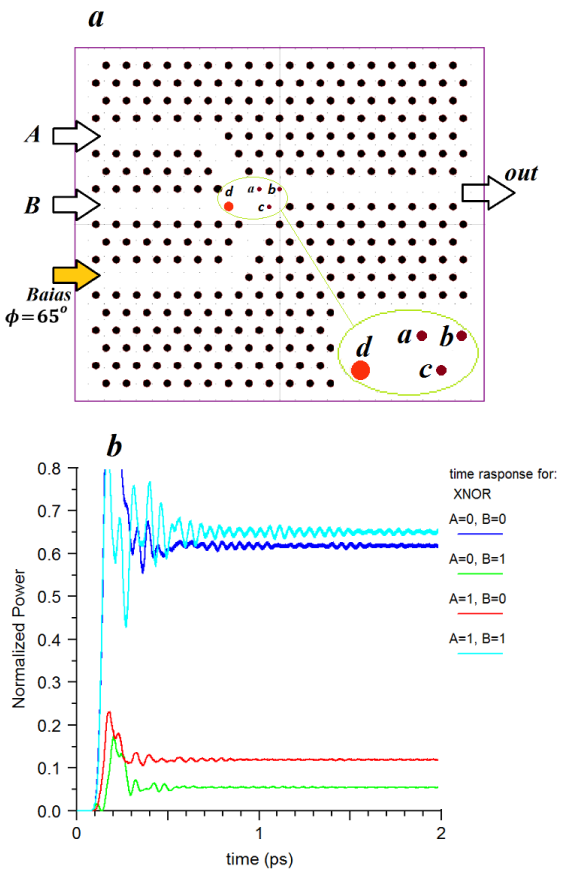

Fig. 5: a) Optical XNOR structure and b) Normalized output power.

When the inputs are not equal, the interference between the active input and the bias source is such that the transmission output power in both cases is low.

The time required for the output responding to the input source is almost 0.1ps, and the time required for the output to become stable is about 0.3ps. This low delay time, as well as the small size of the proposed structure, makes this optical gate suitable for use in high speed optical integrated circuits.

C. OR Optical Logic Gate

The proposed structure can also be used as an OR gate as well. For access this gate, two sources are selected for the inputs and there is no need for a bias source. Considering the results obtained from the optical NAND gate, if the phases of the upper and the lower sources (as shown in Figure 6a) are selected to be 75° and 110°, respectively, the structure functions as an OR gate. The selection of the inputs A and B is shown in Figure 6a. It is clear that, if both inputs are turned off, the power emitted to the output is zero. The output powers for the other three cases are shown in Figure 6b. These values are calculated and found to be normalized.

The diagram obtained shows that in the condition that one of the inputs is switched on, the power emitted to the output is considerable (a logic "1"). For the condition in which A=0 and B=1, the value of normalized power at the output is 0.61, whereas in the condition A=1 and B=0, the value is equal to 0.83. When A=B=1, the normalized power at the output is 0.85. Considering that the output power at a logic "0" is equal to zero and the least power at a logic "1" is 0.61, the output power interval is 0.61 in the worst case.

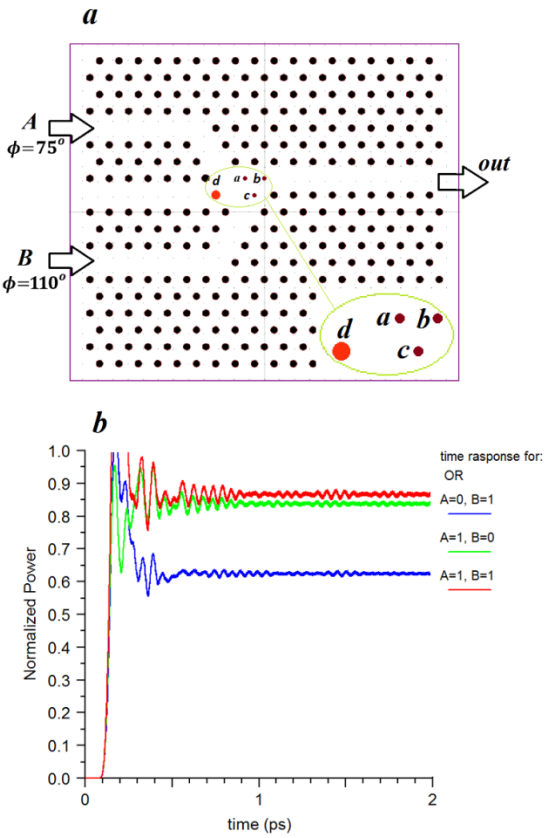

Fig. 6: a) Optical OR structure and b) Normalized output power.

The time diagram shows that the delay time of the optical gate is about 0.1ps and the time required for the output to become stable is about 0.4ps.

Comparing the three optical logic gates (NAND, XNOR, and OR) shows that the time required for the output to become stable in the XNOR gate is about 0.3ps and in the NAND and the OR gates, the time is about 0.4ps. Considering that this time is very short, the suggested optical gates can be used as high-speed optical gates.

Table 2 shows the simulation results for all three logic gates, NAND, XNOR and OR. This table shows the values of the normalized output power for each gate, as well as its equivalent value.

According to Table 2, it is clear, that the output power of each gate is low in the "0" logic state. Also in "1" logic

state, the power is high. These values indicate that the designed gates have a reasonable logical distance and the detection error at the output will be reduced.

The detection error at the output depends on the distance between the two logic values "0" and "1". The smaller distance between the two logic values"0" and "1", will cause the correct detection for the logical values at the output. In this case, the error detection for bits will be reduced.

Table 2: Normalized output optical power for NAND, XNOR, and OR optical logic gates

INPUT		NAND	XNOR	OR
A	B	Output (logic)	Output (logic)	Output (logic)
0	0	0.83 (1)	0.61 (1)	0.00 (0)
0	1	0.88 (1)	0.06 (0)	0.61 (1)
1	0	0.88 (1)	0.12 (0)	0.83 (1)
1	1	0.12 (0)	0.64 (1)	0.85 (1)

The value of Contrast Ratio (CR), which represents the distance between the two logical values "1" and "0", is calculated as the relation CR= 10log(P_1/P_0). Where P_1 and P_0 are the power transmissions to the output in the "1" and "0" logic state, respectively. According to Table 2, this value is equal to CR= 8.4dB for NAND gate and CR= 7.1dB for XNOR gate. Also for the OR gate, since the amount of power in the "0" logic state is zero, the value will be high, for all OR structures.

Due to the fact, that the output of the "NAND" and "XNOR" gates, for zero inputs must be "1", the design of this gate is more difficult than other gates and requires an additional input. Therefore, the design of these gates is usually accompanied by an increase in size. In this paper, a simple structure with small dimensions is used to design these gates.

The results obtained for the NAND, XNOR and OR logic gates are shown in Fig. 4-6. Diagrams b in these figures show the normalized transfer power at the output. These figures show that the designed logic gates have high output power in "1" logic state and low power in "0" logic state. Therefore, it can be said that in this structure, the bit detection error in the output is reduced. Also, due to the low delay in light emission from input to output, the designed gates have a high speed and can be used in high speed optical circuits. To study the effect of wavelength changes, the above structures can be simulated for different wavelengths. However, since the desirable structure for all three gates has the same paths, one of the modes when the structure is used as an OR gate is re-simulated for 1.5um and 1.6um wavelengths and the results obtained are shown in Fig. 7 and 8.

Figure 7 shows the transmission power at the output of the OR gate for the 1.5µm wavelength.

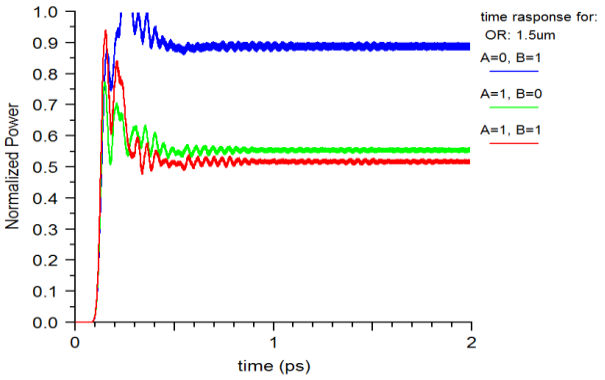

Fig. 7: Normalized output power for OR gate at $\lambda = 1.5\mu m$.

As it is shown in Fig. 7, in cases where the output is in the "1" logic state, one of the outputs is slightly increased but the other two outputs are greatly reduced so that the normalized value is approximately 0.5 and this value is low for logical "1" state.

Now the same OR gate structure is simulated for the 1.6µm wavelength and the normalized power results at the output are shown in Figure 8.

According to Figure 8, it can be seen that the amount of output power for input A=1, B=0 has not changed much and the output power for input A=B=1 has increased significantly. But in the case of A=0, B=1, the amount of output power is reduced to about 0.4 normalized, and this value is very small for logical "1" state. On the other hand, in a logic gate, the proximity of the logic "1" values in different modes is an advantage, because bit detection sensors for different logic "1" values may cause problem.

It should be noted that the proposed NAND and XNOR gates have less losses in this wave length and have better performance considering that designed to propagate light at a wavelength of 1.55µm.

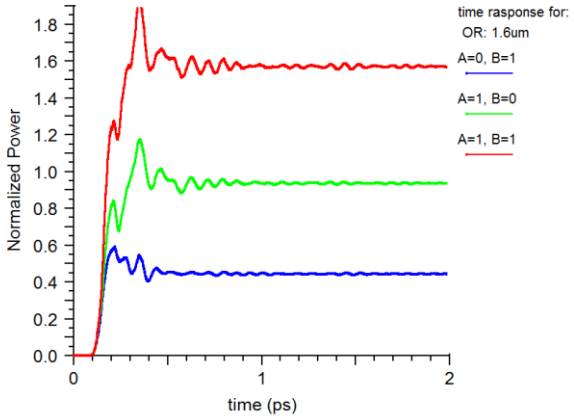

Fig. 8: Normalized output power for OR gate at $\lambda = 1.6\mu m$.

Results and Discussion

In this paper, one structure is suggested for realizing three logic gates. To compare the proposed gates with

the recently designed gates, Table 3 is given. Table 3 shows the simulation results for the designed gates, for the output parameters. These parameters are: structure size (number of rods in horizontal and vertical directions), delay time (the time when the input effect appears on the output) and Contrast Ratio. Table 3 shows that the proposed structure has a smaller size than other references, and therefore, is expected to have less delay time. The CR parameter is also increased. The reason for increasing CR in the proposed structure is the large output power distance for the two logic values.

Table 3: Comparison table of the proposed gate with a number of similar references

Reference	Gates	Size (Number of Rods)	t_{delay}	CR(dB)
[21]	OR	24×31	-	7.27
[29]	NOR	37×27	-	3.5
	NAND			3.4
[34]	XNOR	46×45	0.5ps	6.3
	NAND			3.74
[35]	XNOR	20×41	-	7.2
	NAND			7.4
This work	XNOR	19×19	0.1ps	7.1
	NAND			8.4

Conclusion

In this research, a fixed photonic crystal structure with small dimensions is used as the three optical logic gates. Values of output optical power are determined based on the interference of light waves in the defect paths created. The "0" and "1" logical values are defined based on the value of optical power. The results show that the logic gates have an output power close to zero at a logic "0" and close to the input power source at a logic "1". The difference between a "0" and a "1" is relatively large, which is considered one of the advantages of these gates. Furthermore, considering the short delay time of this structure, the designed gates have high speed.

Author Contributions

M.R. Malmir designed and simulated and carried out the data analysis, and F. Parandin collected the data and interpreted the results and wrote the manuscript.

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Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

Abbreviations

There is no abbreviation.

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