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Research paper

# A Novel Method Design Multiplexer Quaternary with CNTFET

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**Abstract**

**Background and Objectives:** In recent decades, due to the effect of the short channel, the use of CMOS transistors in the nanoscale has become a major concern. One option to deal with this issue is the use of nano-transistors.

**Methods:** Using nano-transistors and multi-valued logic (MVL) can reduce the level of chips and connections and have a direct impact on power consumption. The present study reports the design of a new method of Multiplexers (MUXs) based on quaternary logic and transistors of carbon nanotubes (CNTFET) and having a new look at the layout and use of MUXs.

**Results:** The use of special rotary functions and unary operators in Quaternary logic in the design of MUXs reduced the number of CNTFETs from 27% to 54%. Also, the use of MUXs in the Adder structure resulted in a 54% reduction in Power Delay Product (PDP) and a 17.5% to 85.6% reduction in CNTFET counts.

**Conclusion:** The simulated results display a significant improvement in the fabrication of Adders, average power consumption, speed, and PDP compared to the current best-performing techniques in the literature. The proposed operators and circuits were evaluated under various operating conditions. The results show the stability of the proposed circuits.



## Introduction

Advances in science and technology have considerably increased human need for information, rapid processing, and storage. As a result, scientists face the challenge of fabricating compact integrated circuits that can simultaneously reduce energy consumption and boost the speed of systems. With the advent of complementary metal-oxide-semiconductor (CMOS) technology, technological advancements provided CMOS transistors with further challenges such as short channel effects, leakage current, increased power consumption, and high sensitivity to orbital parameters, which incentivize scientists to take advantage of new technologies at the nanoscale [1], [2]. The remarkable similarity between carbon Nanotube field transistors (CNTFETs) and Metal Oxide Semiconductor Field Effect Transistor (MOSFETs) has been the subject of intense research. CNTFETs enjoy high carrier mobility, low power consumption, lower latency, and smaller intrinsic capacitors, resulting in the acceleration of these elements. Due to the identical mobility of electrons and holes, P and N types of these transistors are similar in terms of channel length. One of the unique features of CNTFETs is the variation of the threshold voltage caused by changing the channel length [3]. Using these transistors along with multi-value logic (MVL) has thus greatly reduced the volume of integrated circuits. MVL circuits do not share common problems of binary circuits such as the high number of connections and higher power consumption [4]. Accordingly, they reduce the intricacy of the circuits and chip surface and allow implementing the rational and mathematical functions

at a higher rate and fewer computations [5]. Multi-valued logic is divided into Ternary, Quaternary, and Pentanary groups, with the Ternary having been more extensively researched than the other two. Among the highest and the lowest levels in MVL circuits, Quaternary logic can be the right option in designing microprocessors. Different circuits have been designed using CNTFETs and MVL logic. Ternary and quaternary circuits work directly with ternary and quaternary logic [6], [7]. The circuits work by converting Ternary and Quaternary to binary and vice versa [8], [9], and by MUXs [10], [11]. Because most computational operations are performed by adding an operator, in this study, different adder blocks were designed using MUXs and circuits with quaternary logic. New insights into MUXs and circuits dramatically reduced the number of transistors, average power consumption, propagation delay, and PDP compared with previous results [6], [12]-[16]. The remainder of the paper is organized as follows. Next Section describes the basic principle. Next Section includes the proposed circuit design. Next Section presents the simulated results and comparison. Finally, Section presents the conclusions.

## Principles

### *A. Carbon Nano Tube Field Effect Transistor (CNTFET)*

Nanotubes are graphite plates with a tubular form and hexagonal structure. The nanotube plates can be conductive or semiconductor depending on their rotational axis. Carbon nanotubes are composed of tubular graphite plates that are based on the chirality vector C= $m\alpha_1 + m\alpha_2$, where $\alpha_1$ and $\alpha_2$ are the unit vectors of the graphite plate and the chirality (m, n) determines how the CNTs twist. SWCNTs can be conductors or semiconductors. If m and n are equal (m = n) or their product is a multiple of 3 (m·n = 3i), then the nanotube will exhibit metal conductivity. Otherwise, the produced nanotube will exhibit a semi-conductive property [17]. Fig. 1 shows the structure of the CNTFET structure. The appropriate threshold voltage for CNTFETs can be obtained using an appropriate CNT diameter. The CNTFET threshold voltage is inversely related to the nanotube diameter as follows [12].

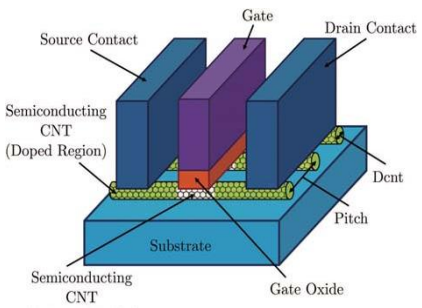


Fig. 1: The structure of the CNTFET.

$$V_{th} \approx \frac{E_g}{2.e} = \frac{\sqrt{3}}{3}\frac{a.V_\pi}{e.DCNT} \approx \frac{0.43}{DCNT(nm)} \quad (1)$$

$$DCNT = \frac{a.\sqrt{m^2+n^2+m.n}}{\pi} = 0.078\sqrt{m^2+n^2+m.n} \quad (2)$$

where α is the distance between two adjacent carbon atoms ($a \cong 0.248$), Vπ is the bond energy between the two carbon atoms (Vπ = 0.033), e is the unit electron charge, and DCNT is the diameter of the carbon nanotube. Therefore, using a CNTFET transistor with appropriate nanotube diameters, different threshold voltages, which are the basis for evaluating various logical levels, can be created. The relations between chirality, CNT diameter, and threshold voltage are shown in Table 1.

Table 1: The relations between chirality, CNT diameter, and threshold voltage

| (n, m) | Diameter (CNTs) | Threshold voltage (N-NTFET) | Threshold voltage (P-CNTFET) |
|---|---|---|---|
| (19,0) | 1.487 nm | 0.289 V | -0.289 V |
| (17.0) | 1.330 nm | 0.328 V | -0.328 V |
| (16,0) | 1.253 nm | 0.348 V | -0.348 V |
| (14,0) | 1.100 nm | 0.398 V | -0.398 V |
| (13,0) | 1.018 nm | 0.428 V | -0.428 V |
| (11,0) | 0.861 nm | 0.506 V | -0.506 V |
| (10,0) | 0.783 nm | 0.559 V | -0.559 V |

### *B. Quaternary Logic*

The Quaternary logic consists of four voltage levels, as shown in Table 2 [18]. Logical functions are also introduced based on quaternary logic such as QNAND, QNOR, QNOT, and other special functions [12], [14].

Table 2: Corresponding voltages with logic values

| Scale | Logic | Voltage(v) |
|---|---|---|
| GND | '0' | 0 |
| Vdd/3 | '1' | 0.3 |
| 2Vdd/3 | '2' | 0.6 |
| Vdd | '3' | 0.9 |

Multi-value functions have various functions due to the type of particular attitude assigned to them; e.g. the inverter has several functions such as Intermediate Quaternary Invert (IQI), Negative Quaternary Invert (NQI), Positive Quaternary Invert (PQI), and Standard Quaternary Standard Invert (SQI) [5], [18].

$$QNOT(a) = 3 - a \quad (3)$$

$$QNAND(a,b) = \overline{MIN(a,b)} = \begin{cases} 3-a & if \quad a \le b \\ 3-b & otherwise \end{cases} \quad (4)$$

$$QNOR(a,b) = \overline{MAX(a,b)} = \begin{cases} 3-a & if \quad a \ge b \\ 3-b & otherwise \end{cases} \quad (5)$$

The accuracy table of inverter functions is presented in Table 3.

Table 3: The truth table of quaternary inverter

| IN | NQI | PQI | IQI | SQI |
|---|---|---|---|---|
| 0 | 3 | 3 | 3 | 3 |
| 1 | 0 | 3 | 3 | 2 |
| 2 | 0 | 3 | 0 | 1 |
| 3 | 0 | 0 | 0 | 0 |

Equation (3) equal to the SQI function, which its accuracy is shown in Table 3.

### *C. Efficient CNTFET-based circuits for unary operators*

In the design of multiplexer-based circuits, special functions and Unary functions are used. These functions are shown in Table 4 and the sample circuits that include these functions are shown in Fig. 2.

AP is equivalent to PQI function, AN is equivalent to NQI function, and AI is equivalent to IQI function. Different circuit operators are defined according to design requirements in this paper [8], [14], [17]. Here, A1, A2, and A3 are rotational quaternary logic operators that represent the beginning of function with the level according to their index. For example, operator A1 starts at level 1 and A2 begins at level 2.

These operators were constructed by varying the voltage levels of the chirality vector according to the status of A and its dependent operators. Fig. 2 illustrates this procedure. MUX 4*1 was applied to construct operators A1, A2, and A3. The voltage levels L1 (0.3v) and L2 (0.6v) were generated by the voltage divider. In Fig. 2 (g), operators S1 and S2 are used to control multiplexer outputs.

For example, in operator A1, when A goes through its corresponding levels 0, 1, 2, and 3, respectively, voltage levels (A) of transistors T4, T5, T6, and T7 are switched on, while levels 1, 2, 3, and 0 are switched on as its output. This is also the case for operators A2 and A3, which produce different levels of output proportional to the input A [14].

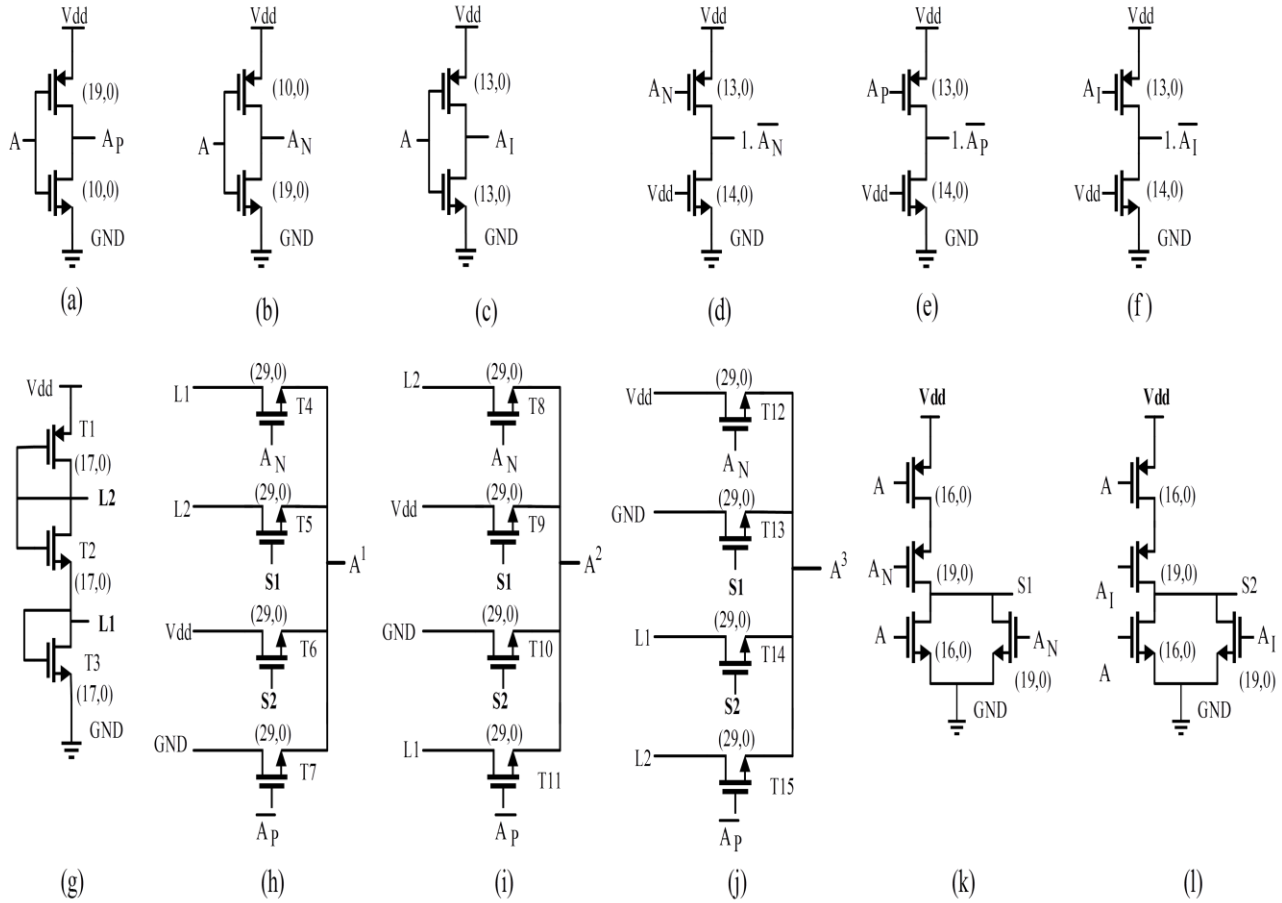


Fig. 2: CNTFET circuits for unary operators: (a) $A_P$ (b) $A_N$ (c) $A_I$ (d) $1.\overline{A_N}$ (e) $1.\overline{A_P}$ (f) $1.\overline{A_I}$ (g) voltage divider (h) $A^1$ (i) $A^2$ (j) $A^3$ (k) S1 (l) S2.

Table 4: Truth table of unary operator

| $A$ | $A_P$ | $A_N$ | $A_I$ | $A^1$ | $A^2$ | $A^3$ | $1.\overline{A_P}$ | $1.\overline{A_N}$ | $1.\overline{A_I}$ | $S1$ | $S2$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 3 | 3 | 3 | 1 | 2 | 3 | 0 | 0 | 0 | 0 | 0 |
| 1 | 3 | 0 | 3 | 2 | 3 | 0 | 0 | 1 | 0 | 3 | 0 |
| 2 | 3 | 0 | 0 | 3 | 0 | 1 | 0 | 1 | 1 | 0 | 3 |
| 3 | 0 | 0 | 0 | 0 | 1 | 2 | 1 | 1 | 1 | 0 | 0 |

## Proposed Circuits

Normally, multiplexers are circuits that connect multiple information inputs to an output according to different choices. In this section, we propose different models of MUXs (i.e., 8*4, and 12*4), depending on their application in the adder circuit.

### *A. Proposed Quaternary Multiplexer*

One of the most common methods of designing multiplexers is shown in Fig. 3. In this method, according to the voltage levels of the selector signal, one of the inputs is connected to the output. In the above circuit, in addition to the selector signal B, the input signal has also quaternary values. In this case, if B = 0, 1, 2, and 3, the inputs D1, D2, D3, and D4 are transferred to the output, respectively. In this design, the signal B1 has an output when the voltage level of the signal B has reached 1 logic (0.3 v) and the output of the signal B2 is activated in B = 2. A total of 30 CNTFETs are used in the Multiplexer shown in Fig. 3.

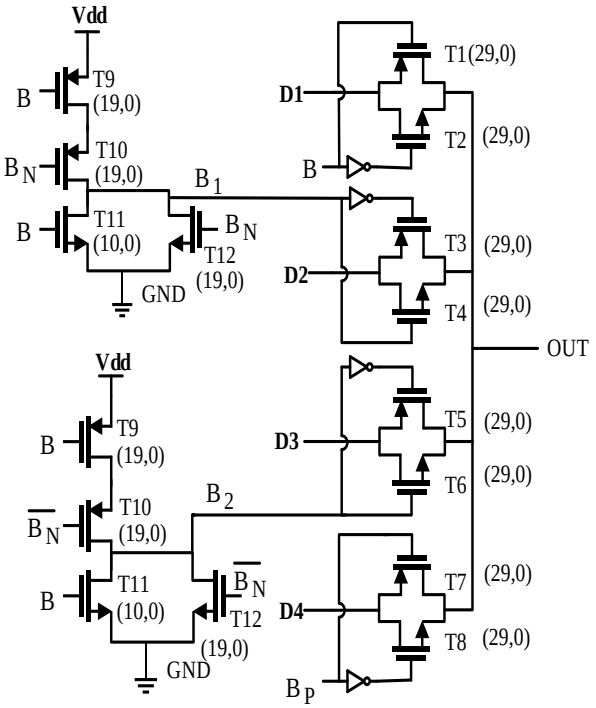


Fig. 3: Structure of MUX 4*1 using the proposed design.

One of the applications of these multiplexers is in the design of Adder circuits.

Table 5 shows the accuracy of a half adder and Fig. 4 shows the application of a MUX 4*1 in the construction of a half adder.

Table 5: The truth table for quaternary half adder [13]

| | Product | | | | | | Carry | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | | | | | A | | | | | | |
| B | 0 | 1 | 2 | 3 | | B | 0 | 1 | 2 | 3 | | |
| 0 | 0 | 1 | 2 | 3 | A | | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 2 | 3 | 0 | $A^1$ | | 1 | 0 | 0 | 0 | 1 | $1.\overline{A_P}$ |
| 2 | 2 | 3 | 0 | 1 | $A^2$ | | 2 | 0 | 0 | 1 | 1 | $1.\overline{A_I}$ |
| 3 | 3 | 0 | 1 | 2 | $A^3$ | | 3 | 0 | 1 | 1 | 1 | $1.\overline{A_N}$ |

According to Table 5, the value of sum and carry are obtained as:

$$\begin{aligned} Sum &= B_0(A_0 + A_1 + A_2 + A_3) + B_1(A_1 + A_2 + A_3 + A_0) \\ &+ B_2(A_2 + A_3 + A_0 + A_1) + B_3(A_3 + A_2 + A_1 + A_0) \end{aligned}$$

$$\begin{aligned} Carry &= B_0(0) + B_1(1.A_3) + B_2((1.A_2) + (1.A_3)) \\ &+ B_3((1.A_1) + (1.A_2) + (1.A_3)) \end{aligned} \quad (6)$$

where $A_0$, $A_1$, $A_2$, and $A_3$ are equal to levels A = 0, 1, 2, and 3, respectively. This also applies to B and its various levels. The sum and carry are rewritten as relationships in (7).

$$Sum = B_0(A) + B_1(A^1) + B_2(A^2) + B_3(A^3)$$

$$Carry = B_0(0) + B_1(1.\overline{A_P}) + B_2(1.\overline{A_I}) + B_3(1.\overline{A_N}) \quad (7)$$

Based on (7), it is possible to design Sum and Carry using two MUX 4*1. This can be seen in Fig. 4. In this combination.

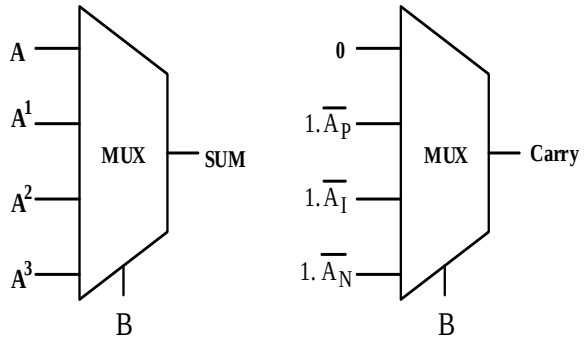


Fig. 4:. Proposed Design QHA.

B acts as a selector in MUX units. Also, by selecting one of the B levels in the Sum operator, one of the inputs A, $A^1$, $A^2$, and $A^3$ is considered as output. Moreover, in the Carry operator, B is selected among the operators $1.\overline{A_P}$ , $1.\overline{A_I}$ , $1.\overline{A_N}$ and 0 is the output.

Two half adders can be used to design the full adder. The full adder block consists of two inputs A and B, one input carry (Cin), and two outputs including Sum and output carry (Cout). According to Table 5, the maximum carry produced is 0 and 1, so Cin can be a maximum of 1. Table 6 shows the accuracy of the performance of a full adder and Fig. 5 presents its structure with the basic blocks of MUX 4*1. Fig. 5 presents a full adder block for each output Sum and Carry, including two blocks MUX 4*1 and one block MUX 2*1. The structure of the first full adder proposed in this article is shown in Fig. 6. Selector signals C and B are shifted together at the beginning and end of the adder block. Each Sum and Carry output consists of 8*4 and 4*1 MUXs, of which the MUX 4*1s is less used than the base full adder mode. In the MUX 8*4 structure, Cin is used as the selector, for example, by selecting C = 0, operator A, $A^1$, $A^2$, and $A^3$ are transferred to the outputs while selecting C=1, operators $A^1$, $A^2$, $A^3$, and A are transferred to the outputs.

Table 6: The truth table of a proposed quaternary full adder with unary

| Cin | B | A | Sum | Cout |
|---|---|---|---|---|
| 0 | 0 | A | A | 0 |
| 0 | 1 | A | $A^1$ | $1.\overline{A_P}$ |
| 0 | 2 | A | $A^2$ | $1.\overline{A_I}$ |
| 0 | 3 | A | $A^3$ | $1.\overline{A_N}$ |
| 1 | 0 | A | $A^1$ | $1.\overline{A_P}$ |
| 1 | 1 | A | $A^2$ | $1.\overline{A_I}$ |
| 1 | 2 | A | $A^3$ | $1.\overline{A_N}$ |
| 1 | 3 | A | A | 1 |

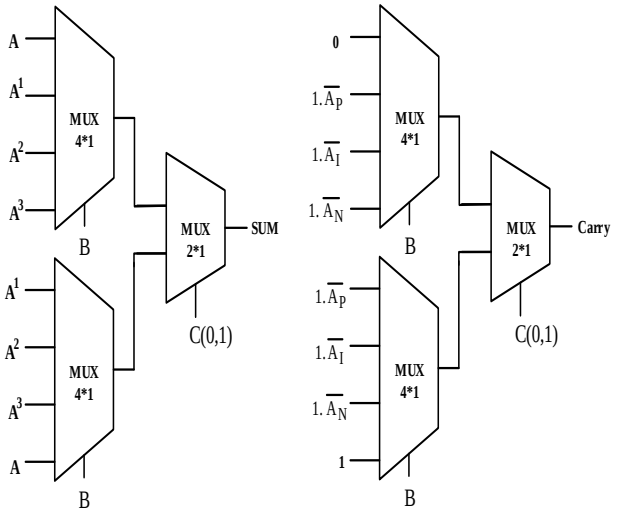


Fig. 5: Structure of the base quaternary FA [3].

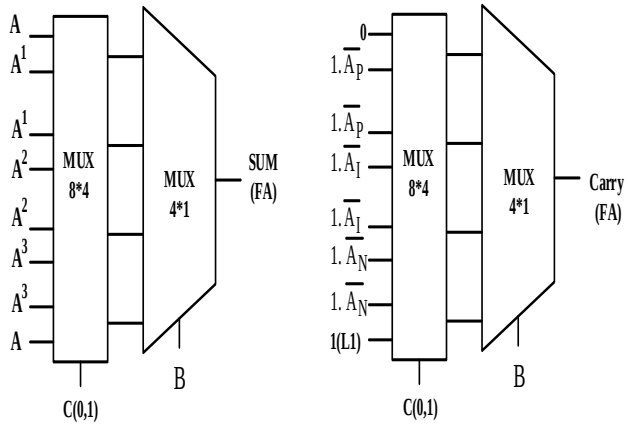


Fig. 6: The structure of the proposed QFA1.

As mentioned earlier, in normal mode, the highest carry will be 1 and can move to the next block in addition to the action. In the worst case, the Cout of a sum block can be the sum of 3 digits each with a value of 3. In this case, the maximum output Cout can be a value of 2 that can move to the next block. Table 7 presents the obtained results. To build a full adder based on Table 7 and with a basic multiplexer structure, 3 MUX 4*1 and 1 MUX 3*1 are required for each Sum and Carry output. The second full adder proposed in this article and with the idea expressed in the first full adder (Fig. 6) requires a MUX 12*4 and a MUX 4*1 to build each of the Sum and Carry blocks. In the new structure, 4 MUX 4*1s are less used than the base full adder mode. presents the structure of the second proposed full adder. In the MUX 12*4 structure, Cin is used as the selector; for example, by selecting C = 0, inputs A, A1, A2, and A3 appear at the outputs. In this way, 4 inputs are transferred to 4 outputs for each selection. Table 8 and Fig. 8 display the accuracy table and structure of the CE operator, respectively.

Table 7: QFA2 truth table

| Cin | B | A | Sum | Cout |
|---|---|---|---|---|
| 0 | 0 | A | A | 0 |
| 0 | 1 | A | $A^1$ | $1.\overline{A_P}$ |
| 0 | 2 | A | $A^2$ | $1.\overline{A_I}$ |
| 0 | 3 | A | $A^3$ | $1.\overline{A_N}$ |
| 1 | 0 | A | $A^1$ | $1.\overline{A_P}$ |
| 1 | 1 | A | $A^2$ | $1.\overline{A_I}$ |
| 1 | 2 | A | $A^3$ | $1.\overline{A_N}$ |
| 1 | 3 | A | A | 1 |
| 2 | 0 | A | $A^2$ | $1.\overline{A_I}$ |
| 2 | 1 | A | $A^3$ | $1.\overline{A_N}$ |
| 2 | 2 | A | A | 1 |
| 2 | 3 | A | $A^1$ | CE |

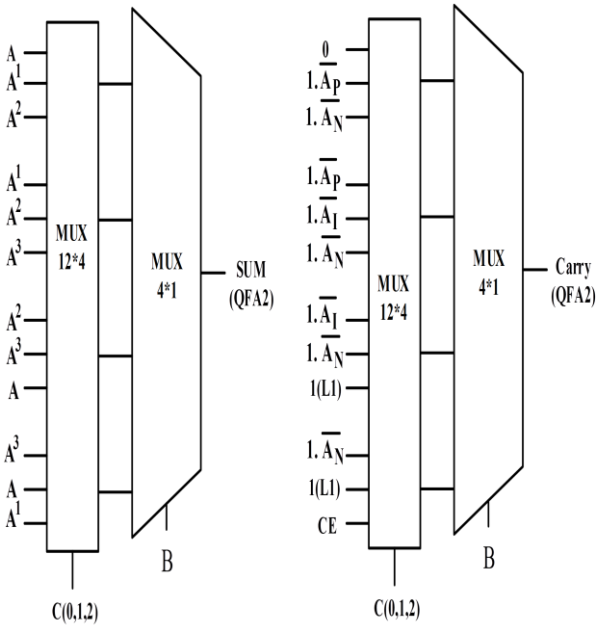


Fig. 7: The structure of the proposed QFA2.

Table 8: The truth table of the CE operator

| Cin | B | A | Sum | Cout |
|---|---|---|---|---|
| 2 | 3 | 0 | 1 | 1 |
| 2 | 3 | 1 | 2 | 1 |
| 2 | 3 | 2 | 3 | 1 |
| 2 | 3 | 3 | 0 | 2 |

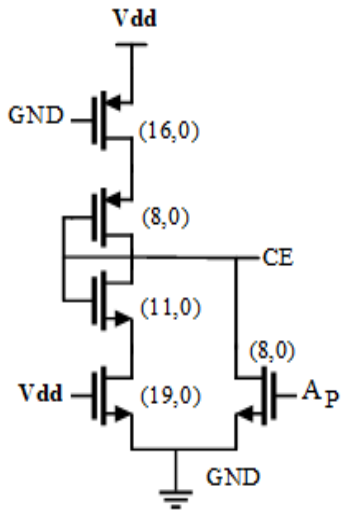


Fig. 9: Unary operator CE structure.

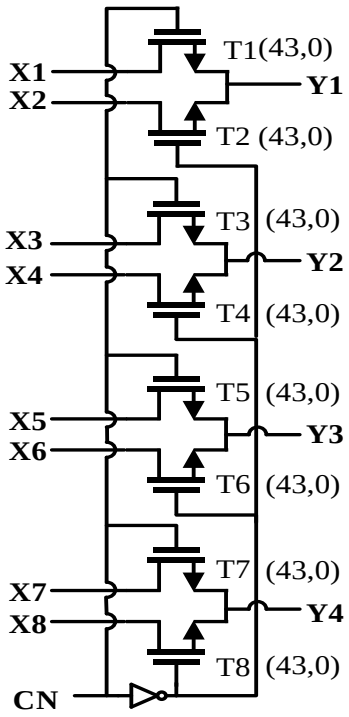


Fig. 10: Structure of the MUX8*4 used in the proposed QFA1.

### *B. Proposed Structure Multiplexer*

As mentioned in the previous section, in the proposed full adder, MUX 8*4 or MUX 12*4 were used to reduce their dimensions. The structure of these multiplexers is shown in Fig. 10 and 10. In the structure of these multiplexers, the Pass Transistor Logic method was used. Fig. 10 shows the structure of the MUX 8*4. In this MUX, if C = 0, transistors T1, T3, T5, and T7 turn on and inputs X1, X3, X5, X7 are transferred to the outputs. Also, if C = 1, transistors T2, T4, T6, and T8 turn on and the inputs X2, X4, X6, X8 are transferred to the output. A total of 10

CNTFETs were used for constructing the MUX 8*4. In the construction of the base full adder (

Fig. 5, 4 MUX 4*1 and 2 MUX 2*1, as well as 132 CNTFETs, were used. Regarding the structure of the first full adder proposed, two MUX 8*4 and two MUX 4*1 were used. Totally, 96 CNTFETs were used, indicating a 27% reduction.

*C. Proposed Structure Multiplexer*

As mentioned in the previous section, in the proposed full adder, MUX 8*4 or MUX 12*4 were used to reduce their dimensions. The structure of these multiplexers is shown in Fig. 10 and 10. In the structure of these multiplexers, the Pass Transistor Logic method was used. Fig. 10 shows the structure of the MUX 8*4. In this MUX, if C = 0, transistors T1, T3, T5, and T7 turn on and inputs X1, X3, X5, X7 are transferred to the outputs. Also, if C = 1, transistors T2, T4, T6, and T8 turn on and the inputs X2, X4, X6, X8 are transferred to the output. A total of 10 CNTFETs were used for constructing the MUX 8*4.

In the construction of the base full adder (Fig. 5), 4 MUX 4*1 and 2 MUX 2*1, as well as 132 CNTFETs, were used. Regarding the structure of the first full adder proposed, two MUX 8*4 and two MUX 4*1 were used. Totally, 96 CNTFETs were used, indicating a 27% reduction.

Fig. 13 shows the MUX 12*4 structure used in the proposed second full adder. This MUX has 20 CNTFETs. In MUX 12*4, if the signal C is selected 0, 1, or 2, then three groups of transistors (T1, T4, T7, T10), (T2, T5, T8, T11), or (T3, T6, T9, T12) are turned on to transmit input data to outputs.

In the base full adder, according to Table 7 and Fig. 5, 6 MUX 4*1 and two MUX 3*1 are required. A total of 224 CNTFEs were used to build multiplexers. In the design of the proposed second full adder (Fig. 5), 104 CNTFETs are used, which reduced the number of transistors by 53.6%.

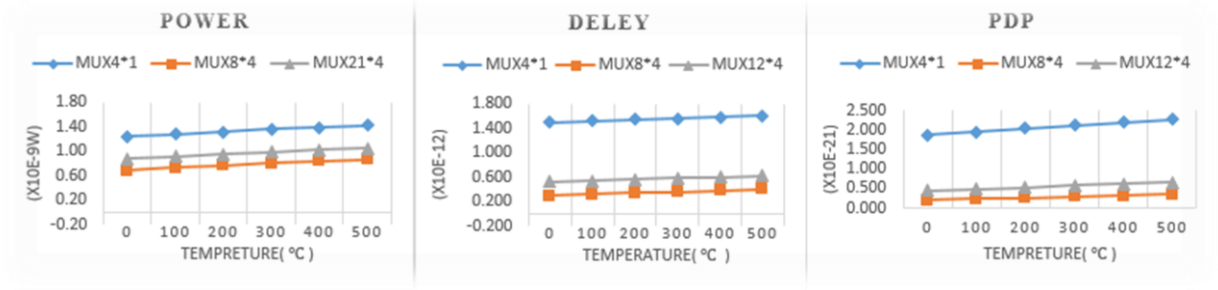


Fig. 11: Evaluation of the proposed MUX for different temperatures.


Fig. 12: Evaluation of the proposed MUX for different load capacitors.

## Results and Discussion

The simulation was run using Hspice software and 32 nm technology with a standard model proposed at Stanford University [18], [21].

In designing the circuits of Fig. 3, 6, and 7, nanotubes were considered to be between 4 and 8 such that MUX circuits were designed to have the best flow drive, a good fan-out with 8 tubes, and a control circuit with 4 tubes.

Fig. 11 and 12 present the accuracy and performance of the circuits designed at different temperatures and under different loads, respectively.

According to Fig. 11, variations of the power consumption are approximately 4 e-11w and the delay changes are approximately 2 e-14s to per 100°C. The proposed full adders were simulated using a 0.9-volt power supply.

The performance of evaluation criteria including delay propagation, average power consumption, and PDP, the number of transistors used, and the number of used power supplies are shown in Table 9. In this evaluation, the worst-case propagation delay includes the longest signal path and the maximum delay.

Table 9 compares all proposed full adders without load and in the presence of 0.7 and 2 fF capacitor loads. The results show a significant decrease in the number of transistors used, PDP, average power consumption, and propagation delay. The results of the first design [14] with no load were better than those of the proposed design.

However, [14] uses 3 power supplies while we employed just one power supply. As shown in the first proposed full adder, the number of transistors used indicates a 32% to 88% reduction compared to other designs.

Also, the proposed PDP design indicates a 50% to 100% reduction compared to other designs. Energy consumption in [20] with 0.7 FF capacitor load was better than the second proposal.

However, [20] uses 3 power supplies while we use only one power supply. As shown in the results of the second proposed full adder, 81.3% increase the propagation speed compared to [20] and in PDP 29% decrease compared to [19].

Finally, in the second full adder proposal, the number of transistors used indicates a 17.5% to 85.6% reduction compared to other designs and in 2fF capacitor load the resulting PDP decreased by 28% to 99% compared to other designs.

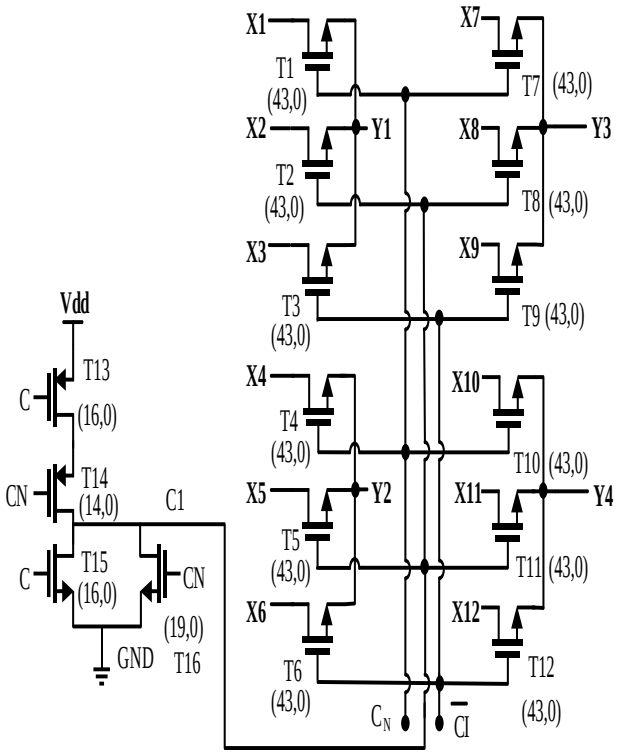


Fig. 13: The structure of MUX 12*4 used in the proposed QFA2.

## Conclusion

Applying MVL logic with CNTFET transistors speeds up computational circuits and decreases the chip size. In this paper, the new method Multiplexers Quaternary logic is designed.

The results showed that the use of these multiplexers in the design of full adders reduced the number of transistors used by 27% to 54% compared to base full adders.

Also, the other results showed a reduction in average energy consumption (by a minimum of 20% and a maximum of 99.5%) and PDP (29.25% to 98.94%).

These results may be of promising value for benefiting from nanotechnology. Finally, according to the results of the application of quaternary multiplexers in the construction of adders, it is possible to suggest the construction of processor circuits and fast and low-consumption arithmetic circuits based on nano transistors and multiplexers.

Also Multi-value multiplexer technology can be used to design telecommunication transmission lines and data networks for new generations of mobile phones.

## Author Contributions

S.Rahmati and E. Farshidi conceptualized the research. S.Rahmati designed the experiments and collected the data. S.Rahmati carried out the data analysis. E. Farshidi and J.Ganje validated the results. S.Rahmati wrote the manuscript. E. Farshidi and J.Ganje reviewed and edited the manuscript.

Table 9: Comparison of quaternary full adder performance

| C-Load= 0e-15fF | Power (uw) | Delay (ps) | PDP (e-16J) | Transistor count | Power Supply count |
|---|---|---|---|---|---|
| Proposed 1 (FA) | 0.7064 | 48.33 | 0.3414 | 93 | 1 |
| Proposed 2 (FA) | 0.7115 | 53.6 | 0.3713 | 113 | 1 |
| Design 1 [14] | 0.212 | 46.71 | 0.099 | 137 | 3 |
| Design 2 [14] | 0.884 | 43.88 | 0.387 | 157 | 1 |
| [12] | 2.467 | 71.72 | 1.178 | 195 | 1 |
| [6] | 75.34 | 112.7 | 84.95 | 163 | 1 |
| Design 1 [15] | 137.5 | 114.7 | 157.5 | 788 | 3 |
| Design 2 [15] | 57.73 | 71.54 | 41.25 | 154 | 1 |
| C-Load= 2e-15fF | | | | | |
| Proposed 1 (FA) | 0.9745 | 95.5 | 0.9306 | 93 | 1 |
| Proposed 2 (FA) | 1.216 | 109.67 | 1.33 | 113 | 1 |
| Design 1 [14] | 0.453 | 407.2 | 1.844 | 137 | 3 |
| Design 2 [14] | 1.161 | 665.0 | 7.721 | 157 | 1 |
| [12] | 2.657 | 107.9 | 2.871 | 195 | 1 |
| [7] | 102.4 | 122.3 | 125.3 | 163 | 1 |
| C-Load= 0.7e-15fF | | | | | |
| Proposed 2 (FA) | 0.986 | 42.53 | 0.4193 | 113 | 1 |
| [19] | 1.73 | 38.13 | 0.6596 | 212 | 1 |

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## Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

## Abbreviations

| | |
|---|---|
| *MVL* | Multi-Valued Logic |
| *MUX* | Multiplexer |
| *PDP* | Power Delay Product |
| *CMOS* | Complementary Metal-Oxide-Semiconductor |
| *CNTFET* | Carbon NanoTube Field Effect Transistors |
| *MOSFET* | Metal Oxide Semiconductor Field Effect Transistor |
| *IQI* | Intermediate Quaternary Invert |
| *NQI* | Negative Quaternary Invert |
| *PQI* | Positive Quaternary Invert |
| *SQI* | Standard Quaternary Standard Invert |
| *QHA* | Quaternary Half Adder |
| *QFA* | Quaternary Full Adder |

## References

[1] S. Iijima, "Helical microtubules of graphitic carbon," Nature, 354(6348): 56-58, 1991.

[2] G. E. Moore, "Cramming more components onto integrated circuits," IEEE Solid-State Circuits Society Newsletter, vol. 11(3): 33-35, 2006.

[3] J. Guo, S. O. Koswatta, N. Neophytou, M. Lundstrom, "Carbon nanotube field-effect transistors," International Journal of high-speed electronics and systems, 16,(4): 897-912, 2006.

[4] T. Temel, A. Morgul, "Implementation of multi-valued logic gates using full current-mode CMOS circuits," Analog Integrated Circuits and Signal Processing, 39(2): 191-204, 2004.

[5] A. N. Gupte, A. K. Goel, "Study of quaternary logic versus binary logic," in Proc. First Great Lakes Symposium on VLSI, 1991.

[6] F. Sharifi, M. H. Moaiyeri, K. Navi, "A novel quaternary full adder cell based on nanotechnology," International Journal of Modern Education and Computer Science, 7(3): 19, 2015.

[7] E. Abiri, A. Darabi, S. Salem, "Design of multiple-valued logic gates using gate-diffusion input for image processing applications," Computers & Electrical Engineering, 69: 142-157, 2018.

[8] D. Das, A. Banerjee, V. Prasad, "Design of ternary logic circuits using CNTFET," in Proc. 2018 International Symposium on Devices, Circuits and Systems (ISDCS), 2018: IEEE, pp. 1-6.

[9] K. Vasundara Patel, K. Gurumurthy, "Design of high-performance quaternary adders," International Journal of Computer Theory and Engineering, 2(6): 944-952, 2010.

[10] C. Vudadha, A. Surya, S. Agrawal, M. Srinivas, "Synthesis of Ternary Logic Circuits Using 2: 1 Multiplexers," IEEE Transactions on Circuits and Systems I: Regular Papers, 65(12): 4313-4325, 2018.

[11] S. Lin, Y.B. Kim, F. Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits," IEEE transactions on nanotechnology, 10(2): 217-225, 2009.

[12] S. A. Ebrahimi, M. R. Reshadinezhad, A. Bohlooli, M. Shahsavari, "Efficient CNTFET-based design of quaternary logic gates and arithmetic circuits," Microelectronics Journal, 53: 156-166, 2016.

[13] F. Sharifi, M. H. Moaiyeri, K. Navi, N. Bagherzadeh, "Quaternary full adder cells based on carbon nanotube FETs," Journal of Computational Electronics, 14(3): 762-772, 2015.

[14] E. Roosta, S. A. Hosseini, "A Novel Multiplexer-Based Quaternary Full Adder in Nanoelectronics," Circuits, Systems, and Signal Processing, 38(9): 4056-4078, 2019.

[15] B. Srinivasu, K. Sridharan, "Carbon nanotube FET-based low-delay and low-power multi-digit adder designs," IET Circuits, Devices & Systems, 11(4): 352-364, 2016.

[16] M. H. Moaiyeri, M. Nasiri, N. Khastoo, "An efficient ternary serial adder based on carbon nanotube FETs," Engineering Science and Technology, an International Journal, 19(1): 271-278, 2016.

[17] M. H. Moaiyeri, K. Navi, O. Hashemipour, "Design and evaluation of CNFET-based quaternary circuits," Circuits, Systems, and Signal Processing, 31(5): 1631-1652, 2012.

[18] J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: Model of the intrinsic channel region," IEEE Transactions on Electron Devices, 54(12): 3186-3194, 2007.

[19] A. Daraei, S.A. Hosseini, Novel energy-efficient and high-noise margin quaternary circuits in nanoelectronics, AEU Int. J. Electron. Commun. 105: 145–162, 2019.

[20] S. Fakhari, N. Hajizadeh Bastani , M.H. Moaiyeri, "A low-power and area-efficient quaternary adder based on CNTFET switching logic", Analog Integrated Circuits and Signal Processing, 98(1): 221-232, 2019

[21] J. Deng, "Device modeling and circuit performance evaluation for nanoscale devices: silicon technology beyond 45 nm node and carbon nanotube field-effect transistors," Stanford University, 2007.

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