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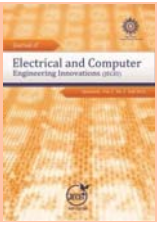
Journal of Electrical and Computer Engineering Innovations

JECEI, Vol. 2, No. 1, 2014

Regular Paper



A New Closed-form Mathematical Approach to Achieve Minimum Phase Noise in Frequency Synthesizers

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ARTICLE INFO

ARTICLE HISTORY:
Received 20 ctober 2013
Revised 15 December 2013
Accepted 15 December 2013

KEYWORDS:
Frequency synthesizers
Phase noise
Phase-locked loop
Phase noise reduction.

ABSTRACT

The aim of this paper is to minimize output phase noise for the pure signal synthesis in the frequency synthesizers. For this purpose, first, an exact mathematical model of phase locked loop (PLL) based frequency synthesizer is described and analyzed. Then, an exact closed-form formula in terms of synthesizer bandwidth and total output phase noise is extracted. Based on this formula, the phase noise diagram as a function of bandwidth is plotted. From the analysis and simulation results, it is observed that the synthesizer has a minimum phase noise at a particular bandwidth.

1. INTRODUCTION

Frequency Synthesizer is an important subsystem of any communication system and radar. A frequency synthesizer is a device that generates one or many frequencies from one or a few frequency sources. Practically, all communication systems use local oscillator (LO) based on frequency synthesis. It is widely used in telecommunication receivers, transmitters and radar systems, as a part of the frequency conversion block. The receiver must be sensitive, selective, and able to detect even a weak signal among many other, possibly stronger signals [1]. Therefore, a good receiver must have an accurate frequency in the local oscillator and low-noise components. However, a transmitter must produce a signal that has enough power, very accurate frequency and also as clean as spectrum.

One of the major issues facing synthesizer designers is the phase noise phenomenon. Phase noise is an undesirable entity that exists in all real world oscillators and signal generators. The phase noise term is used to describe phase fluctuations due to the random frequency fluctuations of signal. It may be cause distortion or damage of incoming information in traditional receivers, and it introduces high bit error rates in modern broadcasting systems because phase deviations directly increase the occurrence of errors in bit detection. Therefore, it is necessary to understand and quantify phase noise. Phase noise and those effects on the performance of synthesizer has been the subject of numerous studies [2]-[5].

Fortunately, Phase noise is a controllable problem. Oscillator designers can minimize phase noise in oscillators, and synthesizer designers can achieve to an appropriate design by choosing a low noise oscillator and other components of synthesizer. External noise and interference degrade the phase noise performance of synthesizers, and engineers need to be aware of these factors so that their effects can be anticipated or avoided. It is important to get the advanced phase noise model for frequency synthesizer, which is used in the broadcasting service transmitting system and receiving terminals, in prediction of phase noise effects and/or design of signal sources with low phase noise. The typical way for predicting the noise performance of the synthesizer is based on the linear phase-domain models that was described in locked state [3], [4].

In section 2, we describe the structure of Σ-Δ charge pump PLL (phase locked loops) and behavioral model of it. Third section represents the noise contribution in PLL and power spectral density (PSD) of each noise source. In section 4, a mathematical method has given to derive a closed-form relationship between synthesizer bandwidth and phase noise in a stable mode. Finally, in section 5, we simulate the mathematical results obtained in previous sections and draw the curve of total output phase noise as a function of bandwidth and discuss it by more details.

2. BACKGROUND

A. Structure of charge-pump PLL

Figure **1** depicts a block diagram of a typical Σ-Δ frequency synthesizer, containing four basic building blocks: phase/frequency detector (PFD), loop filter, voltage controlled oscillator (VCO) and frequency divider. The PFD compares the phase of the reference signal (Φ_{ref}) and divided feedback signal (Φ_{div}). The PFD's outputs are proportional to the input signals phase and frequency difference. These output signals (up and down) are fed to the charge pump, where they control the charge pump sink (I_{dn}) and source (I_{up}) currents.

If $f_{ref}>f_{div}$, the up signal will be non-zero and turn on its associated switch intermittently, while the down pulse will be zero continuously. This will inject positive charges into the loop filter, which in turn results in an increase in the output voltage, V_{tune}, to adjust the VCO frequency. If $f_{ref}<f_{div}$, vice versa of above process will be done.

The charge pump output current is converted to VCO control voltage through the loop filter to drive an external voltage-controlled oscillator (VCO) to increase or decrease the output frequency such that the PFDs average output tend towards zero. The loop filter attenuates high-frequency components in the PFD output so that a smoothed error signal is sent to the VCO input. It should be noted that in charge pump PLLs, the minimum order of the loop filter must be two [3]; therefore, we used a simplest and more typical architecture of loop filter in our system. The output frequency is fed back to the PFD through the divider. The loop reaches locked states when the reference and divided output signals have the same frequency and phase. Since, charge pump is a discrete-time system, as long as the dynamics of the loop are much slower than the signal, it can be considered as a continues-time system [5]. Therefore, in designs, the loop bandwidth to designate between 0.02 up to 0.1 of input frequency. Thus, by use of average value of discrete-time parameters, the PLL can be analyzed as a continuous-time system [6]. Exact analysis of charge pump PLL is given in [7].

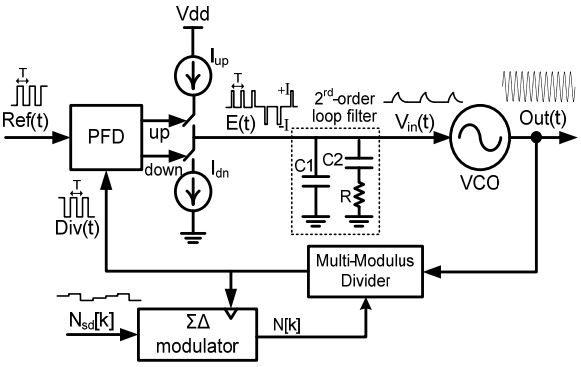

Figure 1: Block diagram of fractional-N frequency synthesizer.

As shown in Figure 1, a sigma delta modulator (SDM) is used to change the value of the frequency division at a high rate compared to the bandwidth of PLL so that, over time, the frequency is effectively divided by an average value that is fractional rather than integer. The resolution of these fractional values is determined by the length of the accumulators making up the SDM. To overcome the spurious signal generation problem, a fractional frequency synthesizer can exploit noise shaping in a multi-stage noise shaping (MASH) SDM in a similar way that analog to digital conversion utilizes this behavior. In a typical frequency synthesizer, the low-pass filtering operation is carried out on the quantization noise by the loop filter [8], [9]. A third order MASH Σ−Δ modulator is used in this design that exhibits by a 3rd-order noise transfer function and a 5-bit output.

B. Behavioural model

In order to reveal the noise contribution in the PLL based synthesizer, a model is needed which can help us to analyze the effect of each noise source into output phase noise. The transient response of the PLL is generally nonlinear, that cannot be formulated. But, in locked condition, the PLL acts as a LTI system and hence the superposition holds. The linear model, depicted in Figure 2, is used to analyze the behavior of the ΣΔ synthesizer in locked condition [10]. It is very useful for PLL stability and phase noise contribution analysis [11]. Note that this linearized model can be used to analyze the "small signal" dynamic properties of the PLL as well as its noise performance; that is, we consider only variations in the PLL frequency caused by small changes in the divider value. If the divider value is large, then cycle slip can be occurred and thereby invalidate our modeling assumptions [10].

Fortunately, for most practical cases, the frequency change is slowly enough to avoid losing frequency lock.

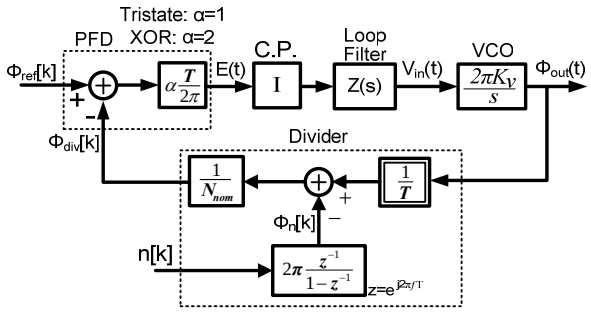

Figure 2: Behavioral model of a typical frequency synthesizer [10].

In the locked state, the phase of the reference source Φ_{ref} and divided VCO signal Φ_{div} are the same. The phase is the parameter of interest and phase characteristics for every block has to be derived.

The loop-filter transfer function, Z(s), is defined as the ratio of its output voltage to its input current. Equations for different loop filter architectures and the theory of their design can be found in [12]. In general, the loop filter design is one of the most critical parts of the synthesizer design. In point of view of noise, passive filters only introduce white noise due to resistors whereas active filters usually contain additive 1/f noise. This noise component is due to active devices (such as op-amp) in these filters.

In this study, we consider a PLL with type II and order of 2 that are fairly standard values for practical broadcasting systems. Therefore, as shown in

Figure **1**, the transfer function of desired loop filter (lead/lag) will be in the following form:

$$Z(s) = \frac{V_{in}(t)}{E(t)} = \frac{1}{sA_0} \cdot \frac{1+sT_2}{1+sT_1} \tag{1}$$

where $A_0=C_1+C_2$, $T_1=RC_1C_2/(C_1+C_2)$, and $T_2=1/RC_1$. This filter is convenient for most synthesizer applications due to the prohibitively high analog complexity required to achieve higher order or higher type values.

3. PHASE NOISE MODEL AND ANALYSIS

A. Noise sources

The noise sources in all building blocks of the PLL appear to as the noise power spectral density of output signal. Noise sources in the circuit can be divided into two groups, namely device noise and interference. Thermal, shot and flicker noises are examples of the former, while substrate and supply noises are in the latter group [13].

Each component of PLL introduces different types of noises. These noises due to active or passive devices employed in the blocks. In order to characterizing the output phase noise of the synthesizer, it is necessary that first we identify the noise properties of individual block of the synthesizer, and then we evaluate those influences on the output phase noise.

Fig. 3 displays the noise contribution of individual block of the synthesizer as additive noise. In this paper we assume that four noise sources appear in the PLL which are originated by PFD, charge pump, voltage-controlled oscillator, and Σ-Δ quantization noise. These noises pass through individual transfer function and affect on the output frequency spectrum of the synthesizer. Since these noise sources are small (compared to the desired signal) and uncorrelated to each other as well as behavioral model is linear, thus the output phase noise power spectrum density (PSD) is calculated by multiplying the input power spectrum density of noise sources, $S_{\varphi\text{-source}}(f)$, by the associated magnitude square of closed-loop transfer function, $F_{source}(f)$, which is defined as (F_{source} = □$_{out}/S_{\varphi\text{-source}}$).

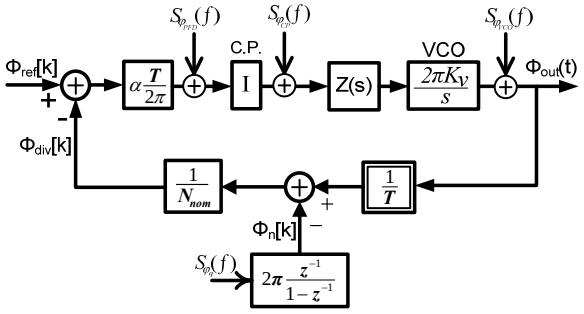

Figure 3: Noise contribution in the fractional synthesizer.

The position of the input noise sources vary depending on the investigating noise. It determines the ability of the system to terminate phase noise. The total output phase noise PSD of the synthesizer is given as follow:

$$S_{out}(f) = \sum_{all\ sources} S_{source}(f) \cdot |F_{source}(f)|^2 \tag{2}$$

By using superposition law, the total output phase noise will be the sum of the Eq. 2 on the all noise sources as follow:

$$S_{\varphi\text{-output}}(f) = S_{\varphi,PFD}(f) \cdot |F_{PFD}(f)|^2 + S_{\varphi,CP}(f) \cdot |F_{CP}(f)|^2 + S_{\varphi,VCO}(f) \cdot |F_{VCO}(f)|^2 + \frac{1}{T} S_{\varphi\text{-}q}(f) \cdot |F_q(f)|^2 \tag{3}$$

The term 1/T at later of equation (3), is that the discrete-time signal, $S_{\varphi\text{-}q}(f)$, is applied to a continuous-time system [10]. In the next sub-sections we investigate properties of each noise source.

A. VCO noise

Many studies performed to characterize the VCO phase noise [14], [15]. In frequency domain, the PSD of VCO noise model can be written as follow:

$$S_{\varphi,VCO} = k_{0,VCO} + \frac{k_{2,VCO}}{f^2} + \frac{k_{3,VCO}}{f^3} \quad (4)$$

According to above equation, the noise prototype of actual VCO have three parts correspond to 0dB/dec, -20dB/dec, and -30dB/dec slopes. The VCO deviates from the -20dB/dec roll-off at low frequencies due to flicker noise, and at high frequencies due to white noise floor. However, the assumption of -20dB/dec roll-off suffices for the frequency offsets of interests.

B. PFD/CP noise

The PFDs have an intrinsic noise in the white and flicker form. If special attention is not paid to their design, PFDs will be still susceptible to noise, particularly, $1/f$ noise, substrate and supply noises.

Their noise properties have been studied to some extent in [3]. In the behavioral simulations, we assume that the charge-pump noise magnitudes are approximately equal for positive and negative current sources. So, it is approximated by variance of up and down current sources which are in the white noise form.

C. Σ-Δ Quantization noise

The spectrum of the quantization noise is shaped according to the order and architecture of the Σ–Δ topology employed. We assume that a MASH structure [16], which is sampled at a rate equal to the reference frequency. Thus, the quantization noise changes continuously and it can be represented statistically as a white noise source [17]. In general, modeling of a Σ-Δ modulator is accomplished by assuming its quantization noise independent of its input. This leads to a linear time-invariant model that is parameterized by transfer functions from the input and quantization noise to the output. For instance, a MASH Σ-Δ modulator structure of order *m*, input *x[k]*, and output *y[k]* is described by:

$$y(z) = x(z) - (1 - z^{-1})^m r(z) \quad (5)$$

Where *r*[*k*] is quantization noise, that is shaped by the filter $(1-z^{-1})^m$ and appear in front of main divider. Quantization noise transfer function is a main performance factor of SDMs. In the 3rd-order MASH type, the quantization error noise spectrum is shaped by the transfer function given in follow [10]:

$$S_{\varphi-q}(f) = \frac{1}{12}(1 - z^{-1})^3 \quad (6)$$

By substituting $Z^{-1}=e^{-j2\pi fT}$ in above equation we have:

$$S_{\varphi-q}(f) = \frac{1}{12}(2\sin(\pi fT))^6 \quad (7)$$

D. Analysis

Now, the transfer functions of individual noise sources should be specified. To parameterize these transfer functions, it is convenient to define a base function that provides a simple description of all the PLL transfer functions of interest. If we define A(s) as the open loop transfer function of the PLL, following function, G(s), works well for this purpose.

$$G(s) = \frac{A(s)}{1 + A(s)} \quad (8)$$

where A(s) is the open loop transfer function in Figure 3 as follow:

$$A(s) = \left(\frac{\alpha}{2\pi}\right) \cdot I \cdot Z(s) \left(\frac{2\pi K_v}{s}\right) \left(\frac{1}{N_{nom}}\right)\Bigg|_{s=j2\pi f} \quad (9)$$

The magnitude square of closed-loop transfer function of each noise sources (mentioned in (2) and (3) as $F_{source}(f)$) is derived from Figure 3 as:

$$|F_{PFD}(s)|^2 = \left|\frac{\phi_{out}(s)}{S_{PFD}(s)}\right|^2 = \left|\frac{2\pi}{\alpha} \cdot N_{nom} \cdot G(s)\right|^2 \quad (10)$$

$$|F_{CP}(s)|^2 = \left|\frac{\phi_{out}(s)}{S_{CP}(s)}\right|^2 = \left|\frac{1}{I} \cdot \frac{2\pi}{\alpha} \cdot N_{nom} \cdot G(s)\right|^2 \quad (11)$$

$$|F_{VCO}(s)|^2 = \left|\frac{\phi_{out}(s)}{S_{VCO}(s)}\right|^2 = |1 - G(s)|^2 \quad (12)$$

$$|F_q(s)|^2 = \frac{1}{T}\left|\frac{\phi_{out}(s)}{S_q(s)}\right|^2 = \frac{1}{T}\left|2\pi \frac{z^{-1}}{1 - z^{-1}} \cdot T \cdot G(s)\right|^2 \quad (13)$$

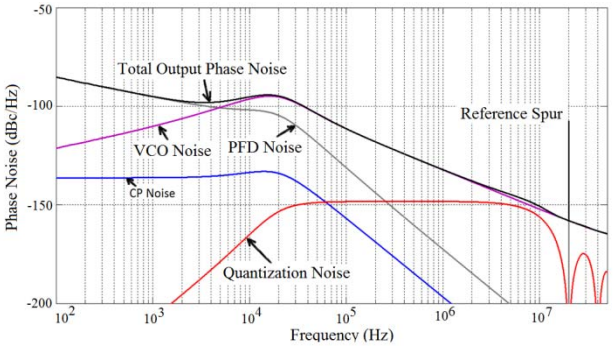

Figure 4: Phase noise characteristic of frequency synthesizer.

So, the output phase noise curve of the synthesizer can be derived by use of Eq. (3). Fig. 4 depicts the output phase noise due to each noise source as well as the total output phase noise. It is clear from Fig. 4 that the output phase noise is mainly influenced by the VCO phase noise for high offset frequency range and phase noise of the PFD for low offset frequency range.

Therefore, to simplify later calculations, we can rewrite the total output phase noise in terms of VCO noise and PFD noise only. So, by use of (3), (9), and (11) the total output phase noise will be written as follow:

$$S_{out}(f) = S_{pfd} \cdot \left|2\pi N G(f)\right|^2 + S_{vco}(f) \cdot \left|1 - G(f)\right|^2 \quad (14)$$

4. METHODOLOGY

In this section, we attempt to find a closed form relation between total output phase noise (Sout(f)) and the closed-loop bandwidth of the synthesizer, i.e., ω_c. For this reason, G(f) in (12) must be extracted only as a function of the bandwidth of system. As shown in (8), G(f) is in terms of A(f) only and therefore, A(f) must be extracted in terms of the bandwidth only.

Substituting (1) into (9) and arranging, we have:

$$A(s) = \frac{I \cdot K_v}{N \cdot s} \cdot \frac{1}{s \cdot A_0} \cdot \frac{1 + sT_2}{1 + sT_1} \quad (15)$$

Assuming φ to be the phase margin of the loop, we have:

$$\tan^{-1}(\omega_c T_2) - \tan^{-1}(\omega_c T_1) = \varphi \quad (16)$$

Tangent of the angle φ in the above equation could be written as:

$$\frac{\omega_c (T_2 - T_1)}{1 + \omega_c^2 T_1 T_2} = \tan\varphi \quad (17)$$

In the PLL design, it is highly desirable to let the maximum phase of the open loop transfer function, $\angle A(j\omega)$, occur at the crossover frequency ω_c in order to obtain the maximum phase margin.

In addition, at the maximum point the first order derivative of the phase is zero, which implies the phase margin has a least sensitivity to the loop parameter variation. The phase of A(s) is:

$$\theta = \angle A(j\omega) = -180 + \tan^{-1}(\omega T_2) - \tan^{-1}(\omega T_1) \quad (18)$$

Let $\left.\frac{d\theta}{d\omega}\right|_{\omega=\omega_c} = 0$, to obtain follow equation:

$$\omega_c = \frac{1}{\sqrt{T_1 T_2}} \quad (19)$$

Substituting (17) into (19), we have:

$$\sqrt{\frac{T_2}{T_1}} - \sqrt{\frac{T_1}{T_2}} = 2\tan\varphi \quad (20)$$

Equation (20) can be written as:

$$\eta + \frac{1}{\eta} = 2 + 4\tan^2\varphi \quad (21)$$

where $\eta = \frac{T_2}{T_1}$. Furthermore, using (19) we can write:

$$T_1 = \frac{1}{\omega_c\sqrt{\eta}} \quad T_2 = \frac{\sqrt{\eta}}{\omega_c} \quad (22)$$

Since in the bandwidth frequency, magnitude of the open loop transfer function is equal to one, i.e., $|A(j\omega_c)|=1$, the constant A_0 is obtained as follow:

$$A_0 = \frac{IK_v}{N\omega_c^2} \cdot \frac{\sqrt{1 + (\omega_c T_2)^2}}{\sqrt{1 + (\omega_c T_1)^2}} = \frac{IK_v\sqrt{\eta}}{N\omega_c^2} \quad (23)$$

By solving the second order equation in (21), two possible values for η can be achieved. Since η is the pole to zero ratio of the loop filter which is always more than 1 for stable systems, we can select one of the two possible answers as follow:

$$\eta = \frac{2 + 4\tan^2\varphi + \sqrt{(2 + 4\tan^2\varphi)^2 - 4}}{2} \quad (24)$$

Now, by substituting (22) and (23) into (15), the open loop transfer function, A(f), could be written in terms of the closed-loop bandwidth(ω_c) and η only:

$$A(f) = \frac{IK_v}{jN2\pi f} \cdot \frac{N\omega_c^2}{j2\pi f IK_v\sqrt{\eta}} \cdot \frac{1 + s\sqrt{\eta}/\omega_c}{1 + s/\omega_c\sqrt{\eta}} \quad (25)$$

where η is obtained from (24).

5. SIMULATION RESULTS AND DISCUSSION

Fig. 5 shows the total output phase noise for several closed loop bandwidths in phase margin of 45°. Each curve has a local maximum around its designed bandwidth frequency. In 4 kHz bandwidth, the phase noise PSD at low offset frequencies is large. If the closed loop bandwidth is increased, the local maximum point is shifted into higher offset frequencies. However, this figure can't show which bandwidth gives the minimum phase noise, since by increasing the bandwidth of the system, the phase noise increases in some region and decreases in another region (e.g. 20 kHz and 200 kHz bandwidth in Figure 5).

To evaluate the effect of various bandwidths on the total output phase noise, we calculate the phase noise power in a particular frequency range for each bandwidth. In fact, we evaluate the phase noise power instead of the phase noise power density. To find the phase noise power, the PSD of phase noise is integrated with interested frequency range (f_1~f_2). This integral may be written as equation (26). In this paper, interested frequency region is from 1Hz to 1MHz.

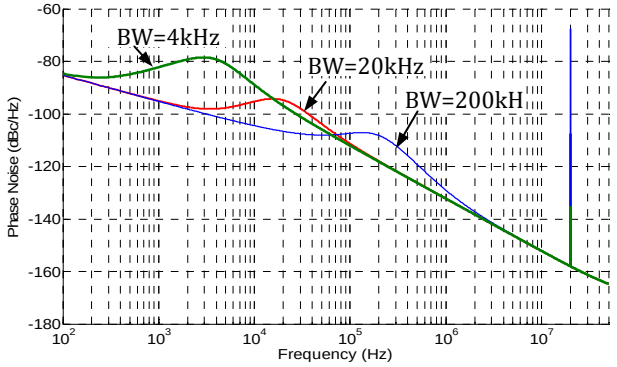

Figure 5:Total output phase noise in bandwidths of 4 kHz, 20 kHz, and 200 kHz.

$$P_{noise_{out}} = \int_{1}^{10^6} S_{out}(f)df \qquad (26)$$

Fig. 6 shows the phase noise power as a function of closed loop bandwidth. As seen, there is an optimum closed loop bandwidth for minimization of phase noise of the synthesizer. In 100 KHz bandwidth, we achieve this minimum phase noise power. Practically, selecting the bandwidth in the range of 30 kHz up to 200 kHz is appropriate for many applications. In this range, larger bandwidths lead to faster lock time but larger reference spur. Furthermore, the loop bandwidth must be between 0.02 up to 0.1 of input frequency to accomplish stability considerations.

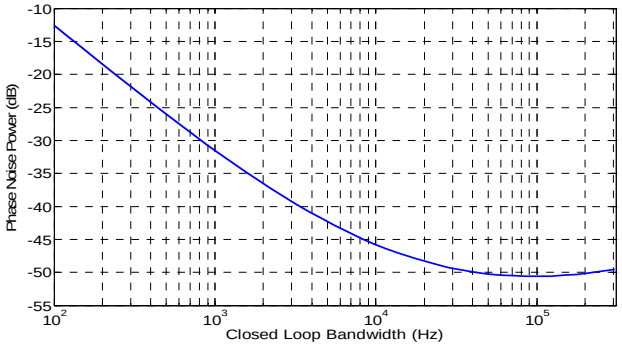

Figure 6: Total phase noise power for closed loop bandwidth.

6. CONCLUSIONS

This paper was addressed the phase noise of the ΣΔ-frequency synthesizer with second-order passive loop filter. A mathematical and accurate model for phase noise of the frequency synthesizer was presented taking into account noise of its components. As we know, Noise sources are: phase/frequency detector, charge pump, VCO, and Σ-Δ quantization noise. Then, output phase noise was predicted in terms of these parameters. A closed-form relationship between the output phase noise and closed loop bandwidth of the synthesizer was also extracted. Finally, the value of optimal closed loop bandwidth minimizing the phase noise was obtained in phase noise analysis.

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BIOGRAPHIES

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