Journal of Electrical and Computer Engineering Innovations
(JECEI)
Journal homepage: http://www.jecei.sru.ac.ir

Research paper

# A 28-36 GHz Optimized CMOS Distributed Doherty Power Amplifier with A New Wideband Power Divider Structure

*M S. Mirzajani Darestani*[1], *M. B. Tavakoli*[1,*], *P. Amiri*[2]

[1]*Department of Electrical Engineering, Arak Branch, Islamic Azad University, Arak, Iran.*

[2]*Department of Electrical Engineering, Shahid Rajaee Teacher Training University, Tehran, Iran.*

## Article Info

**Article History:**
Received 09 March 2019
Reviewed 03 May 2019
Revised 27 July 2019
Accepted 03 December 2019

**Keywords:**
CMOS power amplifier
Distributed structure
Doherty power amplifier
Ka Band
Power divider.

[*]Corresponding Author's Email Address:
*m-tavakoli@iau-arak.ac.ir*

## Abstract

**Background and Objectives:** In this paper, a new design strategy was proposed in order to enhance bandwidth and efficiency of power amplifier.
**Methods:** To realize the introduced design strategy, a power amplifier was designed using TSMC CMOS 0.18um technology for operating in the Ka band, i.e. the frequency range of 26.5-40GHz. To design the power amplifier, first a power divider (PD) with a very wide bandwidth, i.e. 1-40GHz, was designed to cover the whole Ka band. The designed Doherty power amplifier consisted of two different amplification paths called main and auxiliary. To amplify the signal in each of the two pathways, a cascade distributed power amplifier was used. The main reason for combining the distributed structure and cascade structure was to increase the gain and linearity of the power amplifier.
**Results:** Measurements results for designed power divider are in good agreement with simulations results. The simulation results for the introduced structure of power amplifier indicated that the gain of proposed power amplifier at the frequency of 26-35GHz was more than 30dB. The diagram of return loss at the input and output of power amplifier in the whole Ka band was less than -8dB. The maximum Power Added Efficiency (PAE) of the designed power amplifier was 80%. The output $P_{1dB}$ of the introduced structure was 36dB, and the output power of power amplifier was 36dBm. Finally, the IP3 value of power amplifier was about 17dB.
**Conclusion:** The strategy presented in this paper is based on usage of Doherty and distributed structures and a new wideband power divider to benefit from their advantages simultaneously.



## Introduction

Recently, owing to the fact that high-speed communication systems with high speed and high data rate have wide variety of applications, the transmission of data is going to be done by using modern structures, in which one of the initial necessities would be low power consumption and high efficiency. Battery life is one of the main problems related to the new wireless systems [1]. One of the main specifications between power amplifiers is that the highest value for efficiency is obtained only at its maximum output power. Efficiency significantly diminishes with reducing the output power [1]. Under normal circumstances, the power transmission of power amplifier (PA) is less than the maximum output power. Thus, the effective efficiency is far lower than the maximum value. Increasing the efficiency of the amplifier leads to a direct reduction in power consumption [2]. Doherty amplifier improves the

power efficiency for a linear power amplifier over a wide range of output powers [3].

On the other hand, the fifth generation (5G) mobile network scenario is very different from the current mobile standards (ex. LTE) in terms of both frequency band and hardware infrastructure [4],[5]. This network consist of higher cell density, and hence, lower maximum power, carrier frequency in Ka band, broadband, new access methods such as Beam Division Multiple Access (BDMA) and Massive multi-input and multi-output (MIMO) [6]. In addition, in complex modulation schemes, the maximum to average power ratio is greater than 12dB [7]. Such a scenario would definitely apply more strict requirements on the transmitter system, especially for the power amplifier, which is widely known as responsible for the linear efficiency of the entire radio [7]. Thus, the power amplifier efficiency is very significant in 5G, since it is closely related to the base station operating costs and phone battery life. Indeed, the renowned Doherty architecture obtains a high average efficiency in a wide range of RF output powers through active load modulation [8].

Another important issue in telecommunication systems is bandwidth. The most common way to design amplifier in broadband systems is distributed amplifier structure. The bandwidth and performance which are two major challenges have been the focus of power amplifier designers in recent years. Thus, in this paper, using both distributed and Doherty structures simultaneously and benefiting from the proposed wideband power divider (PD), we have been able to obtain these two important factors concurrently with acceptable values. The introduced structure was designed and simulated for a frequency range of 26 to 40GHz, using TSMC CMOS 0.18um process. All simulations have been performed in Advanced Designed System (ADS) software.

## Power Divider

### *A. Design Principle*

Commonly, the amount of power that can be achieved from the output of a single solid-state device is not enough for high frequency applications. As a result, combining the output power of several devices seems to be necessary to achieve demanded power value [9]. Different methods have been proposed for millimeter-wave power combining. One of the most familiar power divider is 3dB-Wilkinson, which is a two-way equal split type. The two-way Wilkinson combiner has applications not only at microwave but also at millimeter-wave frequencies; owing to its low losses [10]. S.B. Cohn modified the primary structure of the two-way Wilkinson in order to increase the bandwidth to one decade [10]. The method is based on substituting the one-step quarter-wave transformer with distributed parts. These parts, containing N pairs of equal-length TLs (transmission line), form the main structure of the two-way multi-stage Wilkinson PD.

Since the most important problem of single-resistor Wilkinson power divider is its very low bandwidth, in the present paper, to increase the bandwidth of the designed PD, we have combined five Wilkinson power dividers. Then, by optimizing its different parts, we have been able to extend the bandwidth very widely. Although many articles have used multistage Wilkinson power divider technique, they have not been able to achieve this broad bandwidth. In this study, all sections are curved, enhancing the bandwidth compared to the previous studies which used rectangular stubs. Indeed, when we use rectangular lines, there are fractures at angular points, which produce resonance and limit the bandwidth. The proposed power divider consists of five single Wilkinson power dividers. Accordingly, there are five resistors in the power divider which are used to isolate the two output ports. Since the introduced PD has a wide band and works up to 40GHz, a Rogers high-frequency substrate (RO5880) with the dielectric constant of 2.2 and a thickness of 0.127mm was used to design and fabricate the PD. The other advantage of the introduced PD is its compactness. The size of the introduced PD is 24.3mm×10mm×0.127mm. The schematic of the designed PD and photograph of the fabricated is shown in Fig. 1 and Fig. 2, respectively.

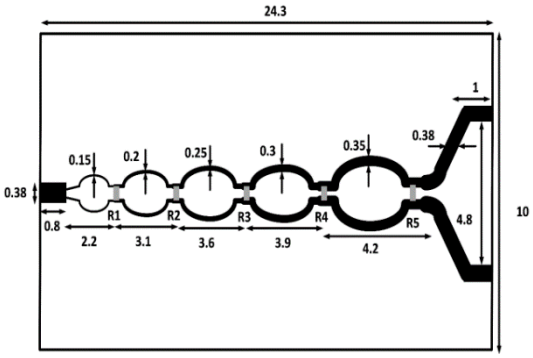


Fig. 1: Structure of introduced PD.

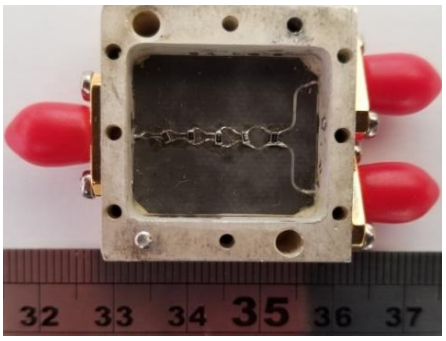


Fig. 2: Manufactured PD.

*B. Simulation and measurement Results*

The diagram of return losses at the three ports of the PD is shown in Fig. 3. The major advantage of the introduced PD is its wide bandwidth. It is observed in Fig. 3 that the values of return losses of the three ports of the designed PD over the entire Ka band are below -15dB, which is far lower than the benchmark of -10dB.

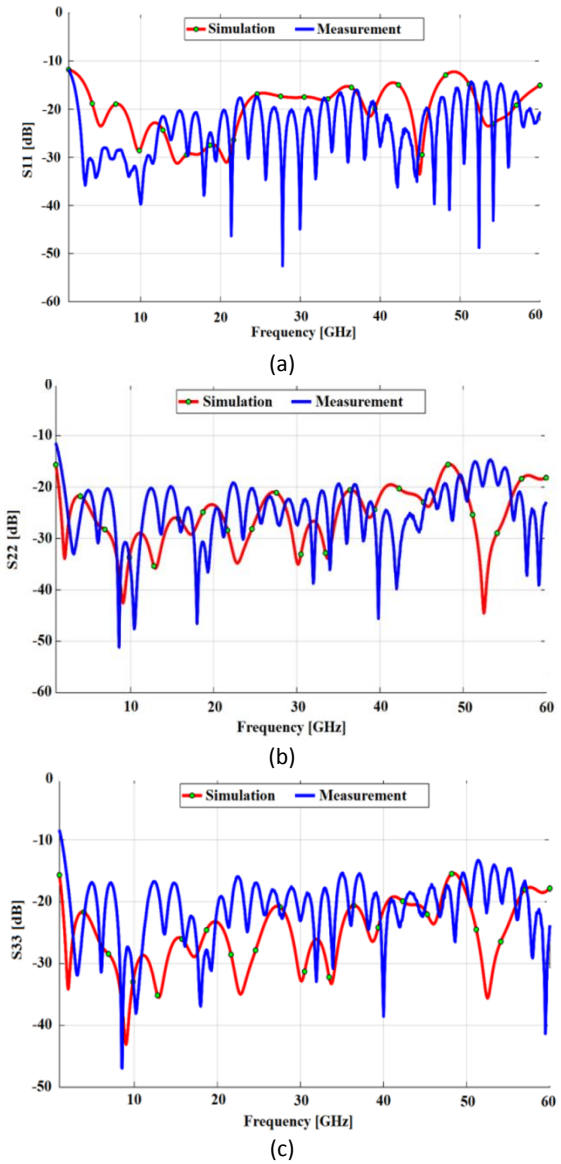


Fig. 3: Return losses at the: a) input port. b) and c) output port.

The transmission diagrams of the proposed PD are depicted in Fig. 4. It can be observed that the ripple rate of each diagram of $S_{12}$ and $S_{13}$ at the frequency of 1-40GHz is less than 0.4dB. Also, the inherent loss of the proposed power divider over the whole band is about 0.1dB. Hence, the sum of the ripples and inherent loss of each of the $S_{12}$ and $S_{13}$ diagrams at the frequency of 1–40GHz is 0.5dB. This means that the $S_{12}$ and $S_{13}$ diagrams, at the frequency range of 1–40GHz, is between -3dB to -3.5dB. This suggests that the inherent loss of the designed PD, at the frequency of 1–40GHz, is lower than 0.5dB.

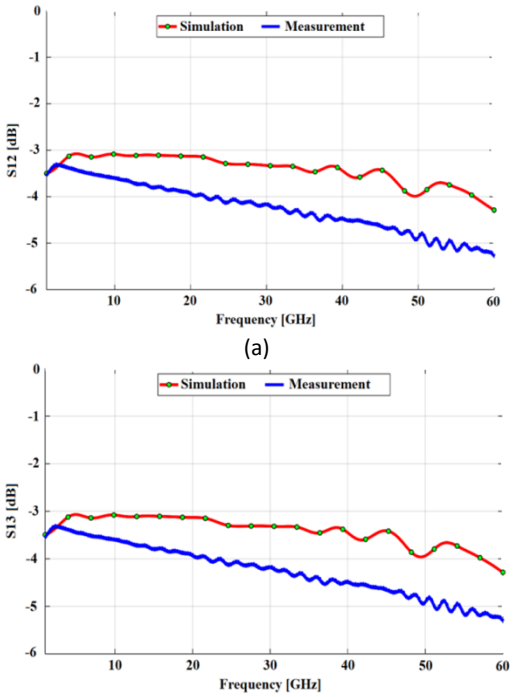


Fig. 4: Transmission diagrams.

It is observed in Fig. 5 that the isolation between the two output ports for the designed PD at 1-40GHz is less than -12dB, indicating that there is a good isolation in the proposed power divider within the entire operating band.

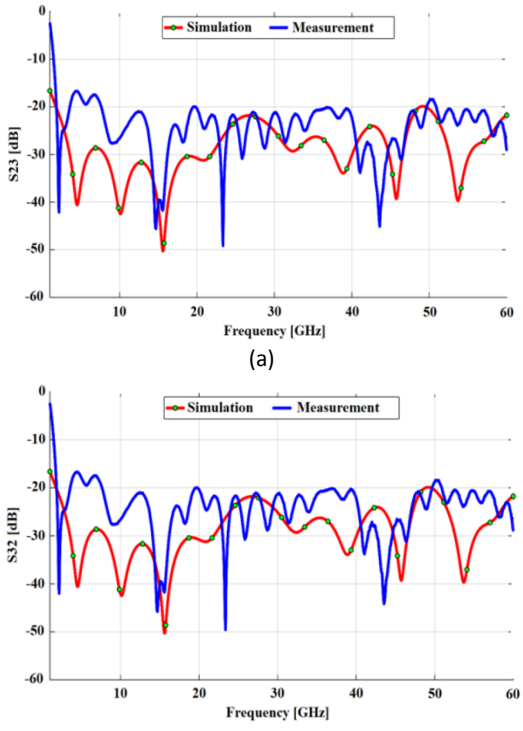


Fig. 5: Isolation of the two output ports.

A review of previous research and its comparison with the current study revealed the advantages of the proposed technique as provided in Table 1.

Table 1: Comparison between operational features of the introduced PD and others developed in previous articles

| Reference | Bandwidth percentage compared to Ka band (%) | Return loss at output ports (dB) | Return loss at input port (dB) | Isolation (dB) | Inherent loss (dB) | Size (mm) | Material | Center frequency (GHz) |
|---|---|---|---|---|---|---|---|---|
| [10] | 60 | < 22 | < 10 | < 15 | 0.5 | 25*35 | FR4 | 3.7 |
| [11] | 110 | < 16.1 | < 15.3 | < 15 | 0.46 | 13*9 | - | 4 |
| [12] | 42 | < 10 | < 10 | < 8 | 0.8 | 10.95*10.2 | RO5880 | 38 |
| [13] | 100 | - | < 15 | - | 0.6 | 35*45 | RO5880 | 4 |
| [14] | 133 | < 15 | < 15 | < 20 | 0.5 | 42*26 | RO5880 | 6 |
| [15] | 90 | < 15 | < 15 | < 15 | 0.4 | 55*31 | FR4 | 1.1 |
| [16] | 109 | < 17 | < 14.7 | < 15.3 | 0.52 | 21*4.6 | - | 6.8 |
| [17] | 101 | < 10 | < 10 | < 10 | 1 | - | - | 6.3 |
| **This work** | **190** | **< 22** | **< 14** | **< 12** | **0.45** | **10*24.3** | **RO5880** | **20.5** |

## Power Amplifier

In power amplifiers, the efficiency is defined as the ratio of the average output power to DC power consumption. Power amplifiers operate mostly on the average power. Indeed, they spend a short time at the maximum power. Thus, their average power efficiency is very important. In conventional amplifiers such as class A, B, and AB power amplifiers, the higher the efficiency at higher powers, the lower the average power efficiency. The high average efficiency is one of the essential parameters for mobile systems, when battery lifetime is considered. To enhance this parameter, a wide variety of solutions have proposed during the history [18]. W. H. Doherty introduced an effective approach in 1936 [19].

The Doherty Power Amplifier (DPA) is according to the modulating the load of an amplifying device. Hence, this process will result in operating of the amplifier at its highest efficiency for a pre-destined value of input and/or output power [20]. As a result, the termination of the amplifying device, Main (or Carrier), is modulated based on load modulation idea [21], [22], by utilizing another active device, Auxiliary (or Peaking). A general structure for Doherty power amplifier is shown in Fig. 6.

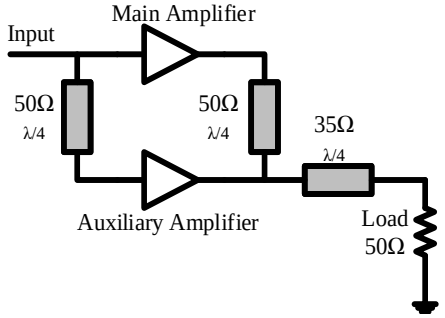


Fig. 6: Typical DPA configuration.

The load modulation circuit operates based on the idea of combining the asymmetric power obtained from the output of both active devices in a current-combining manner. Therefore, the main amplifier functions with maximum performance at a low-power condition and the maximum performance at the higher-power situation [7]. In general, a power amplifier, with certain optimized termination impedance, provides the utmost effectiveness merely at maximum power because the full output voltage and current fluctuations are obtained merely at the maximum of the output power described by the constant load. The dynamically load modulation of DPA will result in the maximum performance at the various power levels specified by the modulated load. In the load modulation process, the carrier amplifier gives the peak effectiveness at one-second of the utmost input voltage, and the utmost effectiveness is kept via this process at a greater power as depicted in Fig. 7.

Fig. 7

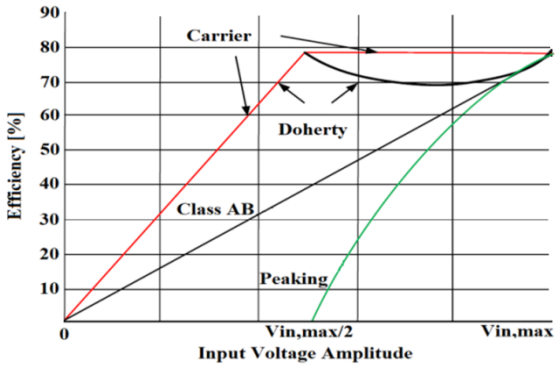


Fig. 7: Efficiencies of DPA vs. input voltage for DPA.

In the low-power area ($0<V_{in}<V_{in,max}/2$), the auxiliary amplifier stays in the cut-off condition, and the load of the main amplifier is twice as large as that of the conventional structure. Therefore, the carrier amplifier achieves the saturation condition at the input voltage of ($V_{in,max}/2$), because the utmost fluctuation of voltage obtains $V_{dc}$ at one-second the current highest level. Consequently, the peak power value is one-second that of main amplifier, and the effectiveness of the DPA is as same as the utmost effectiveness of the main amplifier. In this low-power behavior, merely the main amplifier

with a one-second of the whole power cell generates power, and the effectiveness at a pre-determined power value is double as high as a power cell amplifier [7].

In the higher-power region ($V_{in,max}/2<V_{in}<V_{in,max}$), in which the auxiliary amplifier is ON, the main amplifier produces power with the maximum effectiveness, because the saturated operation is kept owing to the load modulation.

The auxiliary amplifier functions at a large load at the turning on state, and the effectiveness enhances quickly; however, it is still less than the maximum effectiveness. Therefore, the whole effectiveness of the DPA structure is decreased.

However, the next point for effectiveness is obtained when the peaking amplifier with saturated operation generates the utmost effectiveness at the maximum power.

Thus, it has two utmost effectiveness places, improving the effectiveness at the back off output power value as illustrated in

Fig. 7. As a result, the effectiveness of the Doherty structure at the peak point of the input voltage is as same as the utmost effectiveness of the known amplifiers [7].

Hence, the DPA structure generates more effectiveness across the whole power levels in comparison with an ordinary class B amplifier. The obtained structure for DPA can overcome the low efficiency difficulty for amplification of a large peak to average power ratio (PAPR) signal. Thus, DPA structure would be a good choice to increase effectiveness. On the other hand, one of the main concerns about DPA is the limited RF bandwidth.

In Broadband data transmission and receiving systems as well as applications requiring broadband linear phase amplification, there are various approaches to design amplifiers. The most common way is distributed amplifiers structure. Distributed amplifiers (DA) are usually used as a suitable broadband amplifier in telecommunications.

Since they have a stable gain over a wide bandwidth, they prevent the scattering of the received signals [23]. The main idea in the distributed structure is to use multiple cascade transistors to enhance the gain and promote simultaneous absorption of parasitic capacitors into drain and gate transmission lines to acquire a broad bandwidth [24].

The principal form of the distributed amplifier can be seen in Fig. 8, in which a cascade of identical transistors are used, while their gates joined to a TL with a characteristic impedance of $Z_{0g}$ and a length of $l_g$, and their drains are joined to a TL with a characteristic impedance of $Z_{0d}$, and a length of $l_d$ [25].

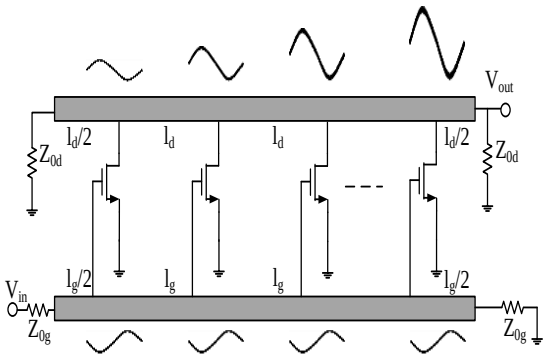


Fig. 8: Basic structure of the distributed amplifier.

The DA structure is based on simultaneous enhancement of the gain and bandwidth of power amplifier [25].

The input voltage wave propagates via the gate line and attains the gate of the transistors with phase shifts. Each transistor increases its gate voltage and produces a drain current via the drain line. If the gate and drain line parts cause same phase shifts, i.e.,

$$\beta_g l_g = \beta_d l_d \quad (1)$$

where $\beta_g$ and $\beta_d$ is the propagation constant of the gate and drain line, respectively, the drain current obtains the termination impedance and effective combine. These lines are ended in their termination characteristic impedance at the other end to attract waves moving in the opposite ways [25]. It is assumed that, the transconductance gain of each element is $G_m$ and the output impedance can be observed by transistors, is one-second of the characteristic impedance of the TL, the gain of the voltage is as (2):

$$A_v = \frac{1}{2} n G_m Z_{0d} \quad (2)$$

Here, n is the number of stages and $Z_{0d}$ is characteristic impedance of the drain line. The gain of the distributed amplifier can be enhanced via utilizing further stages or higher $G_m$. $Z_{0d}$ is tuned by the condition of output impedance matching. It should be considered that (2) is obtained supposing lossless TLs. Due to the existence of loss in TLs, the voltage amplitude weakens as it propagates the gate and drain lines. This result cause the degradation of voltage gain in case further stages are utilized [25]. Hence, there would be an optimized number of gain stages that causes the voltage gain enhancement. The circuit schematic of Fig. 8 assumes that parasitic capacitances of the transistors are evenly propagated along the TLs. The model presented in Fig. 8 cannot propose a realistic evaluation of the DA bandwidth. Moreover, the distributed amplifier could be introduced by lumped-element artificial TLs as depicted in Fig. 9.

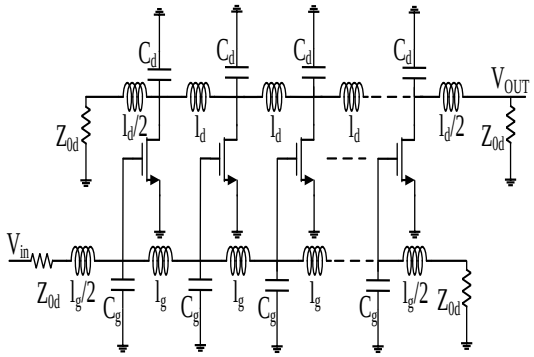


Fig. 9: Distributed amplifier structure constructed by lumped-element artificial transmission lines.

The condition (1) is changed as

$$l_g C_g = l_d C_d \tag{3}$$

Here, $C_g$ and $C_d$ are capacitances at the gate and drain of each transistor, whereas $L_g$ and $L_d$ indicate the inductance of the gate and drain lines, respectively. The bandwidth of the distributed amplifier is restricted by the cut-off frequency of the gate and drain lines. The cut-off frequency can be obtained as follow [25]:

$$\omega_C = \frac{2}{\sqrt{LC}} \tag{4}$$

Here, L and C are the inductance and capacitance of the lumped-element line, supposing that gate and drain lines have equal cut-off frequencies. The wave crossing via the lumped-element line is significantly attenuated over the cut-off frequency. Transistors in small size should be used to obtain higher bandwidth that will decrease the gain of distributed amplifiers. Since the characteristic impedance of the lines is specified by the ratio of L/C, inductance L would not be small to obtain more bandwidth. Therefore, there exists a trade-off between gain and bandwidth in distributed amplifiers. The input capacitance of transistors is the main parasitic capacitance that confines bandwidth of distributed amplifiers. Coupling by using capacitor is an introduced way to reduce the loading result of the gate-source capacitance on the gate line [25]. A capacitor is put in series with the gate of transistors to decrease the capacitance to $C_{gs}=(1 + C_{gs}/C_c)$ [Fig. 10 (a)].

A large resistor in parallel with $C_C$ makes a way for the gate bias. It is worth mentioning that the gain of voltage is decreased by the factor $1 + C_{gs}/C_C$ owing to the splitting of voltage at the input of transistors. The method is generally applied in distributed amplifiers in which the gate-source capacitance of large transistors can confine bandwidth and gain is not the initial priority in design procedure. Other method proposed to decrease the loading result of the input impedance of transistors is utilizing a common-source amplifier with $R_C$ degeneration Fig. 10 (b) as the gain stage. The impedance can be seen at the input of the amplifier is obtained as a series resistance and capacitance. i.e. $Z_{in} = R_{in} + 1/j\omega C_{in}$. With appropriate adjustment of the circuit elements, the parameters of the amplifier are achieved as $R_{in} = 0$, $C_{in} = C_{gs}=(1 + g_m R_s)$, and $G_m = g_m=(1 + g_m R_s)$. Therefore, the input capacitance is declined, that will result in transconductance degradation. In fact, the elements of the circuit are adjusted to obtain negative input resistance. This method is utilized to minimize the loss impact of the gate TL and input parasitic resistance of the transistor. The cascode amplifier depicted in Fig. 10 (c) is a popular structure can be utilized to make high isolation between input and output of the distributed amplifier. The inter-stage inductance transfers the pole related to the inter-stage parasitic capacitance to higher frequencies, and thus, enhances bandwidth [26].

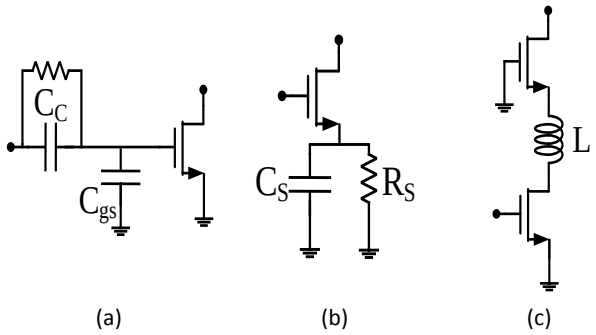


Fig. 10: The conventional structures can be utilized as gain stage of distributed amplifiers. (a) Capacitive coupling, (b) Source RC degeneration, (c) Bandwidth-improved cascode amplifier

To enhance the gain of the distributed amplifier, multi-stage amplifiers are used as the gain stage. Bandwidth improvement methods can be applied to prevent bandwidth constraints by inter-stage parasitic capacitances. The amplifier stages have a bit different 3-dB bandwidths and gain enhancement near the cut-off frequency. The amplifier stages are accurately set to propose a flat gain response [26]. Multiple distributed amplifiers can work in cascade way in order to acquire more gain. The cascaded single-stage DA (CSSDA) is a structure established to obtain high gain and wide bandwidth [27]. The structure presented in this paper is based on simultaneous usage of Doherty and distributed structures in a power amplifier to benefit from their advantages simultaneously. The power divider designed in the previous section, which has a very wide bandwidth, is also used to divide the input power to achieve a wider bandwidth. To combine the power at the output of proposed amplifier, the power divider designed in the previous section is also used in reverse. Fig. 11 depicts the block diagram of the proposed power amplifier.

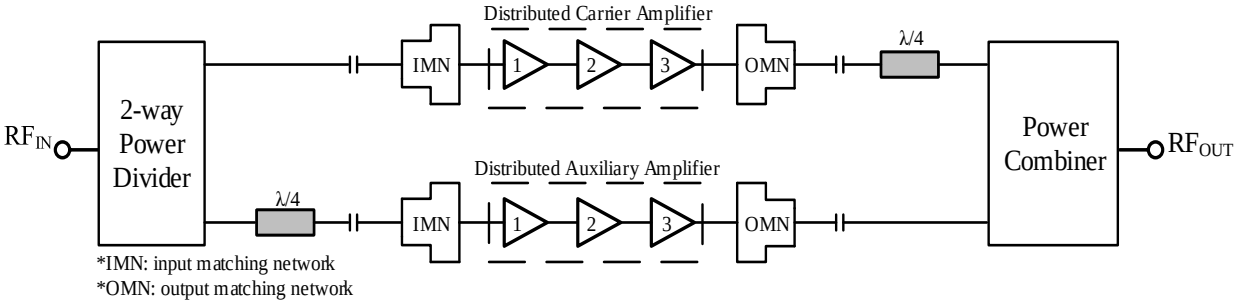


Fig. 11: Introduced structure for PA.

In Fig. 11, the main and auxiliary amplifiers are based on a distributed structure. Based on Fig. 11, each of the main and auxiliary distributed amplifiers is composed of three different parts, represented by 1, 2, and 3, all of which are connected to each other in a cascade manner.

Since the traditional power amplifiers have a high bandwidth but low gain, the tapered cascaded multistage distributed amplifier (T-CMSDA) method was used to improve the gain in the proposed power amplifier (as in reference [28]). Section 1 in Fig. 11 of both main and auxiliary amplifiers has two major tasks: i) matching at the input; and ii) improving the saturation status of the amplifier. In other words, this section functions like a pre-amplifier. Section 1 which is displayed in Fig. 12, is a three-stage distributed amplifier consisting of 6 transistors.

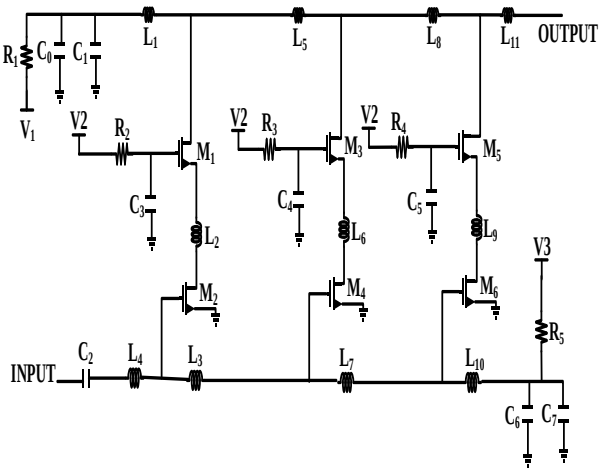


Fig. 12: Schematic view of Section 1.

Section 2 shown in Fig. 13 consists of four transistors, responsible for matching the two sections 1 and 3 and increasing the gain.

Section 3 in

Fig. 14 consists of six transistors linked in a distributed manner functioning as the main amplifier. The amplification job is mainly performed in Section 3 and a small part in Section 2.

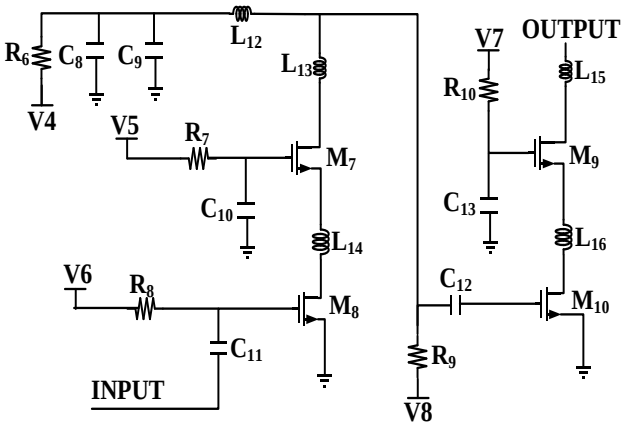


Fig. 13: Schematic view of Section 2

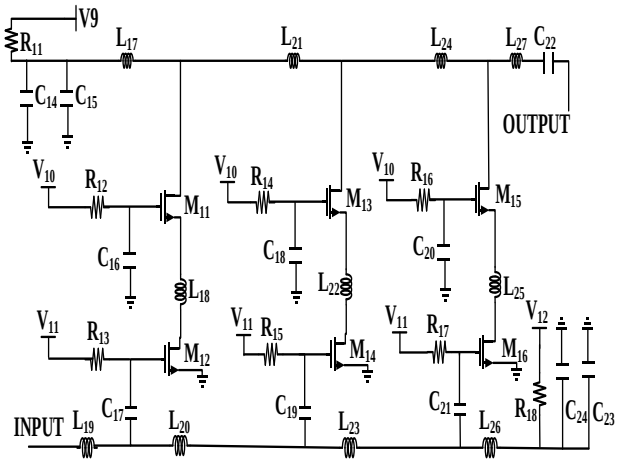


Fig. 14: Schematic view of Section 3.

## Simulation Results

### A. Scattering Parameters

Fig. 15 illustrates the parameter $S_{21}$ for the introduced PA.

It can be observed in Fig. 15 that the proposed circuit gain in this state is 32dB at 30GHz. Over a wide area of the Ka band, i.e. from 26-34GHz, the gain is more than

30dB. The $S_{11}$ or input return losses diagram of designed power amplifier is indicated in Fig. 16.

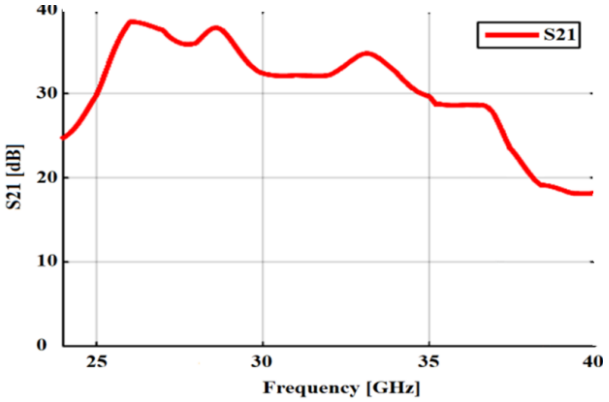


Fig. 15: The $S_{21}$ parameter for the introduced PA.

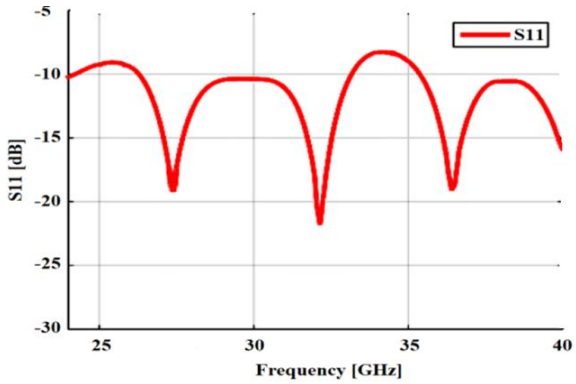


Fig. 16: Input return loss of the proposed PA.

Fig. 16 displays that over the frequency range of 26-40GHz, the parameter $S_{11}$ is below the -8dB. Hence, there is acceptable approximate matching in the input within this frequency range at the input terminal.

The $S_{22}$ or output return loss diagram for the proposed power amplifier is shown in Fig. 17.

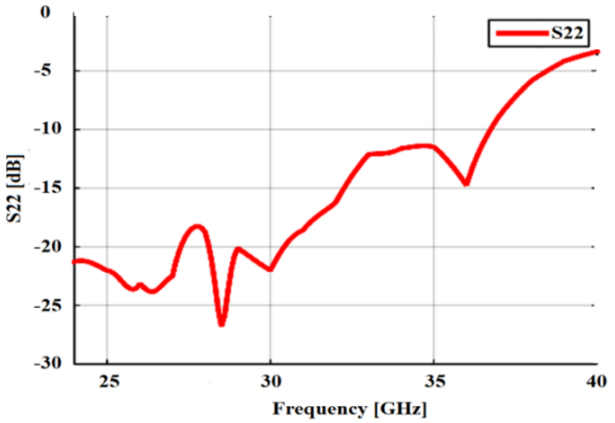


Fig. 17: Output return loss of the introduced PA.

It could be observed in Fig. 17 that over the frequency range of 26-37GHz, the $S_{22}$ parameter is below -10dB; thus, there is acceptable approximate matching within this frequency range at the output terminal.

The $S_{12}$ parameter indicates isolation whose smaller values are more desirable. The $S_{12}$ diagram is shown in Fig. 18 for the designed PA.

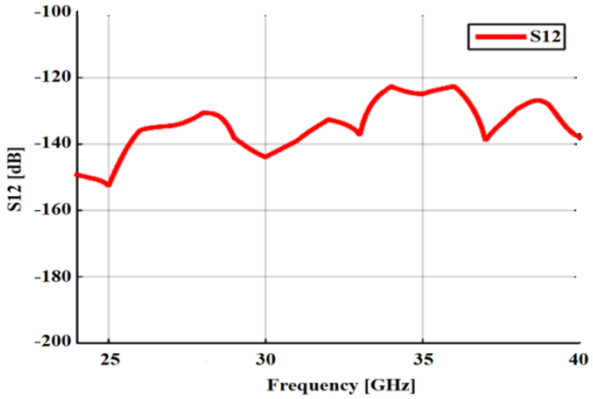


Fig. 18: $S_{12}$ parameter for the introduced PA.

It is observed in Fig. 18 that the isolation in the proposed circuit is less than -120dB for the entire Ka band, which is very good.

*B. Power Added Efficiency (PAE)*

Power Added Efficiency is generally used to analyze the efficiency of a PA under high gain conditions, and is a determining parameter for the RF power amplifiers. The PAE is demonstrated in Fig. 19 in terms of input power, i.e. $P_{IN}$ for designed power amplifier at 26, 30, and 34GHz.

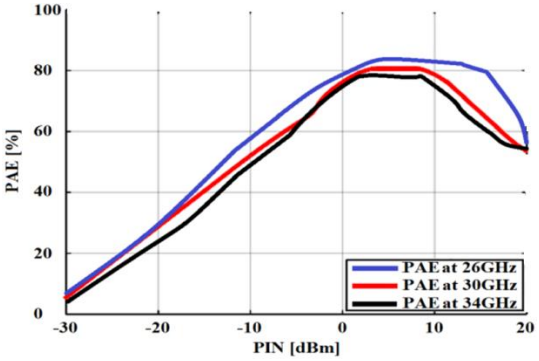


Fig. 19: PAE in terms of input power.

Fig. 19 reveals that at the $P_{IN}$ of 5dB, the power efficiency is at its maximum, about 80%, twice as much as the previous amplifiers.

*C. Gain*

For an ideal linear amplifier, the output power in terms of the input power is a straight line with a slope of 1, where the amplifier gain equals the output to the input power ratio. At a specific range, the amplifier response follows a linear response and then begins to saturate, leading to diminished gain. To determine the range of the linear performance of the amplifier, the 1dB

compression point is defined, at which, changes in the output power are decreased by 1dB compared to the input power. In order to calculate the $P_{1dB}$ point, the gain should be considered for different values of the input power. The point at which the gain is 1dB lower than the primary value, that is the linear gain of the amplifier at low powers, is specified as the 1dB compression point of input power, or $P_{1dB}$ input point. On the other hand, the $P_{1dB}$ output point could be calculated independently of the input $P_{1dB}$ and considering the 1dB compression gain. For this purpose, the gain value should be investigated similarly for different output power values. The point at which the gain is 1dB lower than the primary value, that is the linear gain of the amplifier at low powers, is specified as the 1dB compression point of the output power, or $P_{1dB}$ output point. The gain diagram of the designed power amplifier in terms of input power at 26, 30, and 34GHz is indicated in Fig. 20.

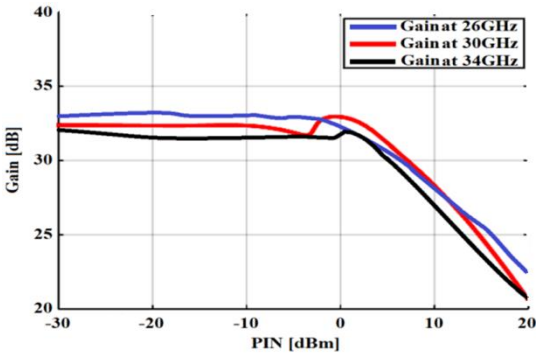


Fig. 20: Gain graph in terms of input power.

It could be observed in Fig. 20 that the $P_{1dB}$ input point of the proposed amplifier is 4dBm at a frequency of 30GHz. Also, the gain value of the proposed amplifier is 32dB at 30GHz.

The diagram of output $P_{1dB}$ point for the introduced PA is illustrated in Fig. 21.

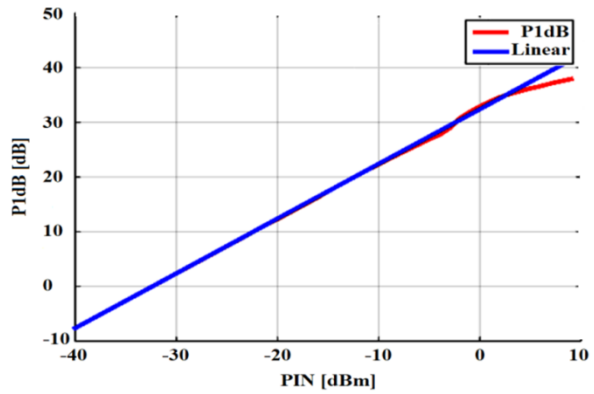


Fig. 21: Output P1dB for the introduced PA.

Fig. 21 depicts the value of $P_{1dB}$ in the introduced PA for the output power of about 35.9dB, which is far greater than that of previous articles.

*D. Output Power*

The output power of the designed PA in terms of the input power at 26, 30, and 34GHz is shown in Fig. 22.

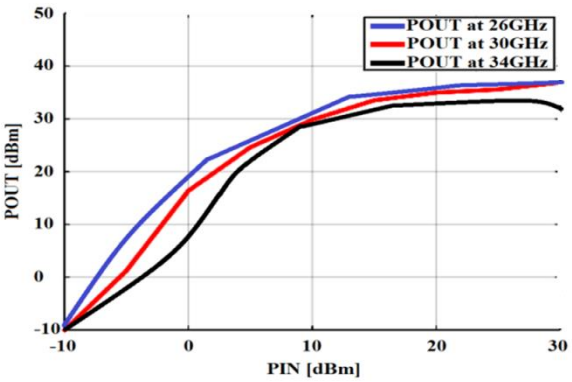


Fig. 22: Output power in terms of input power.

It can be observed in Fig. 22 that the output power of the introduced PA is about 35dBm, which is higher than that of previous articles.

*E. Stability*

With feedback coming from the output to the input, the amplifiers may become unstable. Stability can be achieved through S parameters. The most commonly used definition for stability is the Stern stability factor, which is given as (2):

$$K = \frac{1 + |\Delta| - |S_{11}|^2 - |S_{22}|^2}{2|S_{11}||S_{22}|} \quad (5)$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (6)$$

If the following condition is met, stability is called unconditional. In other words, for each input and output impedance, the PA is stable:

$$K > 1\,, \Delta < 1 \quad (7)$$

Fig. 23 reveals a graph of K drawn based on the Stern stability factor as a criterion for evaluating the stability of the proposed structure.

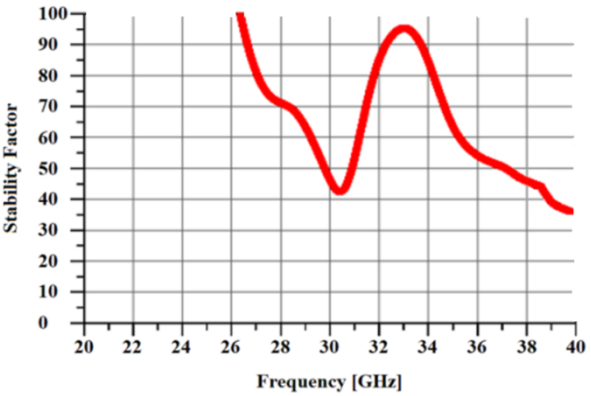


Fig. 23: Graph of K based on the Stern stability factor.

It can be observed in Fig. 23 that the value of K (Stern stability factor) for all frequencies within the range of 26-40GHz is greater than 30. In addition, the value of Δ has calculated using (3) at 26, 30, and 34GHz. The obtained value for Δ in all three mentioned frequencies is less than 1.

Therefore, the proposed power amplifier is unconditionally stable.

*F. IP3*

The relationship between $P_{1dB}$ and IP3 is useful for the third-order nonlinear property, as follows:

$$P_{1dB}=IP3-9.6dB \quad (8)$$

For an amplifier or receiver in the linear performance region, IP3 has a constant value and does not change with increasing input power.

The IP3 for the introduced PA at 30GHz is depicted in Fig. 24.

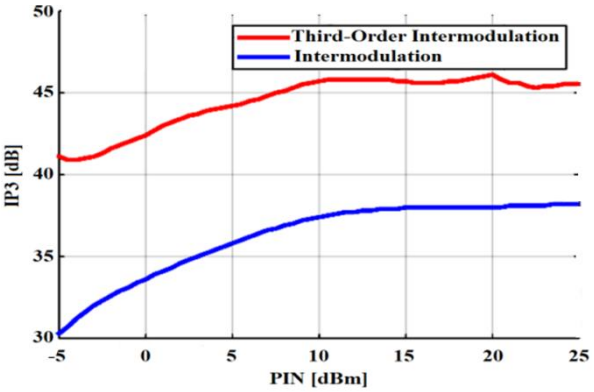


Fig. 24: IP3 for the introduced PA at 30GHz.

It is seen in Fig. 24 that the IP3 value of the proposed amplifier is about 17dB.

A review of the previous articles and their comparison with the current study indicated the advantages of the proposed technique over others as in Table 2.

Table 1: Comparison between the proposed power amplifier with previous articles

| Reference | Frequency (GHz) | Gain (dB) | PAE (%) | Biasing Voltage (Volt) | Technology |
|---|---|---|---|---|---|
| [27] | 40 | 23.4 | 28.5 | - | SiGe |
| [28] | 28.5 | 15 | 37 | 8 | GaAs |
| [29] | 29.5 | 10.5 | 38 | 4 | GaAs |
| [30] | 42 | 7 | 23 | 2.5 | SOI-CMOS |
| [31] | 32 | 22 | 21 | 1 | Bulk CMOS |
| [32] | 70 | 20 | 14 | 1.5 | CMOS |
| [33] | 30 | 15.7 | 35.5 | 1 | CMOS |
| [34] | 28/37/39 | 18.2 | 20.3 | 1.5 | SiGe |
| [35] | 28 | 11.8 | 42 | 4 | GaAs |
| [36] | 1.6-2.6 | 7.6-9.6 | 53-66 | 26 | GaN |
| **This work** | **30** | **32** | **80** | **3.8** | **CMOS 0.18um** |

## Conclusion

This paper introduced a new structure for power amplifiers for operating in Ka band based on applying Doherty and distributed methods in order to benefit from their advantages simultaneously. To design the Doherty power amplifier, first a power divider with a very wide bandwidth, i.e. 1-40GHz, was designed, to cover the entire Ka band. The power amplifier structure presented in this paper was based on Doherty method, which consists of two signal amplification paths, known as main and auxiliary. To amplify the signal in each of the two pathways, a cascade distributed power amplifier was used. The gain of the proposed power amplifier at the frequency of 26-35GHz was more than 30dB. The return losses at the input and output of PA in the entire Ka band was less than -8dB. The maximum PAE of Doherty power amplifier was 80%. The $P_{1dB}$ output point of the proposed power amplifier was 36dB, and the output power of designed power amplifier was also 36dBm.

## Author Contributions

M. S. Mirzajani Darestani introduced all the new structures in the paper and has done all the simulations. In addition, he has done the laboratory tests and prepared the current version of the paper. M. B. Tavakoli and P. Amiri provided scientific and technical advices to the first author and they corrected mistakes during the simulation, laboratory tests, and preparation of the paper process.

## Acknowledgment

The authors acknowledge Islamic Azad University of Arak, for providing scientific resources and laboratory test equipment.

## Conflict of Interest

The authors declare that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism,

informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy, have been completely observed by the authors.

## Abbreviations

| | |
|---|---|
| *PAE* | Power Added Efficiency |
| *DPA* | Doherty Power Amplifier |
| *DA* | Distributed Amplifier |
| *PD* | Power Divider |
| *IMN* | Input Matching Network |
| *OMN* | Output Matching Network |

## References


[1] E. Kaymaksut, D. Zhao, P. Reynaert, "Transformer-Based Doherty Power Amplifiers for mm-Wave Applications in 40-nm CMOS," IEEE Transactions on Microw. Theory and Techniques, 63(4): 1186-1192, 2015.

[2] A. Agah, H. T. Dabag, B. Hanafi, P. M. Asbeck, J. F. Buckwalter, L. E. Larson, "Active Millimeter-Wave Phase-Shift Doherty Power Amplifier in 45-nm SOI CMOS," EEE Journal of Solid-State. Circuits, 48(10): 2338-2350, 2013.

[3] S. C. Cripps, "RF Power Amplifiers for Wireless Communications," 2nd ed. Norwood, MA, USA: Artech House, 2006.

[4] M. Nekovee, "Radio technologies for spectrum above 6 GHz - a key component of 5G," in 5G Radio Technology Seminar. Exploring Technical Challenges in the Emerging 5G Ecosystem, 2015: 1–46, 2015.

[5] A. Gupta, R. K. Jha, "A survey of 5G network: Architecture and emerging technologies," IEEE Access, 3(1): 1206–1232, 2015.

[6] P. M. Asbeck, "Will Doherty continue to rule for 5G," in Proc. 2016 IEEE MTT-S Int. Microw. Symp. (IMS),: 1–4, 2016.

[7] V. Camarchia, M. Pirola, R. Quaglia, S. Jee, Y. Cho, B. Kim, "The Doherty power amplifier: Review of recent solutions and trends," IEEE Transactions on Microw. Theory and Techniques, 63(2): 559-571, 2015.

[8] R. Giofre, P. Colantonio, F. Giannini, "A design approach to ` maximize the efficiency vs. linearity trade-off in fixed and modulated load. GaN power amplifiers," IEEE Access, 6(2): 9247–9255, 2018.

[9] P. Colantonio, F. Giannini, E. Limiti. High efficiency RF and microwave solid state power amplifiers. Wiley, 2009.

[10] R. Nemati, S. Karimian, N. Masoumi, "An Optimized Approach for Design of Three-Section Wilkinson Power Divider," in Proc. 9th international symp. on Telecommunication (IST), Dec. 2018.

[11] S. Wang, L. Sun, G. Wang, Y. Li, Z. Xie, "A 1-4 In-Phase Power Divider for 5G Wireless Communication System," Int. Conf. on Microw. and Millimeter Wave Technology (ICMMT), Chengdu, China, 2018.

[12] S. Ochoa, R. Haro-Baez, I. P. Vizca, "New Design of T-type Power Divider Network in Microstrip Technology for C-Band Downlink," IEEE Microw., Wireless Component Lett., 13(5): 178-180, 2017.

[13] O. Kizilbey, S. Bozdemir, B. S. Yarman, "2-10 GHz Multisection 2-Way Wilkinson Power Divider with Enhanced Port Match and Isolation," IEEE MTT-S Int. Microw. Symp. Dig., Florida, USA,: 1–4, 2017.

[14] M. Chongcheawchamnan, S. Patisang, M. Krairiksh, I. D. Robertson, "Tri Band Wilkinson Power Divider Using a Three-Section Transmission-Line Transformer," IEEE Microw. and Wireless Components Lett., 16(8): 452-454, 2006.

[15] B. Mishra, A. Rahman, S. Shaw, M. Mohd, S. Mondal, P. P. Sarkar, "Design of an ultra-wideband Wilkinson power divider," First Int. Conf. on Automation, Control, Energy and Systems (ACES), Hooghy,: 1-4, 2014.

[16] X. Xu, X. Tang, "Design of an Ultra-Wideband Power Divider with Harmonics Suppression," International Journal of RF and Microw. Computer-Aided Engineering, Wiley Periodicals: 1-6, 2014.

[17] A. Arbabian, A. M. Niknejad, "Design of a CMOS Tapered Cascaded Multistage Distributed Amplifier," IEEE transactions on Microw. theory and techniques, 57(4): 174-178, 2009.

[18] J. Yang, C. Gu, W. Wu, "Design of novel compact coupled microstrip power divider with harmonic suppression," IEEE Microw. Wireless Component Lett., 18(9): 572–574, 2008.

[19] J. Li, Q. Shi-Wei, X. Quan, "Capacitively loaded Wilkinson power divider with size reduction and harmonic suppression," Microw. and Optical Technology Lett., 49(11): 2737-2739, 2007.

[20] A. L. Perrier, J. M. Duchamp, P. Ferrari, "A miniaturized three-port divider/combiner," Microw. and Optical Technology Lett., 50(1): 72-75, 2008.

[21] W. Huang, C. Liu, L. Yan and K. Huang, "A miniaturized dual-band power divider with harmonic suppression for GSM applications," Journal of Electromagnetic Waves and Applications, 24(1): 81-91, 2010.

[22] G. JZ, Y. XJ, S. XW, "A compact harmonic-suppressed Wilkinson power divider using CSCMRC resonators," Microw. Opt. Technol. Lett., 48(2): 2382–2384, 2006.

[23] S. JY, S. C. Huang, Y. H. Pang, Wilkinson power divider incorporating quasi-elliptic filters for improved out-of-band rejection, Electron. Lett., 47(23):1288–1289, 2011.

[24] Z. Zhang, Y. C. Jiao and Z. B. Weng. (2012, June). Design of 2.4GHz power divider with harmonic suppression. Electron. Lett.. 48(12): 705–707.

[25] G. Reza Nikandish, R. Bogdan Staszewski, A. Zhu, "The (R) evolution of Distributed Amplifiers: From Vacuum Tubes to Modern CMOS and GaN ICs," IEEE Microw. Mag, 19(4):66-83, 2018.

[26] M. Gil, J. Bonache, F. Martin, "Synthesis and applications of new left handed microstrip lines with complementary split-ring resonators etched on the signal strip," IET Microwaves, Antennas & Propagation, 2(4): 324–330, 2008.

[27] C. R. Chappidi, X. Wu, K. Sengupta, "A digital mm-Wave PA, architecture with simultaneous frequency and back-off reconfigurability," in Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC),: 328–331, 2017.

[28] D. P. Nguyen, T. Pham, A.-V. Pham, "A Ka-band asymmetrical stacked-FET MMIC Doherty power amplifier," in Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC),: 1–4, 2017.

[29] D. P. Nguyen, J. Curtis, A.-V. Pham, "A Doherty amplifier with modified load modulation scheme based on load–pull data," IEEE Trans. Microw. Theory Techn, 66(1): 227–236, 2018.

[30] A. Agah, H.-T. Dabag, B. Hanafi, P. M. Asbeck, J. F. Buckwalter, L. E. Larson, "Active millimeter-wave phase-shift Doherty power amplifier in 45-nm SOI CMOS," IEEE J. Solid-State Circuits, 48(10): 2338–2350, 2013.

[31] P. Indirayanti, P. Reynaert, "A 32GHz 20 dBm-PS AT transformer based Doherty power amplifier for multi-Gb/s 5G applications in 28 nm bulk CMOS," in Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC),: 45–48, 2017.

[32] E. Kaymaksut, D. Zhao, P. Reynaert, "Transformer-based Doherty power amplifiers for mm-Wave applications in 40-nm CMOS," IEEE Trans. Microw. Theory Techn., 63(4): 1186–1192, 2015.

[33] S. Shakib, H.-C. Park, J. Dunworth, V. Aparin, K. Entesari, "A highly efficient and linear power amplifier for 28-GHz 5G phased array radios in 28-nm CMOS," IEEE J. Solid-State Circuits, 51(12): 3020–3036, 2016.

[34] S. Hu, F. Wang, H. Wang, "A 28GHz/37GHz/39GHz multiband linear Doherty power amplifier for 5G massive MIMO applications," in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,: 32–33, 2017.

[35] Duy P. Nguyen, Binh L. Pham, Anh-Vu Pham, "A Compact Ka-Band Integrated Doherty Amplifier With Reconfigurable Input Network," IEEE transactions on Microw. theory and techniques, 67(1): 234-239, 2019.

[36] J. Xia, W. Chen, F. Meng, C. Yu, X. Zhu, "Improved Three-Stage Doherty Amplifier Design With impedance Compensation in Load Combiner for Broadband Applications," IEEE transactions on microw. theory and techniques, 67(2): 778-786, 2019.

## Biographies

**M.S. Mirzajani Darestani** is Ph.D. student in electronics engineering at Islamic Azad University, Arak Branch. He is the author of more than 15 articles. His research interests are high frequency circuits, gyro stabilized platforms.

**M.B. Tavakoli** is Ph.D. from Islamic Azad University, Science and Research Branch, Tehran, Iran. His main research interest includes electronic circuit design in industries. His primary research interest is in RF and power electronic circuits, with focus on high efficient and high linear power circuit design. He is currently with the Faculty of Electrical Engineering at Islamic Azad University, in Arak, Iran.

**P. Amiri** received his Ph.D. from University Tarbiat Modares (TMU, Tehran, Iran) in 2010, all degrees in Electrical Engineering (electronic). His main research interest includes electronic circuit design in industries. His primary research interest is in RF and power electronic circuits, with focus on high efficient and high linear power circuit design. He is currently with the Faculty of Electrical Engineering at Shahid Rajaee Teacher Training University, in Tehran, Iran.



**How to cite this paper:**
M.S. Mirzajani Darestani, M.B. Tavakoli, P. Amiri, "A 28-36 GHz optimized CMOS distributed Doherty power amplifier with a new wideband power divider structure," Journal of Electrical and Computer Engineering Innovations, 8(1): 85-96, 2020.

**DOI:** 10.22061/JECEI.2020.6992.352

**URL:** http://jecei.sru.ac.ir/article_1425.html