Journal of Electrical and Computer Engineering Innovations
(JECEI)
Journal homepage: http://www.jecei.sru.ac.ir

Research paper

Design of a High-Speed and Low Power CMOS Comparator for A/D Converters

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Article Info

Article History:
Received 14 June 2020
Reviewed 15 August 2020
Revised 25 October 2020
Accepted 27 December 2020

Keywords:
Dynamic comparator
High-speed
Low-power
Bulk driven

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Abstract

Background and Objectives: Comparators play a critical role in the analog to digital converters (ADCs) and digital to analog converters (DACs). Therefore, different structures have been proposed to improve their performance. Power, delay, offset, and noise are the important factors that have significantly affect the comparator's performance. In low power applications, power consumption and delay are the critical concerns that should be minimized to obtain better performance. In this work, a low-power and high-speed comparator has been proposed, which is suitable for applications operating at a low power supply.

Methods: Based on the conventional structure of the comparator, some modifications are implemented to achieve better performance in terms of power consumption and delay. Additionally, the proposed structure gives great performance when the difference of inputs is very small. To verify the proposed structure, it is designed and simulated in a 0.18 µm CMOS technology with a power supply of 1 V and sampling frequency of 2 MHz.

Results: To draw a fair comparison, the conventional and proposed structure is simulated in equal circumstance. The size of transistors is designed with appropriate *W*/*L* ratios to achieve appropriate performance. The proposed structure not only reduces the power consumption by 44%, but also it decreases the delay by 9.1%. The power consumption of the proposed structure is around 0.12 µw. The total occupied area by the proposed structure is approximately 127.44 μm^2.

Conclusion: In this paper, we presented a delay analysis for the proposed dynamic comparator. In addition, based on theoretical analyses, a new dynamic comparator consumes less power and operates faster compared with the conventional structure. The simulation results verify the theoretical analysis.

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Introduction

The comparator [1], [2], [3], [4], [5], [6] is one of the most important blocks in the integrated circuits, which compares two analog inputs and produces digital outputs. Open-loop comparators, regenerative latch comparators, and preamplifier latch comparators are three important architectures of voltage comparators. Each of them is superior to others from the point of view of power consumption, delay, offset, input referred noise [7], and so on. In other words, the high-resolution and high-speed comparator can be achieved by implementing open-loop architectures. Furthermore, the latch comparator is the most useful structure due to its high-speed and low-power consumption.

So, the prominent aspect of the latch-type comparators by comparison with others is its power, particularly at the applications with low power supply. The comparator is a building block in data conversion circuits, including successive approximate register (SAR) [8], [9], [10], [11], Pipeline [12], [13], [14], and Flash [15], [16], [17]. Therefore, the optimal design of the comparator is very important, particularly in terms of power consumption, speed, offset and occupied space on the chip [18], [19], [20], [21].

It should be noted the comparators have a critical influence on the overall performance in analog-to-digital converters. To obtain a high effective number of bits (ENOB), an appropriate comparator is required. As a result, the designers are always looking to achieve the best features of the comparator for special purposes.

In recent years, according to shrinking the feature size of CMOS devices and reduction of the supply voltage (V_{DD}), the power consumption of circuits is diminished, and thereby, the requirement goes toward comparators, which can follow these.

Different structures have been proposed, such as dynamic comparators [22]. However, there is a trade-off between power consumption and speed in low supply voltage of these comparators. In the low supply voltage, they can operate fast.

However, during the two phases, latch and reset phases, the comparator consumes the static current. Therefore, they have a crucial restriction in low-power applications.

To address the problem of dynamic power consumption, a self-reset method is implemented [23]. Moreover, bulk-driven [24], [25], [26] is another technique to improve the speed and power consumption.

However, the technique suffers from lower transconductance (backgate transconductance (g_{mb})) in comparison with its gate-driven counterpart. Furthermore, the popularity of the technique is reduced due to the unique fabrication process.

The comparator with double-tail dynamic structure is presented in [27]. The comparator is designed based on separating the input stage and cross-coupled part. This separation forces comparator to operate fast over a wide input common-mode range and power supply voltage.

In this paper, a new comparator with no additional circuits has been introduced. The proposed comparator is simulated in 180 nm CMOS technology, and exhibits high speed and low-power consumption. Additionally, the delay analysis has been carried out for the proposed structure.

The rest of the paper is organized as follows: the next section is named the proposed comparator, which explains the conventional and proposed structures and analyses the delay. Next, the simulation results are presented and compared with other structures, and finally the last section contains the conclusion of the proposed study.

Proposed structure

Figure 1 shows conventional comparator's schematic with a current source, which input signals are applied to the gate terminal of transistors [28]. The operation of the conventional comparator can be described as follows.

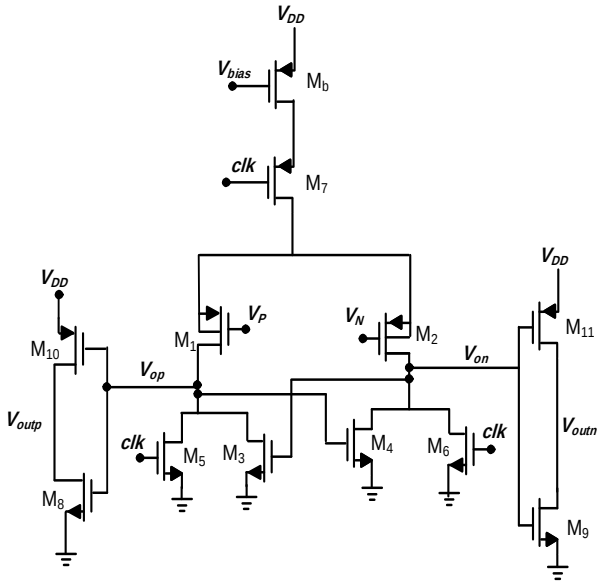

Fig. 1: Schematic circuit of the conventional dynamic comparator.

During the reset phase, when the *clk*=1, transistor M_7 is cut-off, and both points of V_{op} and V_{on} are reset to ground by transistors of M_5 and M_6 to determine an initial condition for the output of the comparator.

Also, the output inverters pull both outputs of the comparator (V_{outp} and V_{outn}) to V_{DD}.

In the comparison phase, when the *clk*=0, the transistors M_5 and M_6 are off, and M_7 turns on. Assuming that $V_P > V_N$, both output point values of V_{op} and V_{on} change according to the differential input voltage. First, the both output points start to decrease until M_4 of cross-coupled nMOS load transistors achieves the turn-on voltage.

In other words, the different voltage between gate and source is higer than the threshold voltage. Then, the output point of V_{on} will continue to discharge to the ground, and at the same moment, the output point of V_{op} will be changed its way and charged to the high level as shown in Fig. 2.

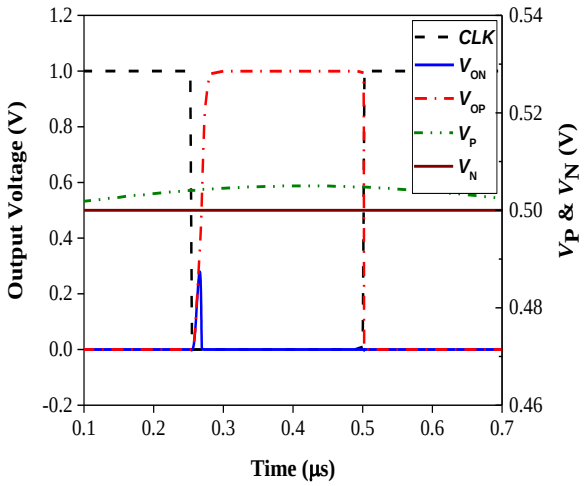

Fig. 2: Transient simulation of the conventional comparator.

The comparator will operate vice versa if V_N is greater than V_P. The total delay of the conventional comparator can be expressed as follows [29]:

$$t_{\text{delay}} = t_0 + t_{latch} \tag{1}$$

where t_0 represents the time for discharging C_L capacitor until the nMOS transistors of M_4 or M_3 turn on.

$$t_0 = \frac{V_{th} \times C_L}{I_{B1}} = \frac{2V_{th} \times C_L}{I_{tail}} \tag{2}$$

where I_{B1} is the drain current of the input transistor. C_L represents the total load capacitance of the comparator, and V_{th} is the threshold voltage of transistor. t_{latch} denotes the latching delay time of the two cross-coupled transistors of inverter and is given by:

$$t_{latch} = \frac{C_L}{g_{m.Total}} \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_l}{g_{m.Total}} \ln\left(\frac{V_{DD}}{2\Delta V_0}\right) \tag{3}$$

where $g_{m,Total}$ is the sum of the transconductance of the differential pair transistors (g_{m1} and g_{m2}) and the transconductance of the cross-coupled nMOS loads. It is assumed that $\Delta V_{out}=V_{DD}/2$, and the ΔV_0 can be obtained as follows:

$$\begin{aligned} \Delta V_0 &= \left|V_{o_p}(t=t_0) - V_{o_n}(t=t_0)\right| \\ &= V_{th} - \frac{I_{B2} \times t_0}{C_L} = V_{th}\left(1 - \frac{I_{B2}}{I_{B1}}\right) \end{aligned} \tag{4}$$

By assuming ΔI_{latch} as (5), the (4) can be rewritten as below:

$$\Delta I_{latch} = |I_{B1} - I_{B2}| = g_{m1.2}\,\Delta V_{in} \tag{5}$$

$$\Delta V_0 = V_{thp} \frac{\Delta I_{latch}}{I_{B2}} \approx 2V_{thn} \frac{g_{m1.2}\Delta V_{in}}{I_{tail}} \tag{6}$$

where ΔV_{in} is the small differential input voltage. Substituting (6) in (3), the total delay of the conventional comparator is obtained as follows:

$$\begin{aligned} t_{\text{delay}} &= \frac{2V_{th}C_L}{I_{tail}} + \frac{C_L}{g_{m.Total}} \ln\left(\frac{V_{DD}}{2\Delta V_0}\right) \\ &= \frac{2V_{th}C_L}{I_{tail}} + \frac{C_L}{g_{m.Total}} \ln\left(\frac{V_{DD} I_{tail}}{4\Delta V_{in} V_{th} g_{m1.2}}\right) \end{aligned} \tag{7}$$

Therefore, there are several parameters that have a significant effect on the delay of the comparator, such as the differential input voltage, transconductance of the input transistors, latch tail current, the capacitance ratio of the output nodes, and transconductance of the intermediate stage transistors.

To address the issues of the delay and power consumption in the conventional comparator, a new structure has been proposed. Figure 3 demonstrates the schematic circuit of the proposed comparator, which consists of two inverters, a current source, and a cross-coupled inverter.

The input signal is applied to gate and body terminals, additionally, a cross-coupled inverter is implemented. These modifications will have a positive effect on the speed and power consumption of the comparator. Moreover, for a given power supply, the speed of the comparator is increased because both g_m and g_{mb} have a significant effect on it.

The operation of the proposed comparator at the reset phase is similar to the conventional comparator. When *clk*=1, M_7 is cut off, and both transistors of M_5 and M_6 are turned on, and the nodes of V_{op} and V_{on} are connected to the ground.

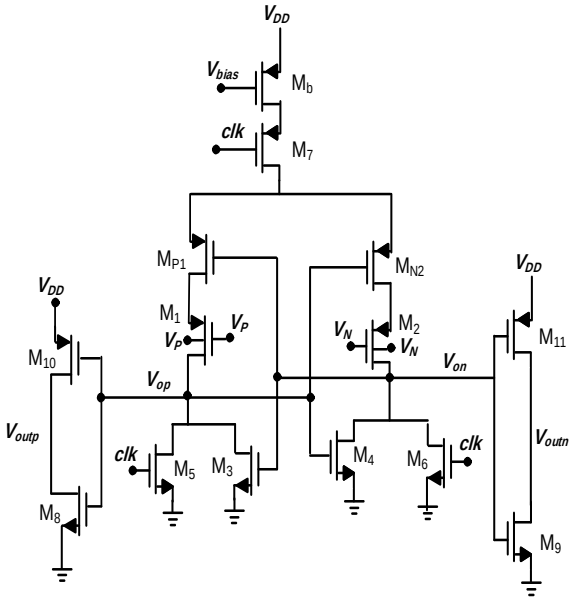

Fig. 3: Proposed dynamic comparator.

Also, at the aforementioned phase, the output nodes of V_{outp} and V_{outn} are charged to the power supply.

As shown in Fig. 3 when *clk* goes low (*clk*=0), the transistor M_7 turns on, and the transistors M_5 and M_6 are cut-off. Therefore, the comparator goes to the comparison phase.

Assume the case that V_P is greater than V_N, both output V_{op} and V_{on} nodes can be started to charge to V_{DD} with different rates according to the differential input voltage. This increment continues until the transistors of cross-coupled achieve the turn-on voltage (V_{gs} >V_{th}). Then, the values of output nodes are determined. The output node of V_{on} will have the same trend and continues to discharge to the ground.

At the same time, the output node of V_{op} will be charged to the power supply.

The final output of the comparator can be obtained by the two inverters. The cross-coupled transistors and the transconductance (g_{mb} and g_m) of the input transistors have a constructive effect on the speed and then the delay of the comparator.

Theoretically, the following equation demonstrates how this structure improves the speed of the comparator.

$$t_{\text{delay}} = \frac{2V_{th}C_L}{I_{tail}} + \frac{C_L}{(g_{mb1.2} + g_{m.Total})}\ln\left(\frac{V_{DD}}{2\Delta V_0}\right) = \frac{2V_{th}C_L}{I_{tail}} + \frac{C_L}{(g_{mb1.2} + g_{m.Total})} \times \ln\left(\frac{V_{DD}\, I_{tail}}{4\Delta V_{in}V_{thn}(g_{m1.2} + g_{mb1.2}))}\right) \quad (8)$$

According to (8), the proposed structure increases the total effective transconductance of the input transistors. As a result, the time constant is reduced, thereby improving the speed of the proposed comparator.

Simulation Results and Discussion

To verify the proposed structure, the simulation results are presented. The proposed comparator is designed and simulated in 180 nm CMOS technology. The simulation results are obtained at V_{DD}=1 V, frequency of 2 MHz, and C_L=10 fF.

The transistors' size is the same in both structures (conventional and proposed structures) to provide a fair comparison.

Moreover, the minimum channel length of all transistors is considered 0.18 µm.

In Table 1, the values of the device parameters are presented. As shown, the size of the input transistors is designed large enough in comparison to other transistors to satisfy a specified offset.

Table 1: Transistor sizing of the proposed comparator

Transistor	*W* (µm)/*L* (µm)
M_1, M_2	3/0.18
M_3, M_4	0.22/0.18
M_5, M_6	0.22/0.18
M_7	1/0.18
M_b	1/0.18
M_{P1}, M_{N2}	0.22/0.18
M_9, M_{10}, M_{11}, M_{12}	0.22/0.18

Figure 4 shows the results of power consumption for the different common-voltage.

The proposed structure's power consumption is decreased remarkably when the common voltage sweeps from 0.4 V to 0.7 V.

However, the conventional comparator exhibits the proper operation at V_{cm}> 0.65 V. Additionally, the delay is decreased in comparison with the conventional structure.

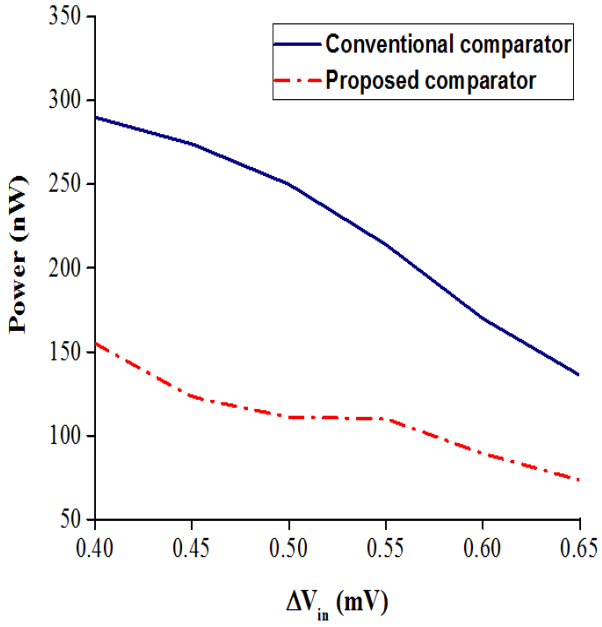

Fig. 4: Power with a different common-mode variation.

As shown in Fig. 5, by increasing the common-voltage, the difference of delays in the conventional and proposed structures becomes more significant. Therefore, the proposed structure presents better performance.

The proposed and conventional comparators are simulated for different input amplitudes to evaluate comparators' operation under this condition.

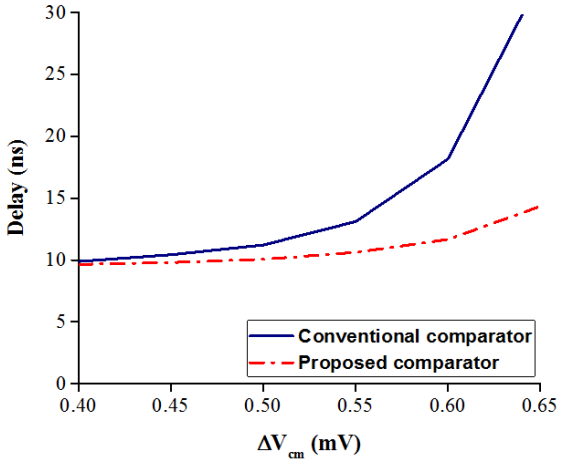

Fig. 5: Delay versus different common-mode variation at ΔV_{in}=0.1 mV.

As shown in Fig. 6, for ΔV_{in}=0.1 mV, proposed comparator's delay is 9.968 ns at V_{DD}=1 V, while the conventional one exhibits the delay of 11.12 ns.

According to the performance of the proposed structure, it is suitable for the applications that have low input amplitude, such as bioelectronics.

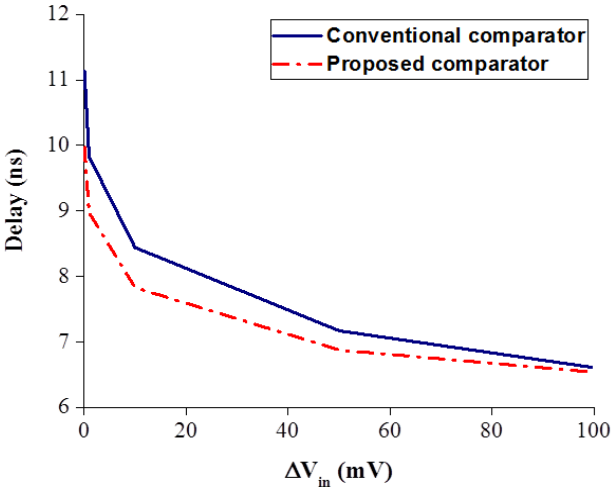

Fig. 6: Delay versus different input amplitude.

Table 2: Performance summary of the proposed mixer and comparison with previous studies

	[21]	[22]	[25]	[28]	[29]	[30]	Conventional Structure	Proposed Structure
CMOS Technology	180 nm	130 nm	65 nm	180nm	180nm	180nm	180nm	180nm
Power Supply (V)	1.2	1.2	1.2	1.2	1.2	1.8	1	1
Sample frequency (MHz)	62.5	1250	-	50	500	1	2	2
Delay (ΔVin=0.1mV) (ns)	1.837	0.1	0.120	3.169	0.55	-	12	9.968
Power (µW)	18.6	600	0.75	23.46	329	130	0.25	0.12
Meas./Sim.	Sim.	Sim.	Sim.	Meas.	Sim.	Sim.	Sim.	Sim.

* Meas.=Measurement
* Sim.=Simulation

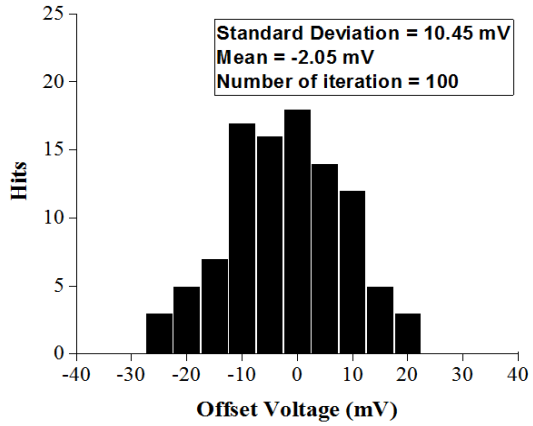

Fig. 7: Monte Carlo simulation of the offset in the proposed dynamic comparator.

Figure 7 illustrates the results of Monte Carlo simulations for a run of 100 samples. The standard deviation of the offset of the proposed comparator is achieved σ=10.45 mV. The value of the offset increases in comparison to the conventional structure by approximately 1 mV. This value is proportional to the backgate transconductance of g_{mb}. Kick back noise of the comparator is another factor should be considered and simulated [18]. At the regeneration phase, the high voltage variations of nodes have a significant effect on the input of the comparator due to parasitic capacitors. The input voltage is disturbed because of the lack of zero output impedance of the preceding stage. To evaluate the kick back noise of the comparator, the circuit as shown in Fig. 8 is implemented.

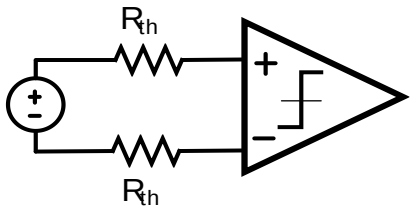

Fig 8: Kick back noise circuit.

The maximum kick back noise which is coupled to the input voltage signal, is 0.28 mV without any compensation.

Moreover, proposed comparator's layout is shown in Fig. 9 that the total active silicon area is 10.8 µm × 11.8 µm.

The performance of the proposed dynamic comparator is summarized in Table 2, and made a comparison with the similar reported works.

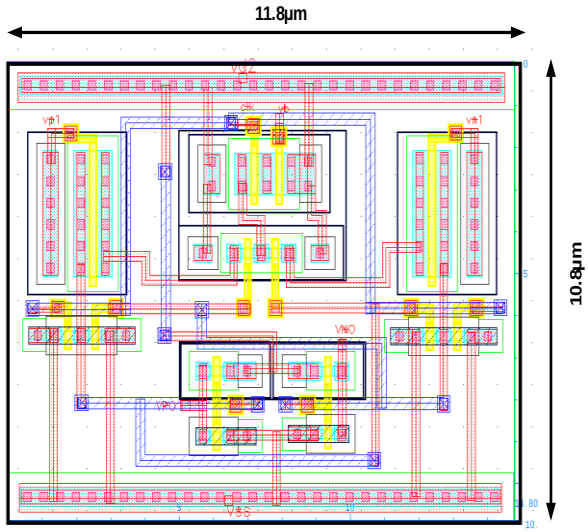

Fig. 9: Layout of the proposed structure.

Conclusion

In this paper, a new structure is proposed for low power and low voltage dynamic comparator. The input signal is applied to bulk and gate terminals.

As a result, both transconductance (g_m) and backgate transconuctance (g_{mb}) contribute to the reduction of delay.

With a power voltage of 1 V and frequency of 2 MHz, simulation results in 180 nm CMOS technology show that the proposed structure is achieved 0.12 µW and 9.968 ns power consumption and delay, respectively.

The proposed comparator not only reduces the power consumption by 44%, but also it has decreased the delay by 9.1%.

Author Contributions

F. Shakibaee and A. Bijari developed the theoretical idea and performed the analytic calculations. F. Shakibaee carried out the simulations. All authors discussed the results and contributed to the final manuscript. A. Bijari and S. H. Zahiri supervised the project.

Acknowledgment

We thank our colleagues from the university of Mashhad (FUM) who provided insight and expertise that greatly assisted the research. We thank R. Lotfi assistance for comments that greatly improved the manuscript.

Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the ethical issues including plagiarism, informed consent, misconduct, data fabrication and, or falsification, double publication and, or submission, and redundancy have been completely witnessed by the authors.

Abbreviations

ADC	Analog to Digital converter
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog converter
ENOB	Effective Number of Bits
SAR	Successive Approximate Register

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How to cite this paper:
F. Shakibaee, A. Bijari, S.H. Zahiri, "Design of a high-speed and low power CMOS comparator for A/D converters," J. Electr. Comput. Eng. Innovations, 9(2): 153-160, 2021.

DOI: 10.22061/JECEI.2021.7602.409

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