Research paper

Realization of Ultra-Compact All-Optical Universal NOR Gate on Photonic Crystal Platform

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Article Info	Abstract
	Background and Objectives: Universal NOR gate is one of the most important gates in digital design. The all-optical NOR gate can be designed using photonic crystals. These types of gates have a small size and can be integrated. **Methods**: In this paper, an optical NOR gate is designed based on 2D photonic crystals. A square lattice has been used to design this structure. This logic gate has two main inputs, a bias input and an output. Because the output of the NOR gate must be "1" for zero inputs, a bias input is required. A combination of linear and point defects has also been used to create waveguides. **Results**: One of the characteristics of this structure is its small size for use in optical integrated circuits. The use of a small number and simple point defects makes the design of this gate easier. The obtained delay time for this gate is 0.06ps. Due to these features, this gate can be used in high-speed optical integrated circuits. **Conclusion**: In this paper, an all-optical NOR logic gate is designed and simulated using photonic crystals. The use of a small number of point defects has reduced the delay time of this gate. The proposed NOR gate can be used in high-speed optical integrated circuits.

Introduction

Transistors are the basis of today's electronic devices used to transmit information. A variety of logic gates are designed using transistors. Logic circuits are also designed using logic gates. Logic integrated circuits that are the basis of computer design are also composed of the same logic circuits. To design high-speed computers, it is necessary to use high-speed transistors. The speed of transistors depends on their dimensions. The smaller the transistors, the faster they will be. Given that the dimensions of transistors have become very small today, it seems that downsizing technology can hardly meet the reduced dimensions of nano-transistors. Therefore, electronic researchers are looking for a new base for computer design. Among the structures used so far, it

seems that photonic crystals are suitable for designing new generation computers due to their properties as a base structure [1], [2].

The reason why this structure has been considered by researchers is that, firstly, these structures are flexible and most circuits used in digital electronics, can be implemented based on photonic crystals. Secondly, due to the fact that light is used in these circuits, the energy-carrying particle is a photon, which has a much higher speed than electrons. Therefore, if the information is transmitted optically, their transmission speed will be higher. Photonic crystals are composed of two materials with different refractive indexes. The refractive index of these two materials is relatively high. These two materials are placed next to each other alternately to

create an alternating structure of two materials with different refractive indexes. The characteristic of these structures is that they prevent the propagation of a continuous range of wavelengths. That is, a continuous range of wavelengths cannot pass through the structure. This range of wavelengths is called the photonic band gap (PBG). If the refractive index distances of the two materials in the photonic crystal increase, the width of the PBG will increase [3]-[5].

Photonic crystals are divided into three categories. These three categories include one-dimensional, two-dimensional, and three-dimensional photonic crystals. In one-dimensional photonic crystals, the structure alternates in one direction. In two-dimensional photonic crystals, the structure is alternating in two directions, and in three-dimensional photon crystals, the alternation will be in three directions. Therefore, three-dimensional photonic crystals restrict light in three directions and are more suitable for use in optical circuits. However, due to the fact that their construction is very complex and the current technology is not widely available for their construction, more two-dimensional photonic crystals are used. Two-dimensional photonic crystals can be created by placing rods with a certain refractive index, in one environment with a different refractive index [6]-[8].

For a two-dimensional photonic crystal to be used as an optical circuit, the wavelength used must be within the PBG range. Therefore, the light wave that radiates from the source to the photonic crystal reflects after hitting the structure. For a light wave to pass through the structure of a photonic crystal, we must create paths for light to propagate through it. These pathways can be created by removing or changing the rods. In other words, by disrupting the alternating structure in a path, light can be directed in that direction. These changes are called defects and the paths in which the defect is created are called waveguides. If one of the bars changes, it is called a point defect, and if some of them change in the same direction, it is called a linear defect. So far, photonic crystals have been used as the base structure for various circuits. One of these circuits is a variety of sensors. Also, different types of fibers are designed using photonic crystals. Photonic crystals can also be used to design a variety of logic circuits [9]-[21].

In the field of logic circuits, Photonic crystals can also be used as a base structure. So far, logic gates such as NOT, OR, AND, XOR and XNOR have been designed and simulated based on photonic crystals [22][23]-[33].

The most important logic gates are NAND and NOR universal gates. Using each of these gates, all logic functions can be implemented. The design of these gates using photonic crystals has been done so far. In some of these structures, the circuit size is large or the delay time is long, which is not suitable for use in high-speed optical integrated circuits. Also, some of them have a lot of defects with high variety, which causes problems during construction [34]-[41]. One of the advantages of these structures in designing various optical devices is their small size and also their ability to design a wide range of devices. The limitation of these structures is their fabrication. The fabrication technology of these structures is not yet complete and so far limited work has been done. Photonic crystals can be used in two structures. In the first structure, the holes in the dielectric substrate and in the second one, dielectric rods in the air are used. The holes in the dielectric substrate is used for the control of electric modes and the rods in the air is used for magnetic modes. In this paper the second structure is implemented. Both types are commonly used in the design of logic gates. In this paper, a low-dimensional, low delay time optical NOR gate is designed and simulated using two-dimensional photonic crystals. In this structure, a square lattice and very few point defects have been used in the design of the proposed NOR gate. Also, the same point defects are considered to have a simple design. According to these features, it can be said that this gate is suitable for use in optically integrated circuits.

NOR Logic Gate

NOR logic gate is one of the universal gates. The universal gate is a gate that can be used to implement all logic functions. The NOR gate is complementary to the OR gate. The output of this gate is only in the "1" mode when all inputs are equal to "0". If one of the inputs of this gate is in the "1" position, the output will be equal to "0". The importance of this gate is because by using this gate alone, all logical gates can be implemented, without using other gates. Figure 1(a) shows the circuit diagram of the NOR gate with two inputs, and Fig. 1(b) shows its accuracy table.
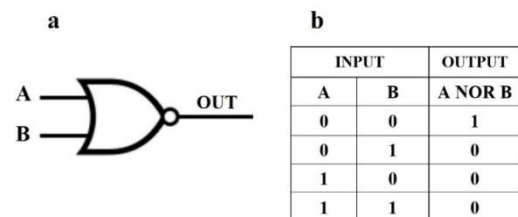

INPUT		OUTPUT
A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

Fig. 1: a) NOR gate circuit diagram and b) its accuracy table.

All-Optical NOR Gate

A photonic crystal structure with a square lattice has been used to design the NOR optical gate. Designing square lattice is easier than other structures. In this structure, several paths are considered for light propagation, which is shown in Fig. 2.

In optical circuits, logic "0" means very low light power, and logic "1" means light power close to the input source in on state. At the optical NOR gate, the

output is in the "1" state, when all inputs are equal to "0". Therefore, when all input sources are off, the output should have optical power close to the "on" source. Therefore, when both inputs are off, there must be an auxiliary source that causes the output to be "1". This input is called the bias input. Figure 2 schematically shows the paths created in the structure to propagate light.
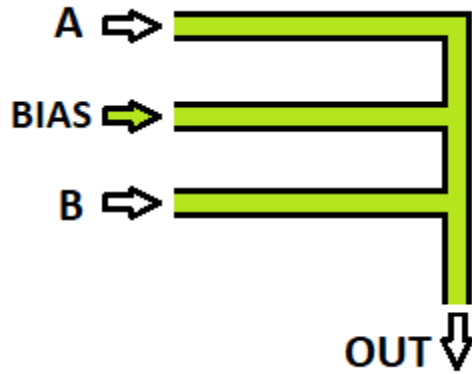

Fig. 2: Light propagation paths for the NOR gate.

The primary photonic crystal structure intended for the realization of the NOR gate consists of silicon rods. The number of these rods is 19 × 13, which are arranged in a square lattice in the air background. Because this structure is designed for a wavelength of 1.55μm, the refractive index of the rods is 3.48 at this wavelength. The air refractive index is also equal to 1. The lattice constant, which is the distance between the centers of adjacent rods, is assumed to be a=0.56μm. The radius of the silicon rods is also equal to r=0.2a.

To simulate the structure, first, the band structure calculations are obtained for the initial structure. In the band structure, the structure behavior is determined for different wavelengths. Figure 3 shows the obtained band structure for the initial structure.
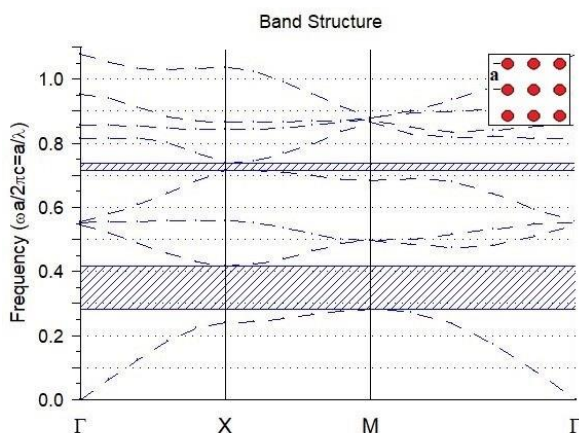

Fig. 3: The band structure for the initial structure.

Figure 3 shows a PBG in the normalized range of 0.28

to 0.42. The wavelength equivalent to this range can be written as 1.33μm to 2μm. Therefore, at this distance from the wavelength, light cannot enter the structure. In order for this structure to be able to direct light in certain directions, the wavelength of light sources must be within the PBG distance. The wavelength used in this simulation is 1.55μm. In the next step, the desired paths for light diffusion are created. For this purpose, the location of input sources is determined first. In this structure, two main inputs are provided for the NOR gate, and one input is provided for the bias input. These paths are created in parallel by removing all the rods. The input paths are then connected using a vertical defect path. One rod at the end of path B is not removed and its radius is changed to $r_d = 0.5r$. Three rods a, b and c in the vertical path are also selected as defect rods. The radius of these rods is also considered as $r_a = r_b = r_c = 0.5r$.

Figure 4 shows the creation of defect paths for the realization of the NOR gate. For better performance of the proposed NOR gate and to increase the distance of the logical values "0" and "1" at the output, the bias source has a phase delay of 130° compared to the two inputs. To create a phase difference between bias signal and input signals, all sources must be coherent and have the same phase. To do this, the input waves must come from the same source. Now, to create a phase difference, the paths taken by these waves must be different. In other words, by adjusting the paths traveled by these light waves, the desired phase difference can be created.
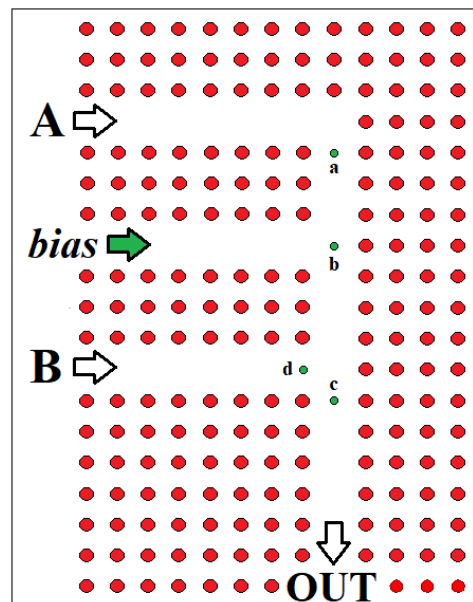

Fig. 4: Proposed structure for optical NOR gate.

Results and Discussion

According to the accuracy table of the two-input NOR gate, four different modes must be analyzed. In the

following, these four modes are analyzed and the distribution of optical power in different paths is obtained for each state. Also, the amount of normalized power at the output is obtained for each of the four input modes. The normalized value is used to calculate the output power. This means that the power of a source in the "on" state is considered as the basis, and the power at the output is calculated relative to that source. Therefore, the minimum optical power will be zero and, the maximum output power will be equal to 1.

State 1(A=B=0): This is the case when both inputs are equal to zero. That is, both input sources A and B are off. In this case, the optical power is emitted from the bias source to the output and causing the output to be in the "1" logic state. Figure 5(a) shows the distribution of optical power in waveguide paths.
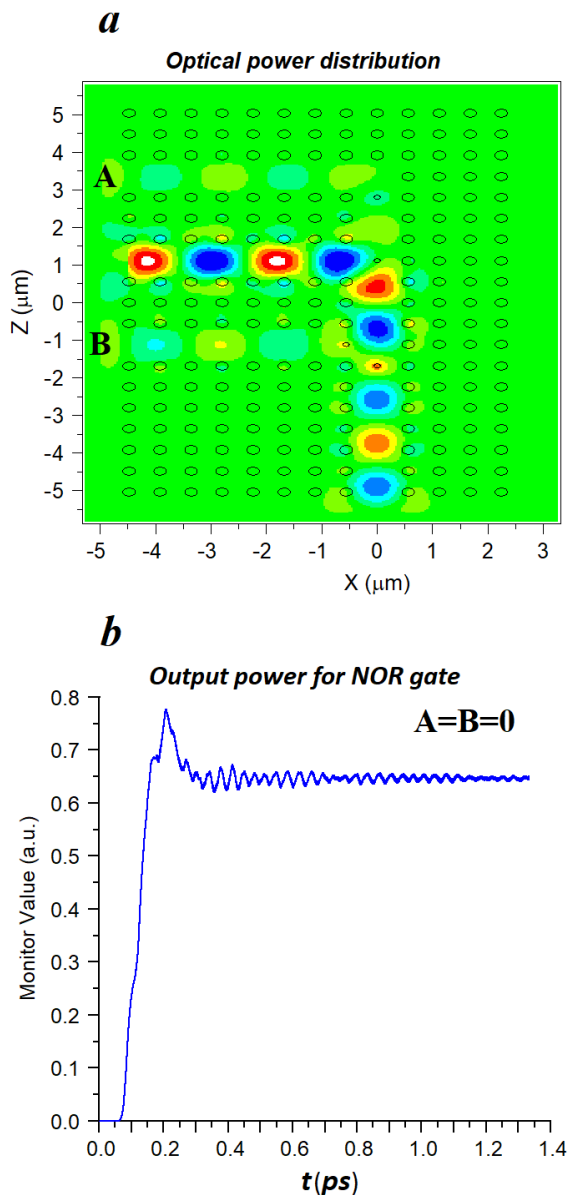
Figure 5(b) shows the amount of normalized power at the output. This figure shows that the amount of normalized power at the output is 0.65. In other words, 65% of the source optical power is transferred to the output, which can be considered as logic "1". The delay time, in this case, is about 0.06ps, as shown in Fig. 5(b). When one or more sources are on, some optical power is reflected in the bias and input paths. The simulation results show that for this case the normalized power reflected the input paths A and B is 0.06 and 0.11, respectively, and also to the bias path is 0.01.

State 2(A=0, B=1): In this case, where only one of the inputs is on, the output is expected to be in the "0" state.

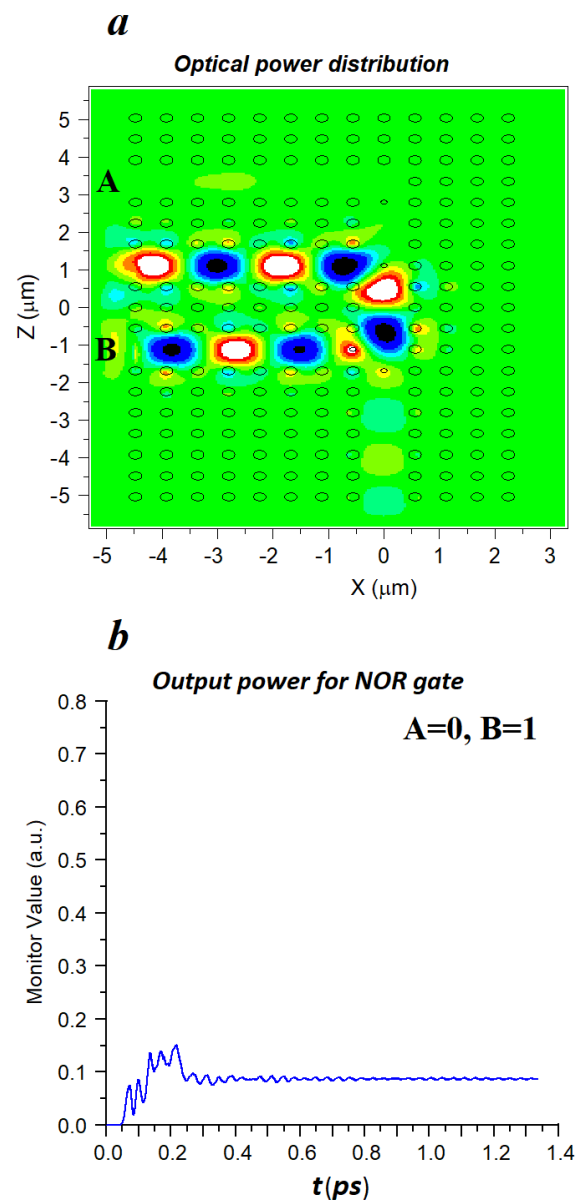Fig. 5: a) Optical power distribution and b) Normalized optical power for A=B=0.

Fig. 6: a) Optical power distribution and b) Normalized optical power for A=0, B=1.

Figure 6(a) shows that in this case the output power distribution in the output path is very low. In this case, the propagating waves from source B and the bias source at the point of collision of the waveguides, interfere in such a way that the amplitude of the output waves is reduced due to the phase difference. Some of the optical power is also reflected to the input paths.

Figure 6(b) shows that in this case (A = 0, B = 1) the normalized power at the output is 0.08. This value can be considered as a logical "0".

The normalized power reflected in the A input, in this case, is zero. While the optical power reflected the B input is 0.27. Also, this power at the bias input is about 0.1.

State 3(A=1, B=0): In this case, as in case 2, only one input source is on. The simulation results show that the optical power distribution in the output path is very low. Light waves from two sources, bias and source A, are attenuated at the point of collision and the power emitted to the output is low. Figure 7(a) shows the optical power distribution in this case.

Time calculations for this situation show that the normalized power propagated to the gate output is 0.09. This amount of power at the output is equivalent to the "0" logic state. The output power diagram, in this case, is shown in Fig. 7(b). In this case, the normalized power reflected the input paths A and B is 0.3 and 0.01, respectively, and also to the bias path is 0.08.
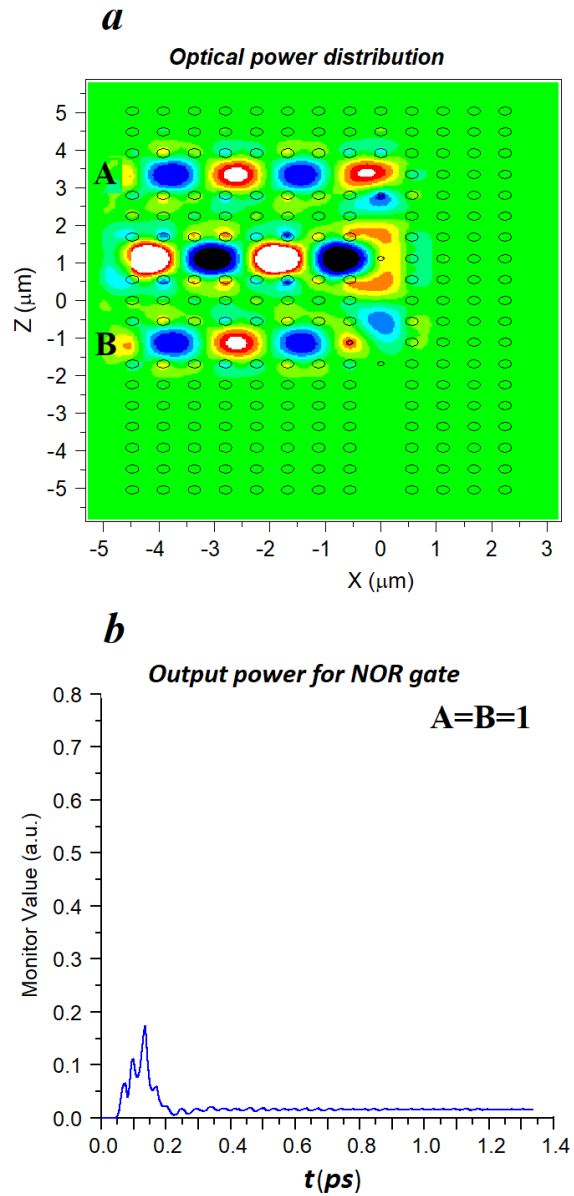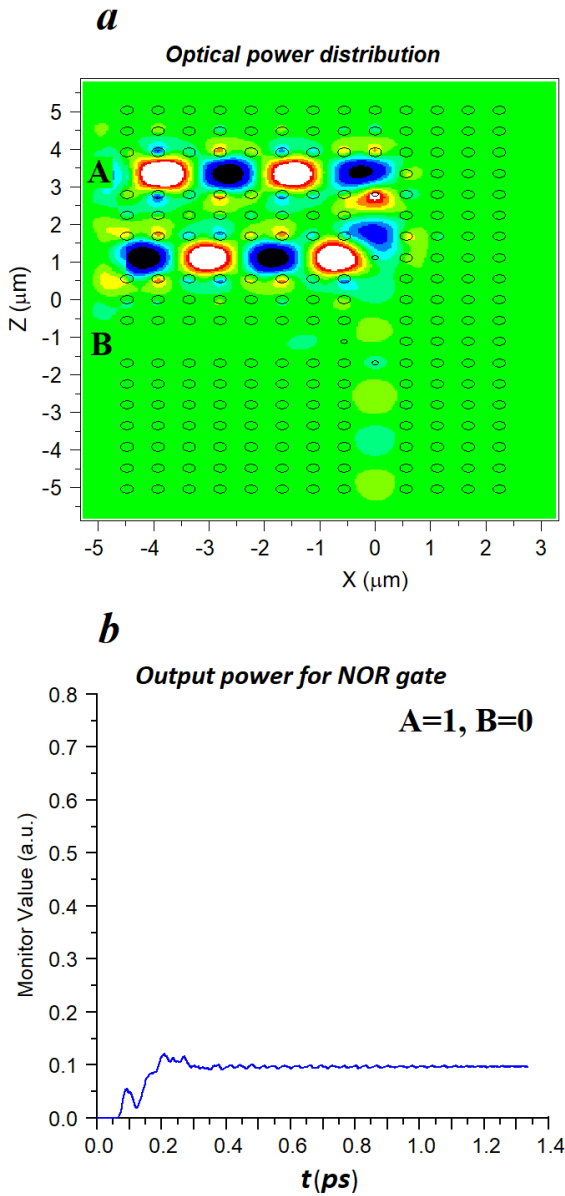

Fig. 7: a) Optical power distribution and b) Normalized optical power for A=1, B=0.

Fig. 8: a) Optical power distribution and b) Normalized optical power for A=B=1.

State 4(A=B=1): When both input sources are on, according to the accuracy table, the output is expected to be zero.

The simulation results are shown in Fig. 8. Figure 8(a) shows the optical power distribution in waveguides. This diagram shows that the emitted waves from the two input sources are attenuated in the event of a bias source wave. Some optical power is also reflected in the input paths.

The emission power to the output is very small in this case.

The normalized optical power at the output is equal to 0.02 in this case, which is equivalent to a logical "0". The output power diagram is shown in Fig. 8(b).

The simulation results show that in this case the amount of normalized power reflected to A and B inputs, is 0.12. Also, this power is calculated to be 0.28 in the bias path.

All the different input modes and their equivalent output power as well as their equivalent logic values are given in Table 1.

According to Table 1, it can be said that the output of the designed gate will be equal to "1" only when both inputs are off. In other words, the output will be "1" when both inputs are in the "0" position. This behavior is the same as the NOR gate function.

Table 1: Optical power at the output

Input		Output power(Logic)
A	B	
0	0	0.65 (1)
0	1	0.08 (0)
1	0	0.09 (0)
1	1	0.02 (0)

The results show that this gate has a small amount of power in the "0" mode. The worst value for logical "0" is 0.09. The normalized optical power in logic "1" mode is also equal to 0.65.

It can be seen that this gate has a low "0" and its value of "1" is relatively high. Therefore, the difference between the two logic levels is acceptable, and this causes the correct detection of logic values at the output, and thus reduces the detection error at the output.

To illustrate the strengths of the proposed optical gate, a number of recently designed structures are listed in Table 2. Important parameters in optical logic gates including size, values of logic levels, and delay time for each of these papers have been investigated and compared with the proposed work.

Table 2: Compare the proposed NOR gate with previous works

Reference	Footprint (μm^2)	"0" Max power	"1" Min power	Delay Time (ps)
[32]	202	0.35	0.75	0.07
[35]	134	0.06	0.58	0.10
[37]	144	0.20	0.51	0.07
[38]	104	0.13	0.62	0.10
[40]	129	0.43	0.60	-
This work	68	0.09	0.65	0.06

According to Table 2, it can be seen that the proposed structure has a very small size compared to previous structures, which makes it suitable for use in optically integrated circuits. The footprint of the designed structure is 68μm^2. Also, the distance between two logical values has been improved so that in this gate, the bit detection error in the output will be reduced. In some previous structures, ring resonators have been used, which complicates the structure and causes problems in fabrication.

Ring resonators also increase the gate delay time. In some other structures without ring resonators, the number of point defects is large and unequal, which also causes problems in their design. The proposed gate does not use ring resonators and also the number of point defects is very small and they are all the same. Therefore, this gate is designed using a simple structure. Another advantage of this structure is its very low delay time, which is due to the use of a small structure. The delay time has also been reduced due to the use of simple defects. The obtained delay time in this structure is equal to 0.06ps.

Low delay time at this gate will increase the data bit rate (BR). Therefore, this optical gate is suitable for use in small and integrated circuits with high speed.

Conclusion

In this paper, an all-optical NOR logic gate is designed and simulated using photonic crystals. The purpose of designing this structure is to use it in high speed optical integrated circuits. For this purpose, its size has been chosen as small as possible. The footprint of the designed NOR gate is 68μm^2. In the design of this gate, simple linear and point defects have been used. The use of a small number of point defects has reduced the delay time of this gate. Another feature of this gate is that the optical power distance is relatively large for high and low logic values. Due to these features, this gate can be used in high-speed and low-error optical integrated circuits.

Author Contributions

F. Parandin designed, simulated, carried out the data analysis, collected the data and interpreted the results and wrote the manuscript.

Acknowledgment

Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

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