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Research paper

A High Voltage Isolated Pulse Generator using Magnetic Pulse Compression and Resonant Charging Techniques for Dielectric Barrier Discharge Applications

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Abstract

Background and Objectives: Dielectric Barrier discharge (DBD) is a suitable method to generating Non-thermal plasma at atmospheric pressure, which utilizes Pulsed power supplies as exciters. Increasing pulse voltage range and frequency and compactness are important issues that should be taking into consideration.

Methods: The high voltage pulse generators which are introduced in the literature have some disadvantages and complexities such as need of additional winding to reset the transformer core and operating under hard switching which increases electromagnetic noise and loss. The leakage inductance of the high voltage transformer increases the rise time of the pulse which is undesirable for DBD applications. The energy stored in the leakage inductance causes the voltage spike across the switch, witch necessitates the use of snubber circuits. The main contribution of this paper is a new high voltage pulse generator with the following characteristics, 1) a capacitor is paralleled with the main switch to reset the transformer core and to provide the soft switching condition for the switch. 2) The resonant charging technique is used which doubles the secondary winding voltage which reduces the turns ratio of high voltage transformer for a certain output pulse peak. 3) The sharpening circuit using magnetic switch produces a sharp high voltage pulse.

Results: The proposed high voltage pulse generator is designed and simulated using Pspice software. To verify the theoretical results, a prototype with the input voltage 48 V, the output voltage pulse 1.5 kV, and the rise time of the output pulse 50 ns is constructed and tested.

Conclusion: This paper proposes a new pulse generator (PG). The proposed PG uses three techniques named forward, resonant charging, and magnetic switch to produce a high-voltage nanosecond pulse. The resonant charging double the secondary voltage of the pulse transformer, which causes reduction in turn ratio of the pulse transformer and decreases the weigh, volume, and price of the PT. The magnetic switch section finally produces a nanosecond high-voltage pulse. The magnitude of the output pulse can be varied using the input source voltage, the MS reset current and the duty cycle. The core of the pulse transformer resets by using a capacitor paralleled with the switch and the PG does not need any additional reset winding like the conventional DC-DC forward converter.

Introduction

Dielectric barrier Discharge (DBD) is an applicable technology for generating Non-thermal plasma at atmospheric pressure.

Non-thermal plasma has various industrial applications such as ozone formation, exhaust gas treatment, surface modification of materials, engine ignition systems and so on [1]-[10]. At first, high voltage ac power supplies were used to excite DBD reactors. But DBD generated by an AC source of periodic sine waves has a relatively low energy input [11], [12]. With the development of semiconductor devices, high voltage pulsed power supplies replaced by ac power supplies for DBD excitation [13]-[16]. Many studies have shown that output pulse parameters of pulsed power supplies like voltage amplitude, rise time and pulse width affect significantly the quality of plasma generated by DBD [17]-[19]. The pulse amplitude is in order of KV, depending on the load requirements. As the pulse rise time decreases, electric field intensity increases in a short time in air gap and produces the higher energy electron to excite and ionize gas molecules [20].

In [21]-[23], three non-isolated solid state pulse generators (PGs) are presented with the combination of pulse forming network (PFN) and boost converter using many MOSFETs switches, capacitors, and inductors. The boost converters provide the initial voltage conditions for the PFNs capacitors. A non-isolated pulse generator is proposed in [24] to produce the high-voltage square waveform. The peaking switch is a serried combination of the low voltage switches. Moreover, the proposed converter needs a high voltage power supply at the input side. A non-isolated solid state pulse generators is presented in [25] using buck-boost technique to provide unipolar and bipolar high-voltage output pulses. The significant mentioned merit of the proposed PG is that the peaking switch tolerates the half of the output pulse voltage magnitude. A combination of a solid-state Marx generator along with the MPC network is proposed in [26] with six IGBTs, three diodes, and two magnetic switches. A boost inverter non-isolated based pulse generator is presented in [25] to produce the bipolar high-voltage pulses. Generally, the non-isolated solid state pulse generators need too many solid-sate switches to control the maximum voltage stress across the switches, which increases complexity and cost and decreases reliability.

Moreover, the magnitude of the output pulse voltage is limited because the voltage stress across the switches is comparable with the peak of the output pulse voltage. The pulse transformer applied with solid state pulse generators has several merits such as establishing the galvanic isolation between the input and output lines, reduction of the maximum voltage stress across the switches, using the low voltage source at the input line, and makes the switch gate driver simpler. In [27], a modular isolated pulse generators is proposed using full bridge multilevel technique. In addition, another modular solid state pulse generators is presented in [28] with the buck chopper technique. In the modular strategies, each module is independent in terms of power supply and pulse generation; therefore, too many components are required. These modular pulse generators are reasonable in the view of the price and complexity for high power application. A compact unipolar nanosecond pulse generator is presented in [29] for DBD applications with two inductors, three capacitors, a pulse transformer and magnetic switch. An isolated PG is presented in [30] with the parallel resonant technique using a transformer, four switches, two capacitors, and a magnetic switch.

This paper proposes a PG with forward technique. The conventional DC-DC forward converter needs an additional winding with complexity to reset the transformer. The proposed PG employs a capacitor paralleled with the switch to reset the transformer. The high-voltage pulsed capacitor is resonantly charged using the leakage inductance of the pulse transformer maximum to twice the secondary winding voltage, which decreases the turn ratio of the pulse transformer, volume and weight, also the efficiency increases. The energy stored in the leakage inductance of the transformer is lost in the resistor-capacitor-diode (RCD) clamp circuit in [15], [16] but the proposed PG employs it beneficially. Moreover, the switch of the PG operates under the low voltage condition.

Modes Analysis of the Proposed PG

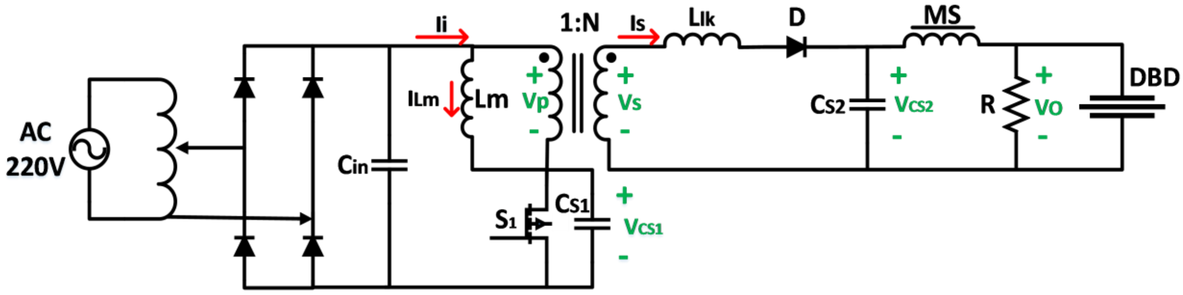

Fig. 1: The Proposed high voltage pulse generator

Fig. 1 shows the structure of the proposed forward pulse generator. As shown, the proposed PG includes a pulse transformer (PT) modeled by the magnetizing inductance Lm and ideal transformer by the turns ratio 1:N and the leakage inductance L_{lk}, the switch S_1, the capacitor C_{S1} for resetting the PT, the high-voltage diode D, the high-voltage capacitor C_{S2}, the magnetic switch (MS), and the resistor R used to stabilize the output waveform. When the switch S_1 is turned on, the low voltage V_i is stepped up by the pulse transformer and the capacitor C_{S2} is resonantly charged maximum to twice the peak voltage of V_S. After the capacitor C_{S2} is fully charged, the magnetic switch is opened and the output pulse voltage with the fast rise time is established. Two main modes is identified for the proposed PG, which is analyzed in details, and the key waveforms are considered.

A. Capacitor Charging (C_{S2}) Mode

This mode begins when the switch S_1 is tuned on. At the low voltage side, the voltage V_i is placed on the primary winding of PT and as shown in Fig. 2 the magnetic inductance L_m is charged as the following equation:

$$i_m(t) = i_m(t_0) + \frac{V_i}{L_m}(t - t_0) \quad (1)$$

At the high voltage side, the voltage V_i is converted to the high voltage Vs through the PT. The model of this mode to analysis the high voltage section is shown in Fig. 3. During this mode, as shown in Fig. 2, the high voltage capacitor C_{S2} is charged resonantly as follows:

$$v_{CS2}(t) = V_s(1 - \cos(\omega(t - t_0)) \quad (2)$$

where ω is the resonant frequency of the resonant charging and is obtained as follows:

$$\omega = \frac{1}{\sqrt{L_{lk}C_{S2}}} \quad (3)$$

Moreover, the current i_S flowing the resonant circuit is achieved as follows:

$$i_S(t) = V_s\sqrt{\frac{C_{S2}}{L_{lk}}}\sin(\omega(t - t_0)) \quad (4)$$

From (4) and Fig. 2 the maximum peak current following the diode D is given as follows:

$$I_{sm} = V_S\sqrt{\frac{C_{S2}}{L_{lk}}} \quad (5)$$

The charge time of the capacitor C_{S2} as shown in Fig. 2 is obtained as follows:

$$T_{ch} = \pi\sqrt{L_{lk}C_{S2}} \quad (6)$$

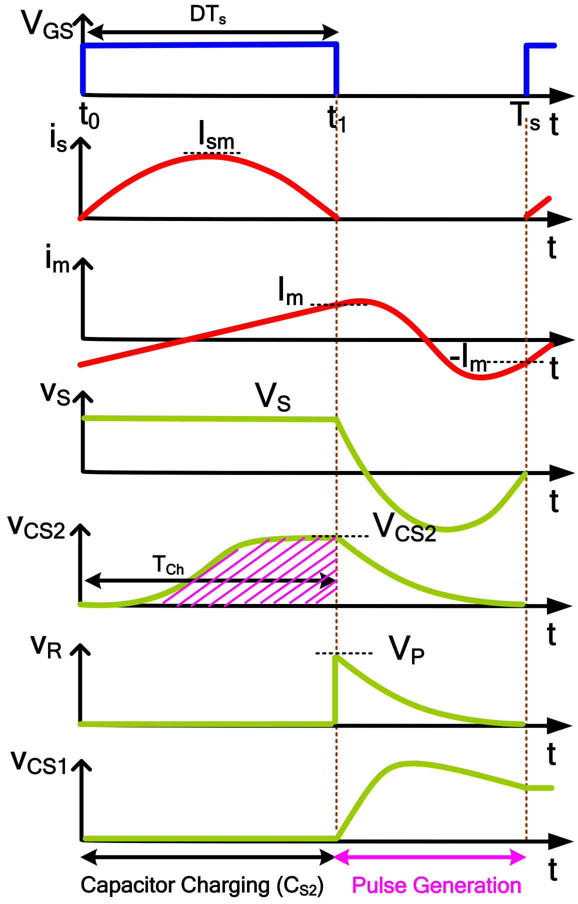

Fig. 2: The proposed PG key waveforms. (a) Capacitor charging (C_{S2}). (b) Pulse generation.

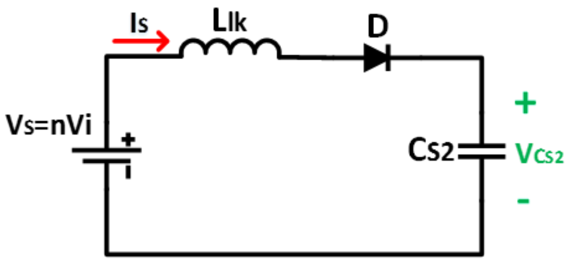

Fig. 3: The model for analyzing of the proposed forward PG in capacitor charging (C_{S2}) mode.

As shown from Fig. 2, the maximum voltage of the capacitor C_{S2} is equal to $2V_S$, therefore the turns ratio of the PT can be reduced. This event can save the copper and reduce the volume and weight of the PT. The equivalent circuit of this mode is illustrated in Fig. 4a.

B. Pulse Generation Mode

When the charge of the capacitor C_{S2} begins at t_0, by neglecting the leakage current of the MS, the whole voltage of V_{CS2} is placed across the MS. The flux density of the MS core changes as follows:

$$B_{MS}(t) = B_{MS}(t_0) + \frac{1}{N_{MS}A_{MS}}\int_{t_0}^{t_0+T_{ch}} v_{CS2}(t)dt \quad (7)$$

where N_{MS} and A_{MS} are the turns ratio and the cross section of the MS respectively as shown in Fig. 6a. In this circuit a reset circuit can be used to adjust the term $B_{MS}(t_0)$. The integral term of (7) is equal to the below area of the voltage V_{CS2} from t_0 to t_1, as shown in Fig. 2.

At the end of the previous mode, the flux density of the MS reaches to the saturation flux density and the MS is saturated. The value of this inductance is small and the circuit model of this mode at the high voltage side is shown in Fig. 4b.

The differential equation of the current i_{MS} is obtained as follows using KVL inside the circuit shown in Fig. 4b:

$$\frac{d^2 i_{MS}}{dt^2} + \frac{R}{L_s}\frac{di_{MS}}{dt} + \frac{1}{L_s C} i_{MS} = 0 \tag{8}$$

The damping factor (DF) of (8) is defined as follows:

$$\xi = \frac{R}{2}\sqrt{\frac{C_{S2}}{L_S}} \tag{9}$$

Based on the value of the DF, there are three answer categories for the equation (8). The following equations are related to the over damped condition ($\xi > 1$):

$$i_{MS} = A_1 e^{-s_1 t} + A_2 e^{-s_2 t} \tag{10}$$

$$s_1 = -\omega(\xi + \sqrt{\xi^2 - 1}) \tag{11}$$

$$s_2 = -\omega(\xi - \sqrt{\xi^2 - 1}) \tag{12}$$

$$A_1 = \frac{1}{s_1 - s_2}\frac{V_o}{L_s} \text{and } A_1 = -A_2 \tag{13}$$

The equations related to the critically damped condition ($\xi = 1$) are given as follows:

$$i_{MS} = (A_3 t + A_4)e^{-\omega\zeta t} \tag{14}$$

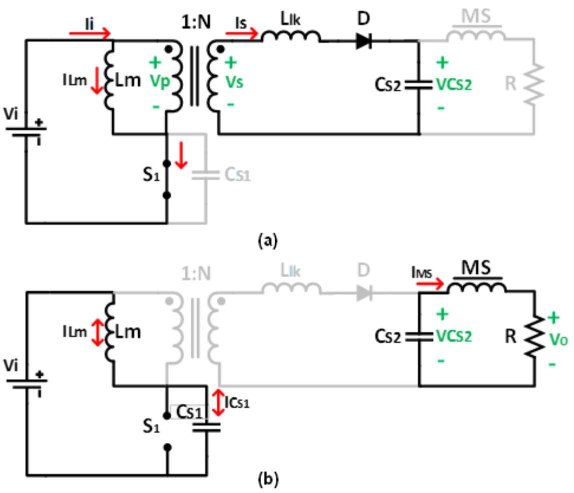

Fig. 4: The equivalent circuit for each operating mode of the proposed forward PG. (a) Capacitor charging (C_{S2}) mode, (b) Pulse generation mode.

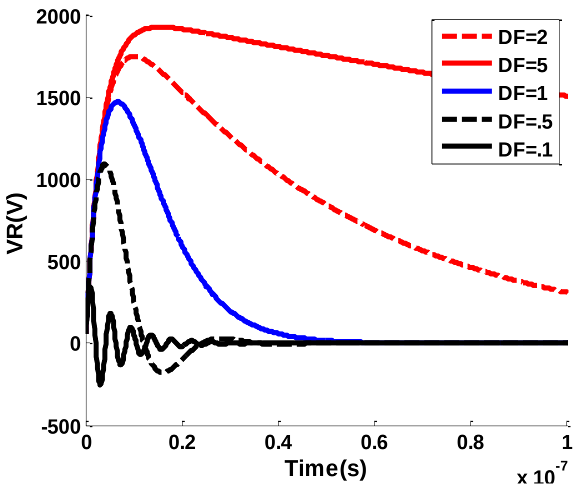

Fig. 5: The waveform of the voltage V_R versus time with Vo=2kV, Ls=1uH, and R=300 ohms, based on the various damping factor (DF).

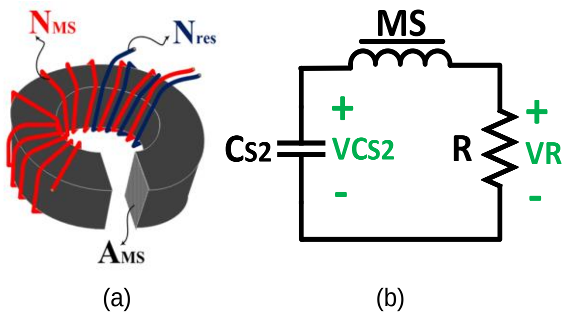

Fig. 6: (a) The image of the magnetic switch, (b) The equivalent circuit of the magnetic switch section.

$$A_3 = \frac{V_o}{L_s} \text{and } A_4 = 0 \tag{15}$$

The following equations are related to the underdamped condition ($\xi < 1$):

$$i_{MS} = A_5 e^{-\omega\zeta t}\cos(\omega_d t) + A_6 e^{-\omega\zeta t}\sin(\omega_d t) \tag{16}$$

$$A_3 = \frac{V_o}{\omega_d L_s} \text{and } A_5 = 0 \text{ and } \omega_d = \omega\sqrt{1-\xi^2} \tag{17}$$

Figure 5 shows the voltage V_R corresponding to the various DF using (10), (14), and (16). As shown, when the DF increases for a certain V_R, L_S, and R, the peak value of the output pulse V_R increases at the cost of increasing the fall time of the V_R.

Moreover, by decreasing the DF, the oscillations appears on the V_R waveform. The magnetic switch in the critical damping has a fast fall time without any oscillation. Based on the load requirements, the DF can be adjusted.

At the low voltage side, the magnetizing inductance Lm establishes a resonant circuit with the input voltage V_i and C_{S1}.

The following equations are determined for both i_i and V_{CS1}.

$$v_{CS1}(t) = V_i(1 - \cos(\omega_i(t - t_1))) + \frac{I_m}{C_{S1}\omega_i} sin(\omega_i(t - t_1))) \tag{18}$$

$$i_i = C_{S1}\omega_i(\frac{I_m}{C_{S1}\omega_i}\cos(\omega_i(t - t_1)) + V_i sin(\omega_i(t - t_1))) \tag{19}$$

where I_m is the current of i_i at t_0 and the ω_i is given as follows:

$$\omega_i = \frac{1}{\sqrt{L_m C_{S1}}} \tag{20}$$

During this mode, the current of I_m is reversed, from (1) the following equation is determined as follows:

$$I_m = \frac{V_i T_{ch}}{2L_m} \tag{21}$$

During this mode, the PT core becomes reset using C_{S1}. The conventional forward DC-DC converters employ an additional winding to reset the transformer, which makes the circuit complex.

Design Procedure of the Proposed PG

By considering the roles of the magnetic pulse compression, resonant charging circuit and the PT, the turns ratio of the PT is designed as follows:

$$N = \frac{K_1 V_P}{2V_i} \tag{22}$$

where from Figure 2, V_P is the peak of the output voltage pulse, and K_1 is defined as follows:

$$K_1 = \frac{V_{CS2}}{V_P} \tag{23}$$

The K_1 coefficient is related to the magnetic pulse compression and is dependent on the DF. For example, for the over damping condition the value of K_1 is one.

By considering the fixed values for the load resistance R and the saturation inductance Ls, for a certain DF, the capacitor C_{S2} is determined as follows:

$$C_{S2} = (\tfrac{2\zeta}{R})^2 L_s \tag{24}$$

According to Fig. 2, and using equations (2) and (7), the following equation is given for the magnetic switch:

$$N_{MS}A_{MS} = \frac{T_{ch}V_s}{2\Delta B} = \frac{T_{ch}NV_i}{2\Delta B} \tag{25}$$

By choosing a core with a certain cross section, the turns of the MS is obtained. The flux density of the MS core can be adjusted using a reset circuit.

The current stress of the switch S_1 and diode D are achieved from (4) as follows:

$$I_{Dmax} = V_s\sqrt{\frac{C_{S2}}{L_{lk}}} \tag{26}$$

$$I_{S1max} = NV_s\sqrt{\frac{C_{S2}}{L_{lk}}} \tag{27}$$

The voltage stress of the diode D and the switch S1 is given as follows:

$$V_{Dmax} = 2V_s \tag{28}$$

$$V_{S1max} = \max(V_{CS1}) \tag{29}$$

From (21), for a given I_m, the magnetizing inductance is calculated.

For a given I_m, and a maximum voltage for C_{S1} from (18) the capacitance C_{S1} is calculated. The switch S_1 is selected based on maximum voltage and current across the switch. The equations (27) and (29) present the maximum current and voltage of the switch S_1, respectively.

Simulation Results

The proposed SSPG with the following specifications: V_i= 48 V, fs=1kHz, V_P=2kV, Ls= 1uH, N=21, Lm=50uH, C_{S1}=100nF, C_{S2}=10nF, $\zeta = 15$, Q=.03, N_{MS}=30, A_{MS}=1 cm^2, and Ferrite material for the core of the PT is designed based on the previous section and is simulated using the Pspice software. Figure 7a shows the waveform of the voltages V_{CS2} and V_R. As shown, the capacitor C_{S2} is charged resonantly to twice of the voltage V_S. When the charge of the capacitor C_{S2} is ended, the MS opens and the output pulse is generated. Figure 7b illustrates the waveform of the input current i_i and the voltage of the switch S_1. Due to the resonant charging performance, the input current is half a sinusoidal waveform. Moreover, the voltage across the switch S_1 is low due to the PT and the resonance between the magnetizing inductance and the capacitor C_{S1}.

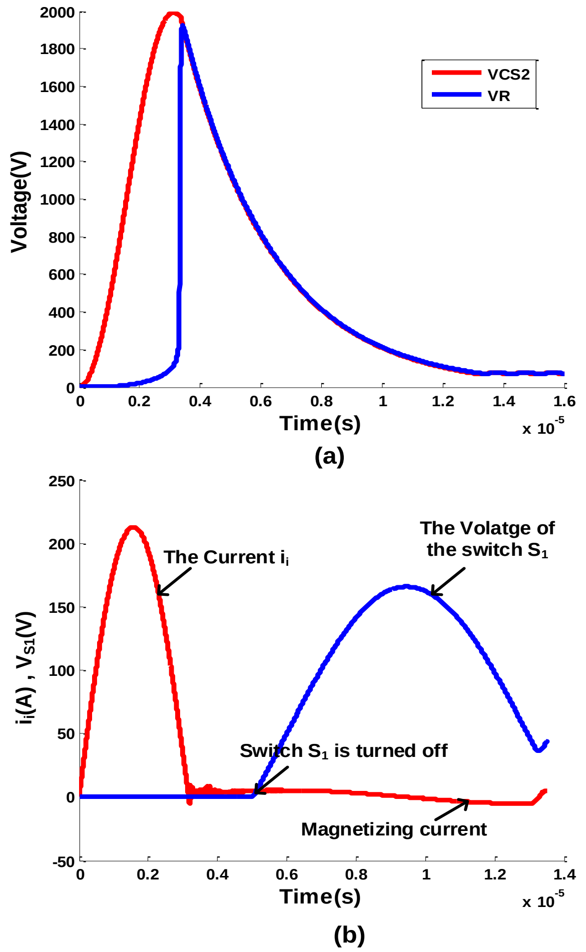

Fig. 7: The key waveforms of the proposed PG. (a) The voltage of the capacitor C_{S2} and the voltage V_R. (b) The input current and the voltage across the switch S_1.

Experimental results

According to the design section, ai$_i$ prototype constructed to verify the theoretical results. Figure 8 illustrates the experimental proposed PG.

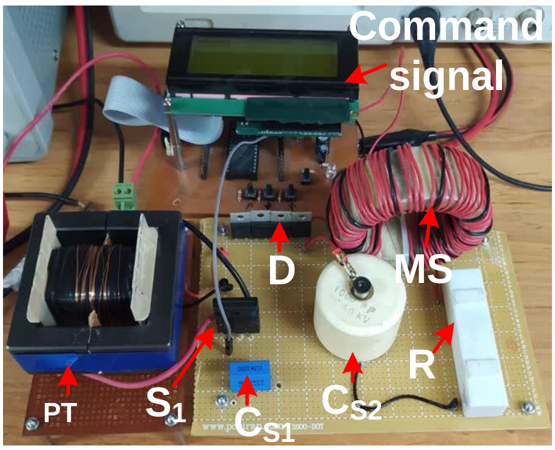

Fig. 8: The prototype configuration and construction of the proposed PG.

Table 1 shows the circuit specifications of the prototype. The input voltage of the proposed PG is 48V and the peak of the output pulse is chosen 1.5 kV. At first, the PT converts the input voltage 48V to 750V and then the resonance charging stage doubles the voltage 750V to 1.5kV. Designing the turn ratio 50 for the MS guarantees that the output pulse is produced at the end of the resonance charging operation.

Table 1: The circuit specification of the prototype

Symbol	Parameters	Value
V_i	Input voltage	48 V
V_P	The output pulse peak	1.5 kV
V_{CS2}	The voltage peak of the capacitor C_{S2}	1.5 kV
V_S	The secondary voltage of PT	750 V
N	The turns ratio of the PT	16
N_1:N_2	Primary turns: Secondary turns	10:160
L_m	The magnetizing inductance	77 uH
L_{lk}	The leakage inductance	270 uH
S_1	The switch part number	IXTK120N20P
C_{S1}	The C_{S1} capacitance	100 nF
C_{S2}	The C_{S2} capacitance	9.4 nF
PT	The Ferrite core	E 58/11/38
MS	The turns ratio	50
D	The four diodes are serried	MUR 860
R	The load resistance	300 ohms

Table 2: The proposed PG and the counterparts

Refs	Switch/ Inductor Num	Cap/MS Num	PT Num	RCD Losses	Switch Voltage stress
[9]	13/4	4/None	None	Yes	High
[10]	15/4	4/None	None	Yes	High
[11]	14/4	4/None	None	Yes	High
[12]	Many/ None	1/None	One	No	Moderate
[13]	5/2	1/None	None	No	High
[14]	6/None	4/2	None	No	Moderate
[15]	2/2	2/None	None	No	High
[16]	Many/ Many	Many/ None	Many	No	Low
[17]	Many/ Many	Many/ None	Many	No	Low
[18]	1/1	3/1	One	Yes	Low
[19]	4/None	2/1	One	No	Low
propos ed PG	1/None	2/1	One	None	Low

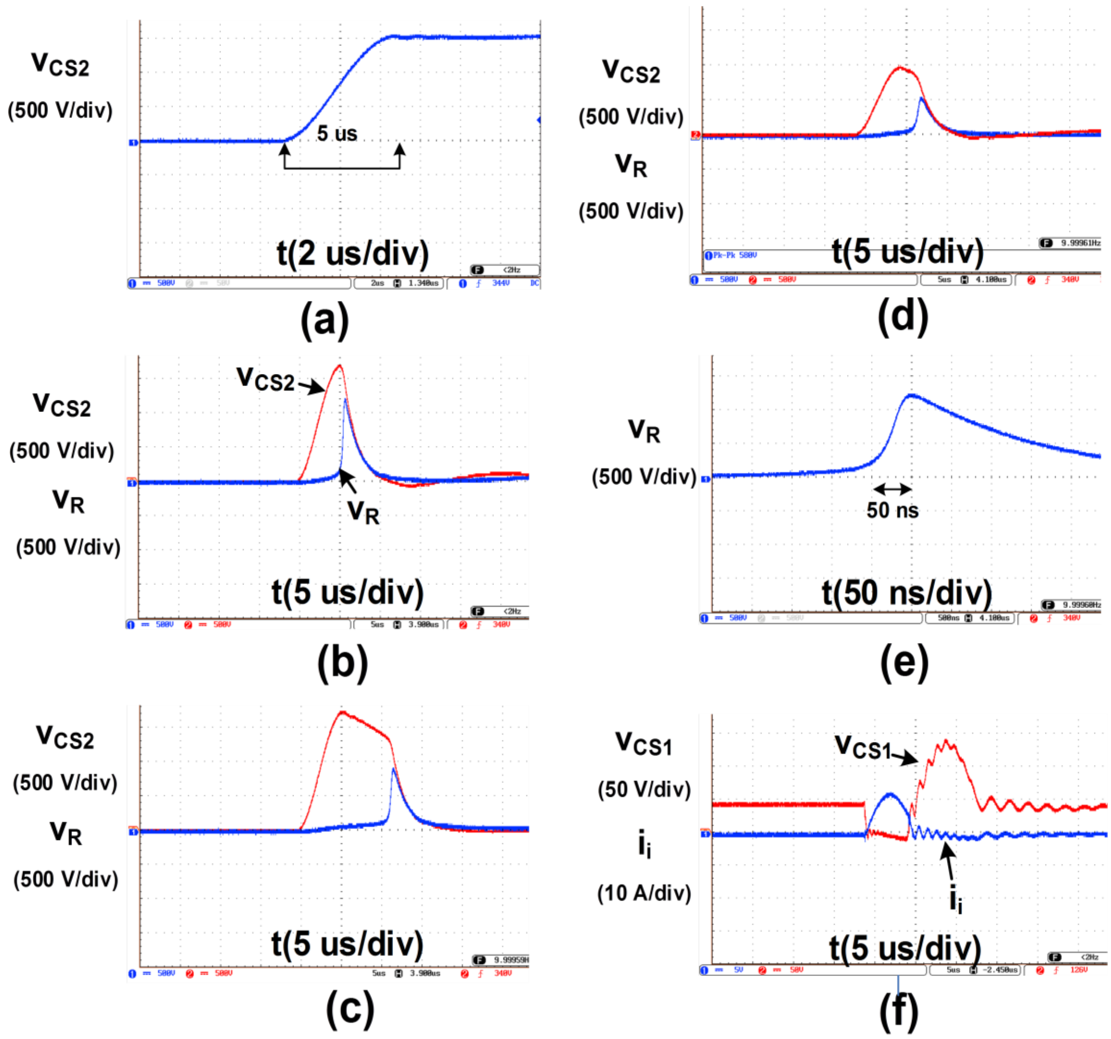

Fig. 9: The experimental results of the PG. (a) The voltage of the capacitor C_{S2} without the MS stage. (b) The output pulse voltage V_R and the output of the resonant charging stage VC_{S2} at the nominal input voltage (48 V). (c) The voltages V_R and VC_{S2} under reducing the reset circuit current at nominal input voltage (48 V). (d) The voltages V_R and VC_{S2} under reducing the input voltage (32V). (e) The rise time of the output pulse voltage. (f) The voltage of the switch S_1 and the current of the input source current.

Figure 9 shows the experimental results of the proposed PG. Figure 9a illustrates the voltage waveform of V_{CS2} without the MS stage. As expected, the voltage of the capacitor C_{S2} is charged to the twice the secondary voltage V_S during the time 5us. As explained at previous sections, the time interval 5us is obtained from the resonance between the capacitor C_{S2} and the leakage inductance L_{lk}.

The voltages V_{CS2} and V_R are shown at the Fig. 9b. As shown, at the end of charge of the capacitor C_{S2}, the MS is opened and the output voltage pulse is established due to the convenient turn ratio of the MS.

The peak of the output pulse V_P can be adjusted using the duty cycle, the input voltage V_i, and the current of the reset circuit of the MS.

As shown in Fig. 9c, under the constant voltage of V_i, the capacitor C_{S2} is fully charged but the pulse generation is delayed using the change of the MS core reset current. The voltage drop of C_{S2} is related to the leakage current of the MS when it is off. As shown in Fig. 9d, by decreasing the voltage of the input source from the nominal voltage, the capacitor C_{S2} is charged less than nominal; therefore, the peak of the output voltage is reduced.

By changing the turn-on time of the switch S_1, also the charge of the capacitor C_{S2} and consequently the peak voltage of the output pulse are varied.

The rise time of the output pulse voltage is approximately 50 ns as shown in Fig. 9e. The rise time of the output pulse voltage is related to the DF and the MS core material.

Figure 9f illustrates the voltage across the switch S_1

and the input source current. As predicted, the input current is the half sinusoidal waveform due to the resonant charging performance.

As seen, the switch S_1 can be turned off softly which reduces the switching losses. Moreover, the voltage across the switch S_1 starts from zero due to the resonance between the magnetizing inductance L_m and the capacitor C_{S1}.

As shown, the proposed PG needs a low voltage switch to produce a high-voltage pulse. From the current i_i, it is seen the magnetizing current is reversed when switch is turned off, therefore the PT does not need any additional reset winding.

Figure 10 illustrates the experimental output pulse when the resistance R changes. As expected from the section two, when R increases, the rise time is constant, but the pulse duration increases due to increasing damping factor.

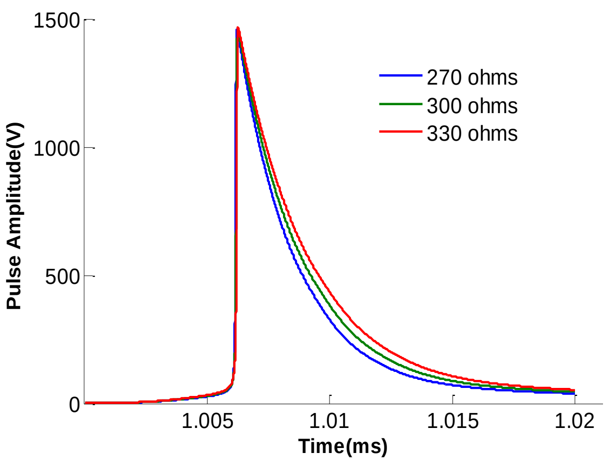

Fig. 10: The experimental output pulse amplitude versus the resistance R.

Conclusion

This paper proposes a novel pulse generator for DBD applications. The proposed PG uses three techniques named forward, resonant charging, and magnetic switch to produce a high-voltage nanosecond pulse. The resonant charging double the secondary voltage of the pulse transformer, this event reduces the turn ratio of the pulse transformer which decreases the weigh, volume, and price of the PT.

The magnetic switch section finally produces a nanosecond high-voltage pulse. The magnitude of the output pulse can be varied using the input source voltage, the MS reset circuit current and the switch duty cycle.

In the proposed PG, a low-voltage switch is needed to produce the high-voltage pulses. At the input source, using a capacitor paralleled with the switch can reset the core of the pulse transformer and the PG does not need any additional reset winding like the conventional DC-DC forward converter. The proposed PG is fully analyzed and the theoretical results are verified by the experimental results.

Author Contributions

Amir Hossein Nejadmalayeri in collaboration with Hamid Bahrami and Aref Balli, designed, simulated and carried out the data analysis, and Iman Soltani collected the data and interpreted the results and wrote the manuscript.

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Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the ethical issues including plagiarism, informed consent, misconduct, data fabrication and, or falsification, double publication and, or submission, and redundancy have been completely witnessed by the authors.

Abbreviations

PT	Pulse Transformer
MS	Magnetic Switch
MPC	Magnetic Pulse Compression
PG	Pulse Generator
PFN	Pulse Forming Network
DBD	Dielectric Barrier Discharge

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