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Research paper

Energy-Efficient Variation-Resilient High-Throughput Processor Design

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Abstract

Background and Objectives: The future demands of multimedia and signal processing applications forced the IC designers to utilize efficient high performance techniques in more complex SoCs to achieve higher computing throughput besides energy/power efficiency improvement. In recent technologies, variation effects and leakage power highly affect the design specifications and designers need to consider these parameters in design time. Considering both challenges as well as boosting the computation throughput makes the design more difficult.

Methods: In this article, we propose a simple serial core for higher energy/power efficiency and also utilize data level parallel structures to achieve required computation throughput.

Results: Using the proposed core we have 35% (75%) energy (power) improvement and also using parallel structure results in 8x higher throughput. The proposed architecture is able to provide 76 MIPS computation throughput by consuming only 2.7 pj per instruction. The outstanding feature of this processor is its resiliency against the variation effects.

Conclusion: Simple serial architecture reduces the effect of variations on design paths, furthermore, the effect of process variation on throughput loss and energy dissipation is negligible and almost zero. Proposed processor architecture is proper for energy/power constrained applications such as internet of things (IoT) and mobile devices to enable easy energy harvesting for longer lifetime.

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Introduction

The future demands of multimedia and signal processing applications forced the IC designers to utilize efficient high performance techniques in more complex System on Chips (SoCs) to achieve higher computing throughput besides energy/power efficiency improvement [1]-[2]. The requirements of target applications are widely various and demanding flexibility makes the custom design method to fail in providing intended performance.

Different parallel structures such as Single Instruction Multiple Data (SIMD), Multiple Instruction Multiple Data (MIMD) and Very Long Instruction Window (VLIW) are developed to reach design goals. These structures use parallel computing in different levels such as instruction-level, task/thread-level, and data-level while each structure has its own features and restrictions [1]. Massive parallel structures such as many-core

processors, systolic arrays, and GPUs are another kind of modern parallel processors which provide dramatic computing throughput [3]-[4]. While, increasing the complexity of the design by using parallel structures leads the design to consume more energy/power and causes cooling or supply challenges.

Power budget restriction is resolved using dark silicon technique or near/sub-threshold design [5]-[6]. Near/sub-threshold design dramatically reduces the energy/power consumption of the chip. However, it causes uncertainty in timing specifications of the design due to the variations in transistor parameters within and between dies, known as process variations [7]. In the presence of variations, more development time and cost with higher guard-bands are required to ensure the correct functionality of the chip. These guard-bands directly result in performance loss and lower production yield. Process variations and achieving higher throughput and keeping the power/energy within the bounds are becoming emerging concerns in new technologies and specifically in near/sub-threshold designs [8]. It is important to know that variations in process parameters considerably affect the expected performance of the design. Furthermore, any degradation in performance or reliability requires compensation techniques that result in higher power/energy consumptions. Therefore, design of variation-resilient architectures is of main concerns in new technologies.

In this work, we design a high-throughput and yet ultra-low-energy processor architecture which is resilient against the process variations. The rest of this paper is organized as follows: In the next section, we will introduce related works and will review advantages and disadvantages of the previous architectures. In Section III, we will describe our new energy efficient architecture and its features. Then, we will analyze the implementation results and estimations. At the end of discussions, we present our parallelization structure and its efficiency in terms of performance and energy consumption. Finally, we will summarize the results and conclude the paper in Section V.

Related Works

As mentioned in the previous section, process variations affect the timing specifications of the design, and energy efficient near/sub-threshold design intensifies the effect of these variations. Therefore, variations should be considered to keep demanding performance besides energy efficiency of the design. In this section we introduce recent energy-efficient or high-throughput processors as baseline architectures to be compared with our proposed architecture.

Subliminal [9] is a processor with three different versions of architectures which are designed for energy constrained applications operating at sub-threshold region. Using complex instruction set computer (CISC) architecture with complicated addressing modes, the authors achieved 1.2pj per instruction in 130nm technology providing 0.5 MIPS processing throughput at 200mv. This processor is suitable for low or mid performance applications, while not suitable for high performance applications. Higher power supply will improve the throughput while increasing the energy consumption.

TamaRISC-CS [10]-[11] is another energy efficient processor which uses custom instruction and custom memory architecture to optimize the energy efficiency besides higher performance in a multi-core environment. This processor exploits RISC style architecture with complicated addressing modes to construct a simple energy-efficient core working with high frequency to achieve high computing throughput. The results show that 62x speed-up is achieved through efficient ASIP design. At the other hand, this processor provides limited performance with lower energy efficiency.

In [12] a 10-lane SIMD processor namely Synctium I is designed to work at 530mv and provides high throughput with low timing variation. Timing uncertainty of Synctium I is minimized using three techniques: 1- error detection and correction, 2- decoupling queue between lanes and 3- lane sparing. These techniques have also doubled the performance of the processor. This processor has poor energy efficiency providing dramatic performance.

The authors of [13] have designed a processor for battery-less systems which are able to operate using ambient energy sources. They have explored different architectural configurations such as no-pipeline, n-Stage pipeline and out-of-order execution considering the requirements of 3 different scenarios for target applications. The authors have proposed design guidelines for energy-efficient processor design with respect to the application requirements.

In [14], a novel heterogeneous dual-core processor has been proposed to meet both high throughput and ultra-low-power requirements for continuous operation of target applications. The processor architecture has two cores: one low-power core which operates in near-threshold region and a high-performance one to provide burst-mode requirements. They have proposed an energy-efficient task mapping to employ the underlying cores to achieve both requirements at the same time. The processor consumes 7.7pJ/cycle to have no deadline miss for target benchmarks.

Authors of [15] have proposed an artificial intelligence processor (AIP) with three heterogeneous units to provide performance and power requirements: 1) 8-thread search processor and decision making

accelerator, 2) 3-level cache to reduce repetitive computations and 3) on-chip variation monitoring to keep operations stable. The processor is working at 0.5-1.2V consuming 1.1mW to 150mW.Exploiting an embedded variation compensation unit, energy consumption is reduced by 32% while providing 276X search speed-up in comparison to the Cortex-M3 processor.

In [16], the authors proposed a method to use dynamic timing slack of the processor to improve energy consumption. The probability of critical path activation highly depends on the application. The authors present an automated method to detect the dynamic slack based on path activation of the design and achieve 25% average power reduction.

Authors of [17] propose SPARC M7 processor which consists of eight cache clusters, and an on-chip network high speed SerDes to have higher communication rate between underlying units. Their proposed architecture totally has 32 performance improved cores with low latency cache and memory hierarchy structure which provides 3X speed-up in comparison to its previous version SPARC M3.

The authors of [18]-[19] have proposed a bit-serial structure of openMSP430 for energy-constrained sensor applications to achieve higher energy efficiency and provide energy harvesting capability. The serial structure without any ISA modifications results 42% power improvement.

The serial architecture has 1.1X higher clock rate while provides 16X lower computation throughput at nominal supply voltage which is proper for low-performance applications. Their proposed serial architecture operates in near/sub-threshold region and the supply reduction degrades the processor specifications and reduces the improvements.

Authors of [20] proposed a near-threshold processor based on RISC-V architecture for low and mid performance IoT applications. This processor works down to 250mV power supply and consumes 4.5 pJ to 9.6 pJ per cycle. RISC-V architecture is also used in [20] and [22] in a parallel structure to design a processor for ultra-low-power applications such as IoT and wearable sensing. Power consumption of Parallel Ultra-Low Power processor (PULP) proposed in [21] is lower than 12mW to process the sensor data for human machine interaction. The next PULP processor in [22] is able to deliver 2.5 GOPS consuming only 55mW. It is about 38x more energy efficient compared to ARM Cortex-M as a low power processor working with 0.7V power supply.

Authors of [23] proposed a many-core processor for digital signal processing working in sub/near-threshold regime. In this work, a many-core processor is proposed using small processing core to achieve higher throughput while consuming lower power/energy. They claimed that with a negligible hardware overhead, the overall processing time for target benchmark applications (signal processing domain) is improved by 90% and reduced the power consumption by about 30% which results more reduction in energy consumption.

In the next section, we present our proposed simple energy efficient processor core in order to achieve energy efficiency which consumes lower energy in comparison with the literature. In this architecture we have used the basic custom core to build a parallel architecture and to improve the performance of the design. This architecture provides both high throughput and energy efficiency at the same time, while to get the one, the other has sacrificed in the literature.

Processor Architecture

According to our previously published analysis [24], using bit-serial structure for designing computational units in newer technologies, specifically in sub-threshold region leads to less current leakage during computation cycles.

We have also shown that the effect of process variations on working frequency is reduced because of shorter paths, while achieving mid performance. Therefore, we designed a RISC-style serial processor as our basic processing element namely ultra-low-energy (ULE). ULE has higher energy efficiency in comparison to bit-parallel structures and would exploit parallelization to improve the computation throughput.

The proposed architecture is designed to meet the variation resilience besides energy efficiency and higher throughput.

Variation resiliency and energy efficiency are provided using a simple serial core and higher throughput is achieved by massive data level parallel structure. The proposed processor can execute the same program on different data and this feature highly improves the computation throughput.

In this section, we present our energy-efficient serial core including memory organization, controller logic, ISA, and encoding scheme. At the second step we will describe our proposed parallel structure using the basic core.

The processor architecture is based on Harvard architecture with physically separated instruction and data memories and signal pathways. We have divided the data memory into 128-Byte pages to reduce the energy consumption of the memories and also provide concurrent accesses to different pages in our parallel structure.

High-level block diagram of the processor as shown in Fig. 1, includes instruction memory, data memory (at least 128B), and the processing core.

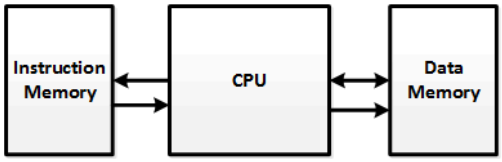

Fig. 1: system-level diagram of processor.

We have chosen a RISC-style bit-serial architecture for ULE processing core to decrease area and logic depth for diminishing process variation effects, and also improving energy efficiency. Fig. 2 shows the bit-serial structure for an adder unit which utilizes a single-bit full adder in combination with a flip-flop to perform addition at different clock cycles (SFA). This structure is more area- and energy-efficient and less vulnerable to variations in comparison to parallel structures [24]. Equations (1), (2) depicts the energy consumption(delay × power) of parallel and serial structures(respectively) to do the same computation considering the variation effects and (3) shows the energy ratio for both structures(nominator is parallel and denominator is serial) which serial structure is 8 times energy efficient.

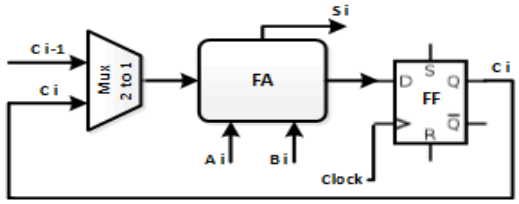

Fig. 2: Single-bit full adder (SFA) in combination with a flip flop to do n-bit addition sequentially at subsequent clock cycles [13].

$$E_{parallel\text{-}8bit} = (8 * \mu + 3*\sqrt{8}\sigma\,) * 8\,P_{full\text{-}adder} \quad (1)$$

$$E_{Serial\text{-}8bit} = 8 *(\mu + 3*\sigma) * P_{full\text{-}adder} \quad (2)$$

$$\frac{E_P}{E_S} = \frac{8\mu+6\sqrt{2}\sigma}{\mu+3\sigma} \sim \frac{8\mu+8\sigma}{\mu+3\sigma} \sim 8 \quad (3)$$

where μ is the average delay for a full adder unit (FA) and σ defines the standard deviation of delay for the same unit.

Fig. 3 represents the block diagram of the ULE processing core. Data path of the processor includes fetch and decode unit, data memory buffer, constant register, serial shift register file, ALU, and controller units. The fetch unit reads an instruction from instruction memory, then the decode unit decodes the instruction and generates controlling signals. Data memory controller calculates the address of load/store including both page and entity addresses, and then it activates read/write signal serially from/to data memory buffer. Jump shift register is used to save jump address, and then this address is transferred to program counter (PC) for next fetch as the next instruction address. Jump target address would be a direct immediate or register-indirect address.

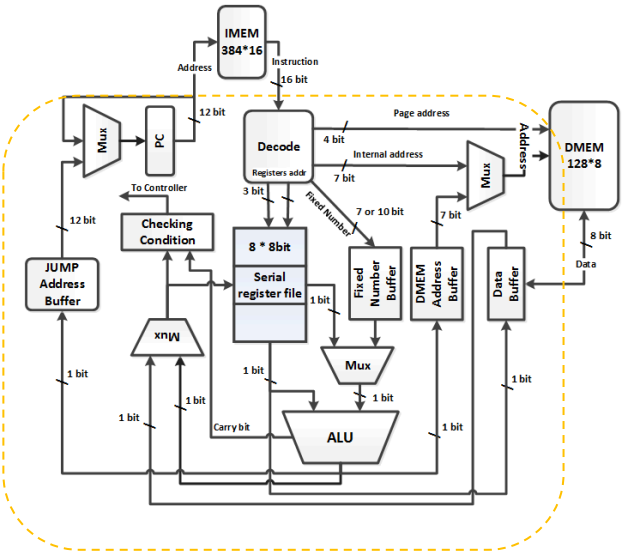

Fig. 3: Structure of ULE core.

ALU is designed in a bit-serial structure and input data is received sequentially while the previous registered carry bit (for add/sub) is used to calculate the next carry and sum. Therefore, the result is generated serially one bit per cycle and the number of clock cycles to complete the operation is equal to the number of bits. Generated results are shifted into register file bit by bit and the operation is performed using a multiplexer. Fig. 4 shows the ALU structure.

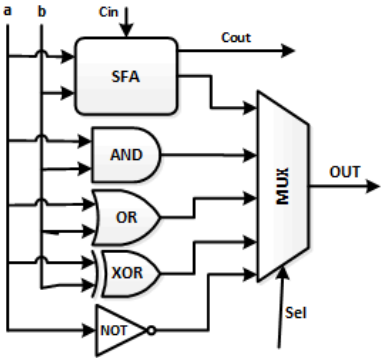

Fig. 4: ALU structure of the CPU.

Serial register file or shift register file of CPU consists of eight 8-bit shift registers, which shifts the data to the destination address at write-back stage in a pipelined manner. The ALU and processor data-path are configurable and designed to operate in various data widths such as 8, 16 or 32 bits. In this case we have used 8-bit version by 8 consequent clock cycles for each instruction.

The RISC-based instruction set architecture (ISA) of the CPU is designed based on a simplified instruction set. An important parameter in ISA design is the number and variety of supported operands. We have chosen2-operand load-store RISC-style ISA for our proposed architecture which is shown in Table 1. The choice of 2-operand instructions is based on [2] which shows that for the representative set of applications, the 3-operand choice generates about 10% larger code in comparison with 2-operand one. The encoding scheme of 16-bit instructions is shown in Fig. 5 and Table 1. The instructions set format have five generic fields: I (Immediate and condition), Op (operation code), Rd (destination register), Rs (source register), and condition field. Encoding scheme is defined in a regular structure: I and OP sections are available for all 7 instruction types and the other parts are specific to the operation and operands of each type. For instruction types listed in rows 1, 3, 4, 5 and 6 in Table 1, different execution modes are provided, which are conditional, unconditional and immediate execution. These modes can be selected by two bits (as I section) at the beginning of instruction encoding.

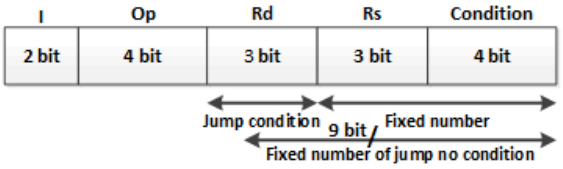

Fig. 5: Generic structure format of instructions.

Table 1: ISA Organization. s: sign bit, c: carry, g: greater than, l: lower than, ge: equal or greater than, le: lower than or equal, e: equal, ne: not equal. Shift input can be 0 (I0), 1 (I1), s, c. Source register (rs) and destination register (rd) are from the eight registers r0 to r7

#	Instructions	Code format	Structure format
1	Add, Sub, And, Or, Xor, Mov, Cmp	(Condition) rd,rs; rd,rs; rd,#Fixed_num;	00 or 01 | Op 4 bit | Rd 3 bit | Rs 3 bit | Condition 4 bit 10 | Op 4 bit | Rd 3 bit | Fixed number 7 bit
2	Not	rd; (Condition) rd;	00 or 01 | Op 4 bit | Rd 3 bit | xxx | Condition 4 bit
3	Shl, Shr	rd; (Condition) rd; rd, shift_Input, #num_shift	00 or 01 | Op 4 bit | Rd 3 bit | Shift input 3 bit | Condition 4 bit 10 | Op 4 bit | Rd 3 bit | Shift input 4 bit | Fixed number 3 bit
4	Load, Store	rd,[#address_fixed_num]; rd,[rs];	10 | Op 4 bit | Rd 3 bit | Fixed number 7 bit 00 or 01 | Op 4 bit | Rd 3 bit | Rs 3 bit | Condition 4 bit
5	Jump	(Condition) #jump_address; #jump_address;	11 | Op 4 bit | Condition 4 bit | Fixed number 6 bit 10 | Op 4 bit | Fixed number 10 bit
6	Stc, Ldc	; (Condition);	00 | Op 4 bit | xxxxxxxxxx 10 | Op 4 bit | Condition 4 bit | xxxxxx
7	Chp (chpd), Chpi	#Page_address;	10 | Op 4 bit | D/M 1bit | Page number 4 bit | xxxxxx

Results and Discussion

We have synthesized our proposed processor using 90nm sub-threshold library [24] and estimated the power consumption using VCD files at different supply voltages ranging from 0.2V to 1.0V. Firstly, we present the evaluation results of basic core in comparison to the own implemented subliminal processor in 90nm (named as SSL2 in figures).

Performance, power, and energy estimations is done using FIR and TEA programs [9], [26], [27], [30] as signal processing and encryption algorithms which are used in different applications.

Finally, we will present the parallelization results and throughput improvements. Fig. 6 presents the evaluation flow chart.

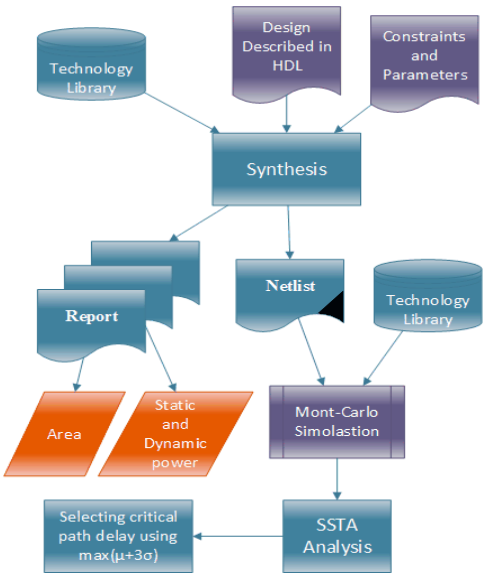

Fig 6: Evaluation flow chart for proposed architecture and re-implemented subliminal processor [9] in 90nm technology.

A. Area

Table 2 summarizes the area results for our proposed architecture in comparison with our implementation of subliminal core. This comparison is done through the same size of program and data memory for fair comparisons. According to this table, with different cores and the same memory area, our proposed architecture has almost 1% smaller area due to bit-serial core structure. The area reduction relaxes the parallelization limits to achieve higher performance/throughput besides lower die cost. Due to bigger memory area in comparison to processing cores in both architectures, total area reduction is not considerable, however, in contrast, excluding the memory area, core area is reduced by 35%.

Table 2: Area results of proposed processor in custom90nm CMOS

Architecture	Subliminal	Proposed	DSP [22]
Total Area(μm2)	242228	240639	248631
Core Area(μm2)	4540	2951	10943

B. Power Consumption

Leakage power in finer technologies and especially in near/sub-threshold region plays an important role and directly relates to the design area. Proposed architecture has lower leakage power due to area reduction. Table 3 and Fig. 7 present the total power consumption of both architectures running benchmark applications at different supply voltages.

According to these results, the proposed architecture dissipates 75% lower power in comparison to the baseline processor.

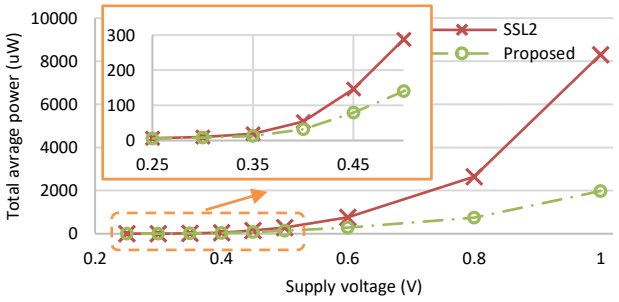

Fig. 7: Total power consumption of the proposed architecture in comparison to subliminal [9].

Table 3: Powerconsumtion results in custom90nm CMOS

Voltage (v)	Subliminal (uW)	Proposed (uW)	DSP [22] (uW)
1.0	8305	1980	-
0.6	754	293	200
0.4	54	31.7	40
0.3	10.1	8	10

C. Performance and Throughput

In the next step, we use different metrics for performance evaluation. The critical path delay indicates the working frequency as a measure of processor performance. Clock per instruction (CPI) is another important factor which is useful in conjunction with working frequency to figure out the other important performance parameters such as instruction latency, execution/computation throughput, and application latency. Million instructions per second (MIPS) is also a well-known parameter to measure the execution throughput of any processor.

Fig. 8 and Table 4 summarize the critical path delay and working frequency at different supply voltages in comparison to the subliminal processor. Also, the required clock cycles to execute each instruction are shown in Table 5. Proposed architecture has about 3x higher clock rate in comparison to the baseline architecture, while more clock cycles are needed to execute each instruction. Combining these parameters (which is the product of critical path delay and CPI) will show that the instruction latency for the proposed architecture is almost 2.6xmore than subliminal. For example, at 1V supply voltage instruction latency of the proposed and baseline architecture is 8.4ns and 3.2ns, respectively.

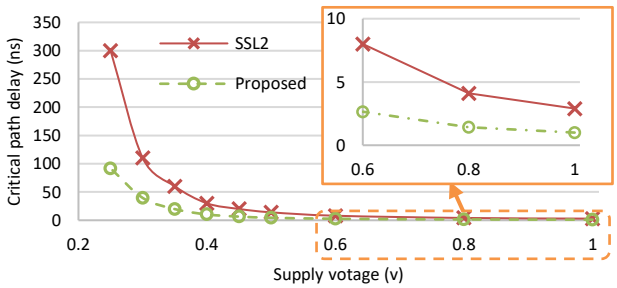

Fig. 8: Critical path delay at different supply voltages.

Table 4: Working frequency in custom90nm CMOS (MHz)

Voltage (v)	Subliminal [9]	Proposed	DSP [22]
1.0	345	1000	350
0.6	125	377	130
0.4	33	97	40
0.3	9	25	15

Table 5: Performance results (CPI)

	Subliminal [9]		Proposed		DSP [22]
CPI	FIR	TEA	FIR	TEA	FIR
	1.2	1	6.5	10.3	1.070
Average	1.1		8.4		1.070

Considering instruction latency, Table 6 and Fig. 9 summarize the MIPS results for both architectures.

According to these results, proposed architecture is capable of providing demanding performance.

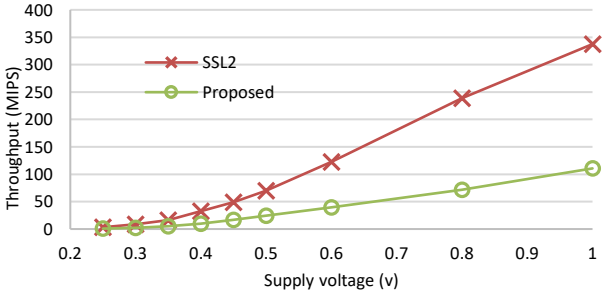

Fig. 9: Throughput vs supply voltages for both architectures.

Table 6: Performance results in90nm CMOS (MIPS)

Voltage (V)	Subliminal	Proposed
1.0	337.5	110.6
0.6	122.3	39.8
0.4	32.6	9.9
0.3	8.9	5.1

D. Energy Consumption or Power-Delay Product

Energy consumption is another important metric to be considered in energy-constrained systems. It is important to know that higher performance improves energy efficiency due to dominant effect of leakage power in newer technologies especially in near/sub-threshold regions. Therefore, a system with lower power consumption and higher performance could be more energy efficient in comparison to a system with lower power and lower performance.

Energy per instruction is a common parameter for comparing two different architectures, which is the product of instruction latency and total power consumption. Furthermore, total energy dissipation of application is another important factor which indicates the processor efficiency. Fig. 10 shows the energy per instruction of both architectures in average for FIR and TEA applications at different supply voltages. Table 7 and Table 8 summarize the energy per instruction and total energy consumption of both processors at different supply voltages.

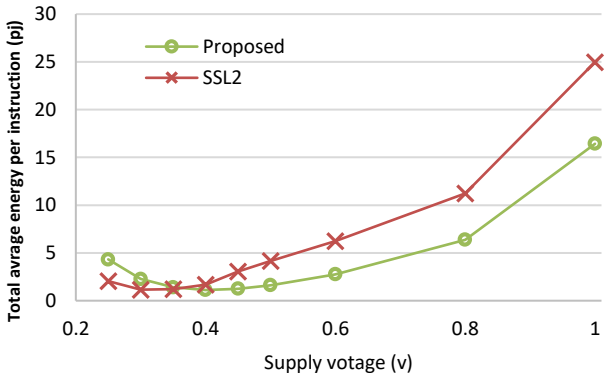

Fig. 10: Total energy consumption of proposed architecture in comparison to subliminal.

Table 7: Energy per instruction (pJ) in custom90nm CMOS

Voltage (V)	Subliminal [9]	Proposed	DSP [22]
1.0	25	16.4	-
0.6	6.2	2.8	3
0.4	1.7	1.1	1.2
0.3	1.2	2.3	0.8

Table 8: Total energy dissipationin custom90nm CMOS (nJ)

Voltage (V)	Subliminal [9]	Proposed	DSP [22]
1.0	2070	1678	-
0.6	493	200	270
0.4	130	85.5	130
0.3	93	43.6	70

According to the results, in average, the proposed architecture has 30%lower energy per instruction and also 20% lower total energy consumption at 1V. The improvement would be even better at lower supply voltages.

E. Variations Analysis

As mentioned previously, the effect of process variations in newer technologies has grown and should be considered in design time to boost demanding performance and energy efficiency. Since shorter paths means higher working frequency and lower performance loss, due to process variation, the proposed architecture suffers almost 60% less than subliminal in terms of path delay. Fig. 11 shows the delay variation of both processors at 1V and 0.4V supply voltages in comparison.

This reduction also reduces performance loss and energy overhead. The mean (μ) and standard deviation (σ) of path delay distribution for the proposed architecture (normalized to the delay distribution of the baseline processor) at different supply voltages are presented in Fig. 12 and Fig. 13. According to these figures, the proposed architecture has more compact delay distribution and higher working frequency and these differences are far in higher voltages which is compatible with the results of Fig. 11. Due to lower power consumption, the proposed architecture is capable to operate in higher voltages with the same power consumption to achieve higher working frequency and reduce the performance difference in comparison to the subliminal.

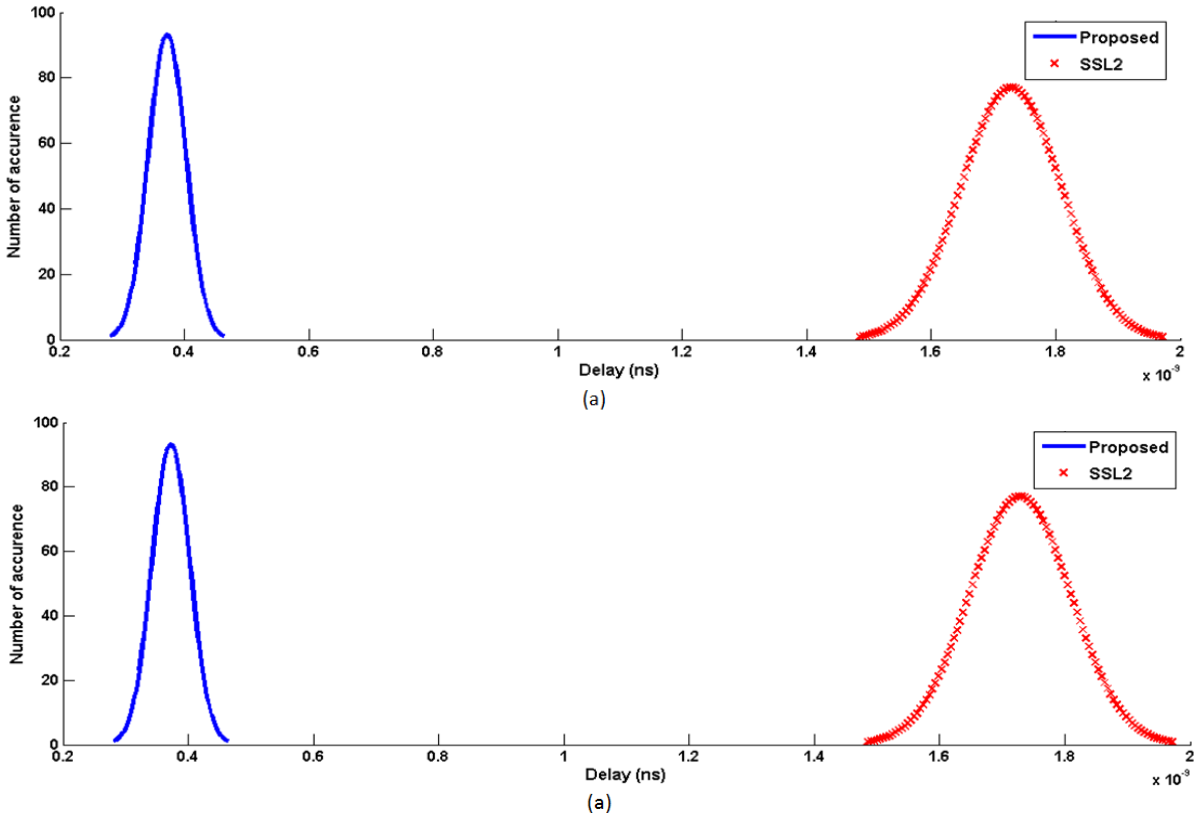

Fig. 11: delay distribution for a) 1V and b) 0.4V.

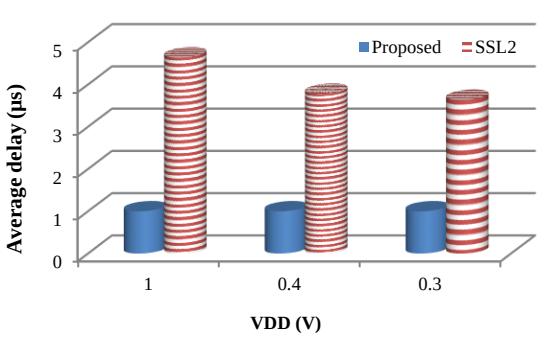

Fig. 12: Average delay (μ) parameter of critical paths normalized to proposed design.

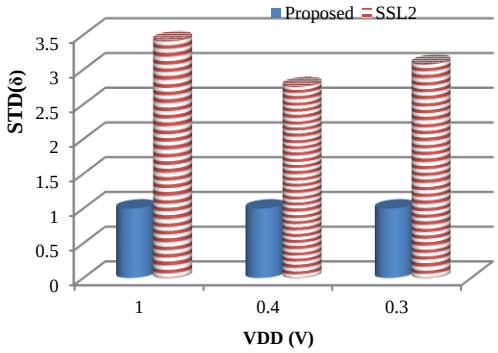

Fig. 13: Standard deviation (σ) parameter of critical paths normalized to proposed design.

F. Parallelization

The results show that the proposed processor has smaller area and lower cost besides higher energy efficiency, lower performance, and lower energy overhead in case of process variation. On the other hand, the proposed core provides similar performance compared to baseline processor. Achieving higher performance/throughput could be provided by parallelizing energy-efficient basic structure. Utilizing serial data-path of basic core in SIMD parallel structure enables the processor to run the same instructions on different data. Using paged data memory provides parallel access to data blocks without any contention and access overhead. Fig. 14 shows the proposed parallel architecture utilizing the energy-efficient basic core. This parallel structure is capable of achieving higher throughputs accordant to application demands. Exploiting data level parallelization reduces the dependency between different processing lanes and reduces the complexity. Therefore, the proposed parallel structure could deliver higher performance besides energy and cost efficiency.

The proposed parallel architecture is organized to use the controlling part of each lane as a common shared unit which is known as shared part in Fig. 14. This unit decodes the instructions and manages the processing lanes with proper controlling signals. Processing unit and other resources such as register file, address and data buffer (for accessing data memory) are isolated for each lane known as private parts (Fig. 15). The parallel architecture is optimized to reduce the parallelization overhead and keep energy efficiency besides higher throughput.

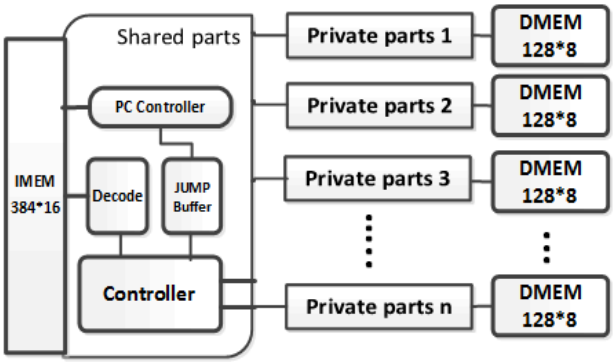

Fig. 14: SIMD processor architecture.

Table 9 summarizes the performance results of parallel SIMD structure using basic data-path with different parallelization degree. In this table, the candidate architectures working at 0.4V and performance results at this voltage are listed for different processors (except for Synctium I which is functional above 0.53V). It is important to know that we have considered the proposed simple core to work with the same frequency as proposed SIMD version and the parallelization overhead is considered in single core structure.

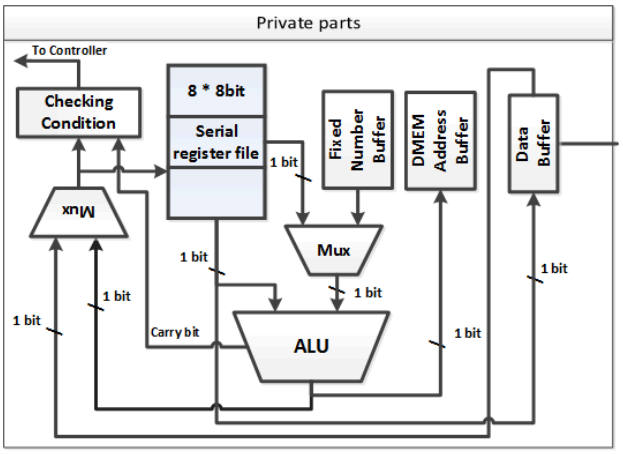

Fig. 15: Private parts of each SIMD lane.

Table 9: MOPS results for candidate processorsat 0.4V.

Processor	Technology (nm)	Energy per instruction (pJ)	Throughput (MOPS)	Freq. (MHz)
Subliminal [9]	90	1.7	19	33
Proposed	90	1.1	9.5	97
8-lane proposed SIMD	90	2.75	76	97
TamaRISC-CS [10]	90	5	0.8	0.11
Synctium-I [12]	45	165	680	85
Many-Core [22]	90	0.8	-	40

Taking an analytical look at performance results may lead to superiority of subliminal [9] running at lower supply voltages in comparison to the proposed core with higher supply voltage, which consumes lower power while providing similar performance with small loss. At the other hand, due to multi-cycle completion of instructions in proposed core, process variations have more effects on the proposed core according to accumulative manner of variation in timing in consecutive cycles. The conclusion is correct for single core design without considering the parallelization. We have designed the underlying energy efficient core to utilize in parallel structure. Then it is important that the goal of basic core is to reduce the energy consumption and the duty of parallel structure is to increase the performance with smaller overhead. Trying to use the subliminal in a parallel structure needs more hardware overhead and the energy requirements will grow in parallel structure. Due to energy efficient basic core, 8-lane proposed SIMD only consumes energy less than 2x of subliminal while providing 4x more performance. in

order to achieve the same performance using 4 subliminal cores in parallel structure, the processor will consume energy 2.5x more than proposed SIMD core.

According to the performance results for the proposed and baseline processors (listed in Table 9), the proposed architecture provides higher computation throughput while consuming lower energy. On the other words, performance loss and energy overhead due to process variation is reduced. Massive parallel structures such as GPUs and systolic arrays have bright future for applications with high performance and low energy demands such as multimedia applications and specially hand-held and portable devices. Enabling partial power gating for each lane provides more flexibility for these architectures to support wider applications from low to high performance requirements.

Conclusion

Recent technology advancements help the designer to achieve higher performance realizing complex SoCs. Despite performance improvements, feature size scaling has made the power/energy consumption more challenging and process variation has intensified the crisis.

In this paper, we have proposed area and energy/power efficient bit-serial processor architecture which delivers acceptable performance. On the other words, the performance loss due to process variation is reduced by 60%while consuming 35% less energy. The proposed core exploits RISC ISA with serial structure to reduce power/energy consumption and increases energy efficiency. Furthermore, shorter paths improve performance at the presence of process variation, and reduce performance loss due to fluctuations.

Higher performance/throughput is achieved using parallel structure and banked memory organization. Using the proposed parallel structures dramatically improves energy efficiency besides cost and performance improvements.

It is important to note that when talking about ultra-low-power/energy and near/sub-threshold computation, there are similarity between 90nm and up-to-date technologies (below 10nm) in the ratio between static and dynamic power/energy consumption and sensitivity of the design to any change in path delays. Employed design techniques in sub-threshold regime for 90nm are applicable for newer technologies due to mentioned similarities.

Author Contributions

A. Teymouri, H. Dorosti, and M. E. Salehi designed the experiments with the guidance of S. M. Fakhraie. A. Teymouri collected the data with the help of H. Dorosti through proper simulations, and data analysis is carried out by A. Teymouri and H. Dorosti. Finally, A. Teymouri, H. Dorosti, and M. E. Salehi interpreted the results and wrote the manuscript.

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Conflict of Interest

Authors declare that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

Abbreviations

DSP	Digital Signal Processor
ISA	Instruction Set Architecture
FFT	Fast Fourier Transform
TEA	Tiny Encryption Algorithm
FIR	Finite Impulse Response
RFID	Radio Frequency Identification
ALU	Arithmetic and Logic Unit
MAC	Multiply and Accumulate
RISC	Reduced Instruction Set Computer
CISC	Complex Instruction Set Computer
CPI	Clock Per Instruction
MIPS	Million Instruction Per Second
VCD	Value Change Dump

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