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Research paper

An Ultra-Low Power Ternary Multi-Digit Adder Applies GDI Method for Binary Operations

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Abstract

Background and Objectives: A novel low-power and low-delay multi-digit ternary adder is presented in this paper which is implemented in carbon nanotube field effect transistor (CNTFET) technology.
Methods: In the proposed design, CNTFET technology is used where reducing the power consumption is the main priority. A CNTFET's geometry directly determines the threshold voltage. In this architecture, at each stage, a half adder is applied to generate the intermediate binary signals which are called half-sum (HS) and half-carry (HC). To implement the binary operations of the design, the gate diffusion input (GDI) method is applied. A significant reduction of the power consumption is achieved while the PDP is improved.
Results: The proposed designs are simulated in synopsis HSPICE simulator. The Stanford 32 nm CNTFET technology is applied while the power supply is 0.9 v and the simulation is performed at room temperature. In this case, the pitch value of 20nm are chosen where the number of the tubes taken are 3. In this work a GDI based sum generator and a low-power encoder are used to calculate the final sum value of each stage. Furthermore, the proposed carry generation/propagation block results in a remarkable reduction of the overall propagation delay time. The simulation reveals a significant improvement in terms of the power consumption (up to 27%), the PDP (up to 41%) and the FO4 delay (up to 20%).
Conclusion: An efficient CNTFET based multi-digit ternary adder has been presented in this paper. The Synopsis HSPICE simulator is used where Stanford 32 nm CNTFET model are applied to simulate the design. According to the results, a significant saving in average power consumption is achieved where the power-delay product (PDP) is improved by 41% compared to the best existing design.

Introduction

Binary combinational logical circuits have an important concern in terms of the design complexity [1]. Generally, interconnects generate 70% of total on-chip capacitance [41]. Due to that, they are the most important sources of the power dissipation in a VLSI chip [2], [42], [43]. Recently, Multi Valued Logic (MVL) has been of interest.

It has brought many benefits in terms of hardware utilization, interconnects, number of digits required and average power consumption. Also reducing the scale size to the Nanometer limits the usage in the implementation of low-power digital designs. A review of the literates depicts that non-silicon devices of multi-valued logic systems are an offered circuit to implement high-

efficiency digital architectures. Since hardware complexity is directly proportional to the radix of a MVL system [3], calculations of base-3 (close to *e* = 2.718) is an optimum choice called ternary logic. New molecular devices have been widely developed to succeed conventional silicon-based CMOS technology. CNTFETs may be an alternative to silicon MOSFET devices due to their excellent operating characteristics with some similarity in their inherent characteristics [4].

The similar dimension of an N-type and a P-type CNTFET has the same mobility. It affects the sizing of the transistors in a complex circuit. CNTFETs are more suitable for implementing three-valued logic circuits because they can obtain multiple threshold voltages by changing the physical dimensions of the carbon nanotubes (CNTs). Chirality is a well-known characteristic of CNTFETs. It depends on the diameter of the CNTs. Any variation of the chirality affects the CNT's threshold voltage.

Multiple threshold voltages are required to implement a three-valued logic circuit. So, it can be obtained by CNTFETs of different chirality [5]. A wide different CNTFET-based ternary operations and logic circuits such as the logic gates, adders, and multipliers are discussed in [6]-[23].

Also, two CNTFET based Ternary ALUs (TALUs) which include a huge number of transistors have been presented in [21] and [22]. These power-consuming structures use a decoder-encoder based approach. A novel CMOS based ternary ALU is proposed by [26]. It employees the decoders, the ternary gates and the ternary buffers to implement various digital blocks like the adder, the subtractor and the multiplier. In this work [26], the depletion type MOS transistors and the large off-chip resistors significantly increase the power and the area consumption. A modified version of this TALU [26] is presented by [27] where the adder and the subtractor modules are in the same block and the outputs are multiplexed using the ALU select signals. There is a modified version of [27] which is proposed by [28], where the adder, the subtractor and the Ex-OR gate are combined in a single module. In this paper, a novel multi-digit ternary adder is introduced while it is more efficient in terms of the power and the PDP metrics. The proposed architecture applies the GDI method for implementing the binary operations.

Hence, an improvement is expected in terms of the power consumption. The rest of this paper is organized as the following: section two gives a concept of the ternary logic and the multi-digit ternary adders.

Our detailed proposed design is presented in Section three. In section four the simulation results and the comparisons have been fully discussed. Finally, section five is the conclusion.

Backgrounds of Research

A. CNTFET Based Ternary Logic

A three-valued logic (ternary logic) is an offered type of multi-valued logics. In this, the three truth values indicating *true*, *false* and an indeterminate 3rd value are included. In this case, 0, 1 and 2 directly correspond to a voltage value of 0, Vdd/2, and Vdd. In fact, f(y) is a ternary logic function of y= {y_1, y_2, …, y_n} maps $\{0.1.2\}^n$ to $\{0.1.2\}$. In this three-state logic, AND and OR functions are defined as min {y_i, y_j} and max {y_i, y_j} respectively. In three-state logic, the inverting gate, which is widely used in the design of other gates like NAND and NOR and most of the logic circuits, is defined as NTI, PTI and STI (which stand for negative, positive and standard ternary inverter respectively). Threshold voltage changes in exchange for CNT diameter changes have made them a viable option in MVL circuits. A graphite sheet is rolled up to create a CNT. In this case, C is the roll-up vector ($C = n\bar{a} + m\bar{b}$).

In this equation, $\bar{a}$ and $\bar{b}$ are the unit lattice vectors and the pair (n,m) is the chirality vector of the carbon nanotube. The integer values (n,m) determine the type of a CNT: metallic or semiconducting. If (n = m) and (n-m = 3i e.g. i is an integer), a CNT is a metal.

Otherwise, it treats as a semiconductor. The diameter of a CNT in Nano-meter is expressed as: $D_{CNT} \approx 0.0783\sqrt{n^2 + m^2 + n.m}$. Also, the threshold voltage of a FET in volt and a CNT's diameter in (nm) are inversely proportional as: $V_{th} = 0.43/D_{CNT}$. The most common chirality vectors that are used for implementation of MVL circuits are (19,0), (13,0) and (10,0) so that they provide threshold voltages of 0.289, 0.428 and 0.559 for an N-CNTFET and equivalent values with negative sign for a P-CNTFET respectively [29].

B. The GDI Transistor Level Implementation Technique

The gate diffusion input (GDI) method [30]-[34] is a well-known method which is developed based on a simple cell including two transistors.

It is shown in Fig. 1. G: the common gate input of the NCNT and the PCNT transistors (in CMOS technology NMOS and PMOS are used), P: the outer diffusion node of the PCNT transistor, N: the outer diffusion node of the NCNT transistor, D: the common diffusion node of the both transistors.

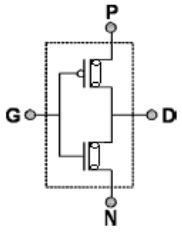

Fig.1: The basic cell of the GDI method [34].

Depending upon the circuit structure, P, N, and D would be either input or output ports. Table 1 includes several simple logic functions implemented by the GDI method.

Various Boolean functions could be simply implemented when a simple configuration changes occurred at the inputs. So, the GDI method gains simpler design, fewer transistor of the structure, and lower power dissipation [34].

Table 1: Several functions which are implemented by the basic GDI cell [34]

N	P	G	D	FUNCTION
$'\mathbf{0}'$	B	A	$\bar{A}B$	F1
$\boldsymbol{B}$	$'1'$	A	$\bar{A}+B$	F2
$'\mathbf{1}'$	B	A	$A+B$	OR
$\boldsymbol{B}$	$'0'$	A	AB	AND
$\boldsymbol{C}$	B	A	$\bar{A}B+AC$	MUX
$'\mathbf{0}'$	$'1'$	A	$\bar{A}$	NOT

C. Ternary Adders

Reviewing the literates introduces a simple architecture which implies several single-digit adders to implement a multi-digit adder [45]. This suffers from a long propagation delay time. A similar structure is presented by [46]. Another design including two half-adders are applied to generate the sum where a standalone circuit is utilized to generate the carry signal. The carry is ternary in nature and it is propagated to the next stage [47]. In some ternary adders provided in the literates, a ternary decoder is utilized to generate the binary version of the input. The three outputs of the decoder $(Y^0.Y^1.Y^2)$ are created according to the input (Y) as in (1). Since there are two possible states of the decoder outputs, the binary logic gates are utilized to generate the intermediate binary values. Then, these intermediate binary values produce the ternary sum/carry. The adder presented in [35] has a simple structure. A fast carry generation block is included in the design. Hence, an improved overall delay for multi-digit adders is expected spending large average power consumption. A multi-digit adder is introduced by [36] in which two half-adders are applied to produce the sum value. It applies a self-governing circuit to create the carry. The carry signal is ternary in nature while it needs to be transferred to the next stage. The most important drawback of the design is huge power consumption and a large amount of delay. Why so at any stage of the adder, a voltage divider is applied made the ternary carry. An energy efficient single-digit/multi-digit adder is illustrated in [36]. In the first stage of the architecture, positive and negative ternary complements of the inputs are generated. Then, the outputs of the first stage and the original inputs are fed to a network of transistors to estimate the intermediate output. This structure gains a moderate power consumption and PDP in comparison with the other existing designs.

$$\begin{aligned} y_i + y_j &= \max\{y_i.y_j\} \\ y_i.y_j &= \min\{y_i.y_j\} \\ \overline{y_i} &= 2 - y_i \end{aligned} \tag{1}$$

The Proposed Multi-Digit Ternary Adder

The proposed multi-digit ternary (multi-trit) adder applies some intermediate binary calculations to perform the operation. At each stage, two decoders are used to prepare the intermediate binary signals from the inputs. Then, the intermediate binary signals are applied to a half adder circuit. The outputs of the half adder are also binary signals which in turn drive the final sum generator circuit. The gate diffusion input method (GDI) method is utilized as a power efficient method to design the binary circuits. Finally, an encoder converts the binary sum to a ternary digit. The proposed structure is based on the model which is introduced in [37]. In the proposed architecture, a carry generator determines the carry-out of *i*th stage using the half-adder outputs of *i*th stage and the carry signals of the $(i-1)$ th stage. It leads to a reduction in carry propagation time while the complexity is slightly increased. Since the half adders work in parallel while a part of the carry-out is pre-calculated by the half adder, the carry propagation delay is decreased. To explain the design in detail, $(A_{N-1}.\ldots.A_1.A_0)$, $B(B_{N-1}.\ldots.B_1.B_0)$, $C_{in}$are considered as the ternary inputs. $Sum(Sum_{N-1}.\ldots.Sum_1.Sum_0)$, and *Cout* are the ternary outputs. The intermediate binary signals are expressed by Y_i^j which corresponds to *i*th digit-adder stage. There are two possible value of the intermediate binary signals: logic 2 (if $Y = j$) or logic 0 (if $Y \neq j$), where j {0, 1, 2}. For instance, A_0^1 corresponds to input of 0th digit-adder stage whose value is logic 2 only if ternary signal *A* is equal to logic 2. Fig. 2, shows the block diagram of the proposed multi-digit ternary adder for the ith stage. In this structure, ternary inputs are decoded to binary signals. A binary half adder computes the intermediate signals half-sum (HS) and half-carry (HC) which in turn are used to compute the final sum/carry signals in the binary sum/carry generator block. Finally, an encoder converts the binary signals to a ternary value. The binary operations, which are applied to compute the HS and HC signals, are shown in Fig. 3 [38]. A power and delay optimized decoder are designed to generate the mutually exclusive binary signals as in (1). In this design, an NTI is

used to calculate A_i^0, a pair of PTI-GDI inverter is used to compute A_i^2 and finally a GDI NOR is applied to calculate A_i^1.

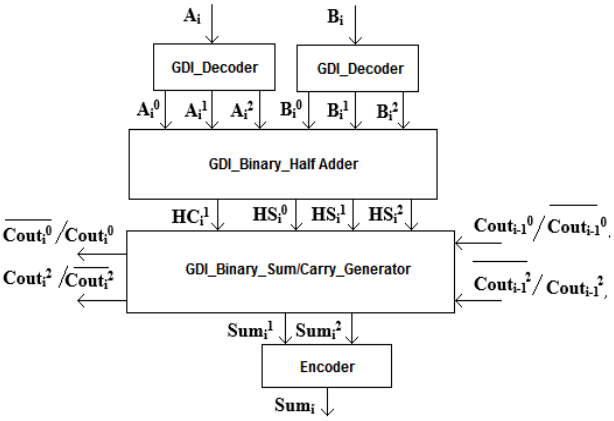

Fig. 2: The ith stage block diagram of the proposed ternary adder.

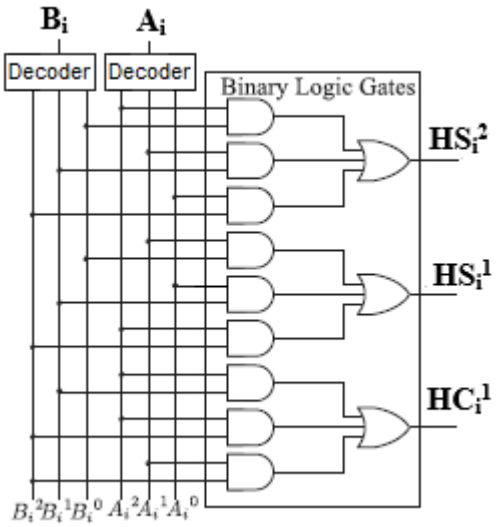

Fig. 3: The binary operations of the half adder to calculate the intermediate binary signals [38].

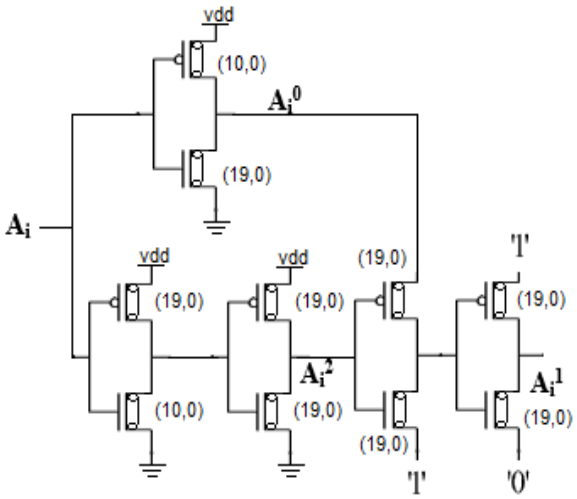

Fig. 4: The proposed GDI-based decoder.

The transistor level implementation of the proposed GDI-based decoder is shown by Fig. 4. These binary signals are fed to GDI-binary half adder to compute the intermediate binary signals. The proposed half adder generates mutually exclusive intermediate binary signals HS_i^0, HS_i^1 and HS_i^2. HC_i^1 represents the carry signal. Table 2 is the truth table of a ternary half adder which represent HS and HC for all of the inputs states. According to Table 2, (2)-(4) are obtained. Since HS_i^0, HS_i^1 and HS_i^2 are mutually exclusive signals, only two of these signals should be calculated. The third one could be implemented applying a NOR operation [37]. In this case, the GDI method is used to implement (2)-(4). Noting to the equations, "OR, AND, NOT" operations are implemented using the basic GDI cell.

Clearly, the transistor level implementation of the proposed GDI-binary half adder is presented by Fig. 5 where all the N-CNTs and the P-CNTs have the chirality of (19,0). The circuits in Fig. 5(a), (b), (c) and (d) are the CNTFET-based implementation of HS_i^0, HS_i^1, HC_i^1 and HS_i^2 respectively.

$$HS_i^2 = (A_i^1 + \bar{B}_i^1)\ (A_i^2 + \bar{B}_i^0)\ \ (A_i^0 + \bar{B}_i^2) \tag{2}$$

$$HS_i^1 = (A_i^1 + \bar{B}_i^0)\ (A_i^2 + \bar{B}_i^2)\ \ (A_i^0 + \bar{B}_i^1) \tag{3}$$

$$\overline{HC}_i^1 = (A_i^0 + \bar{B}_i^2)\ \ (\bar{A}_i^2 + \bar{B}_i^1) \tag{4}$$

Table 2: The truth table of a ternary half adder

A	B	HS	HC
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

Then, the intermediate binary signals are applied to the GDI-binary sum/carry generator block to calculate the sum and the carry.

There are two separated CNTFET implementation for the sum and the carry generators. The GDI method is also utilized for the binary operations. Table 3 is the truth table of the ith stage output carry ($Cout_i$) in order to the sum of

the inputs (A_i, B_i) and the previous stage carry (input carry of the ith stage: $Cout_{i-1}$).

stages while it generates $\overline{Cout_i^2}$ *and* $Cout_i^0$ for the odd stages.

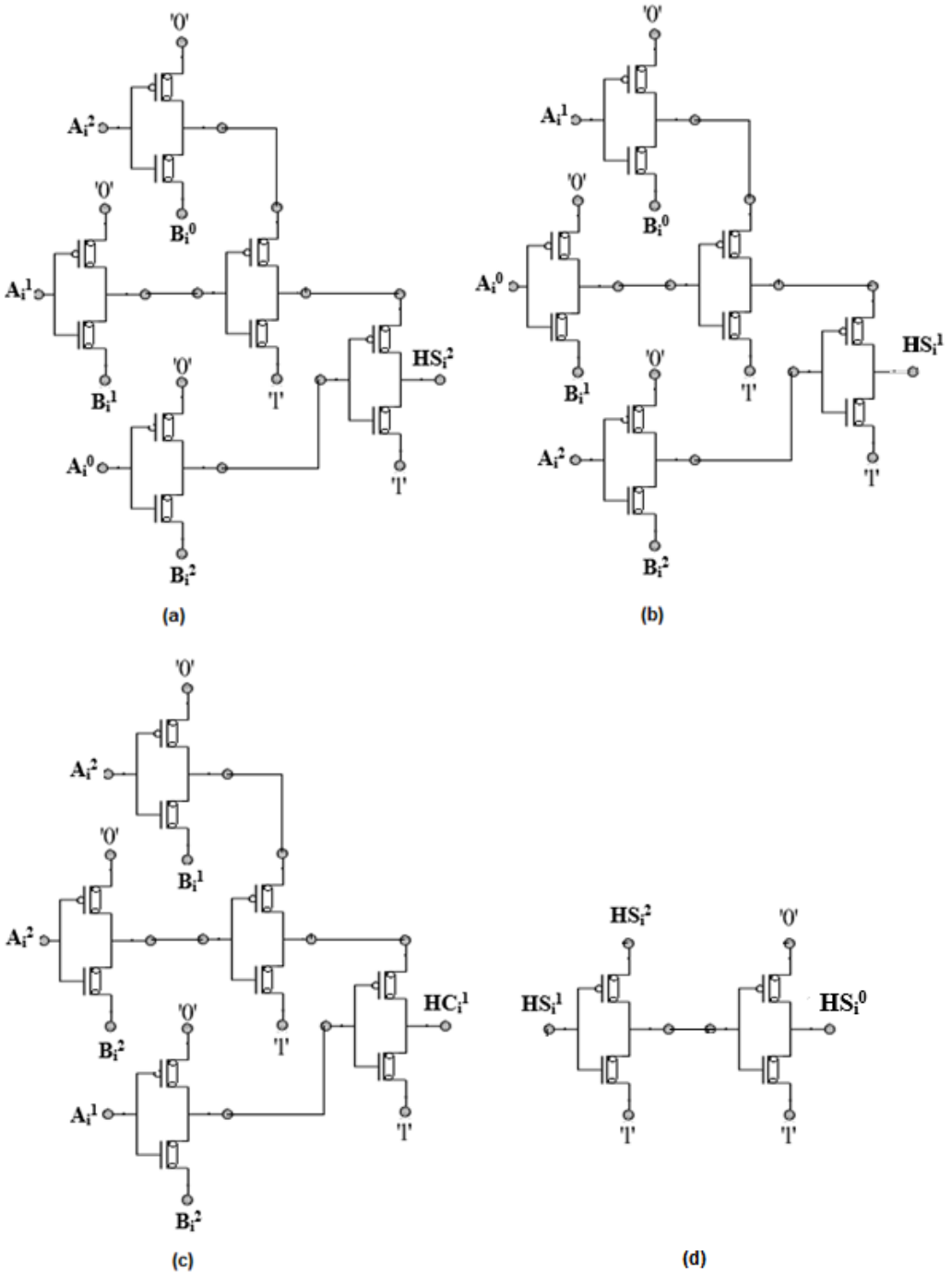

Fig. 5: The proposed GDI-binary half adder. All the CNTFETs have the chirality of (19,0).

The intermediate binary signals (HS_i, HC_i) are also included in the table. According to the truth table, the carry signal could be simply calculating by the following logical (5), (6). That is clear that only binary AND, OR and NOT are required to implement these equations. In this case, the basic CNTFET based GDI cell is used to implement the carry generator. The ith stage carry generator generates $\overline{Cout_i^0}$ *and* $Cout_i^2$ for the even

Fig. 6 shows the implementation of the carry generator in the 0th and 1th stage GDI-binary sum/carry generator block where the basic GDI cell is employed to implement the logical operations. The CNTFET based circuits in Fig. 6(a), (b), (c) and (d) are used to implement $Cout_0^0$, $Cout_1^0$, $Cout_0^2$ and $Cout_1^2$ respectively. In this design, all the CNTFETs have the chirality of (19,0).

$$Cout_i^0 = (\overline{HS_i^2} + Cout_{i-1}^0)\ \overline{HC_i^1}\ (HS_i^0 + \overline{Cout}_{i-1}^2) \quad (5)$$

$$Cout_i^2 = HS_i^1\ HC_i^1\ Cout_{i-1}^2 \quad (6)$$

2	0	2	0	1	1
3	1	0	1	1	1
4	1	1	1	1	2

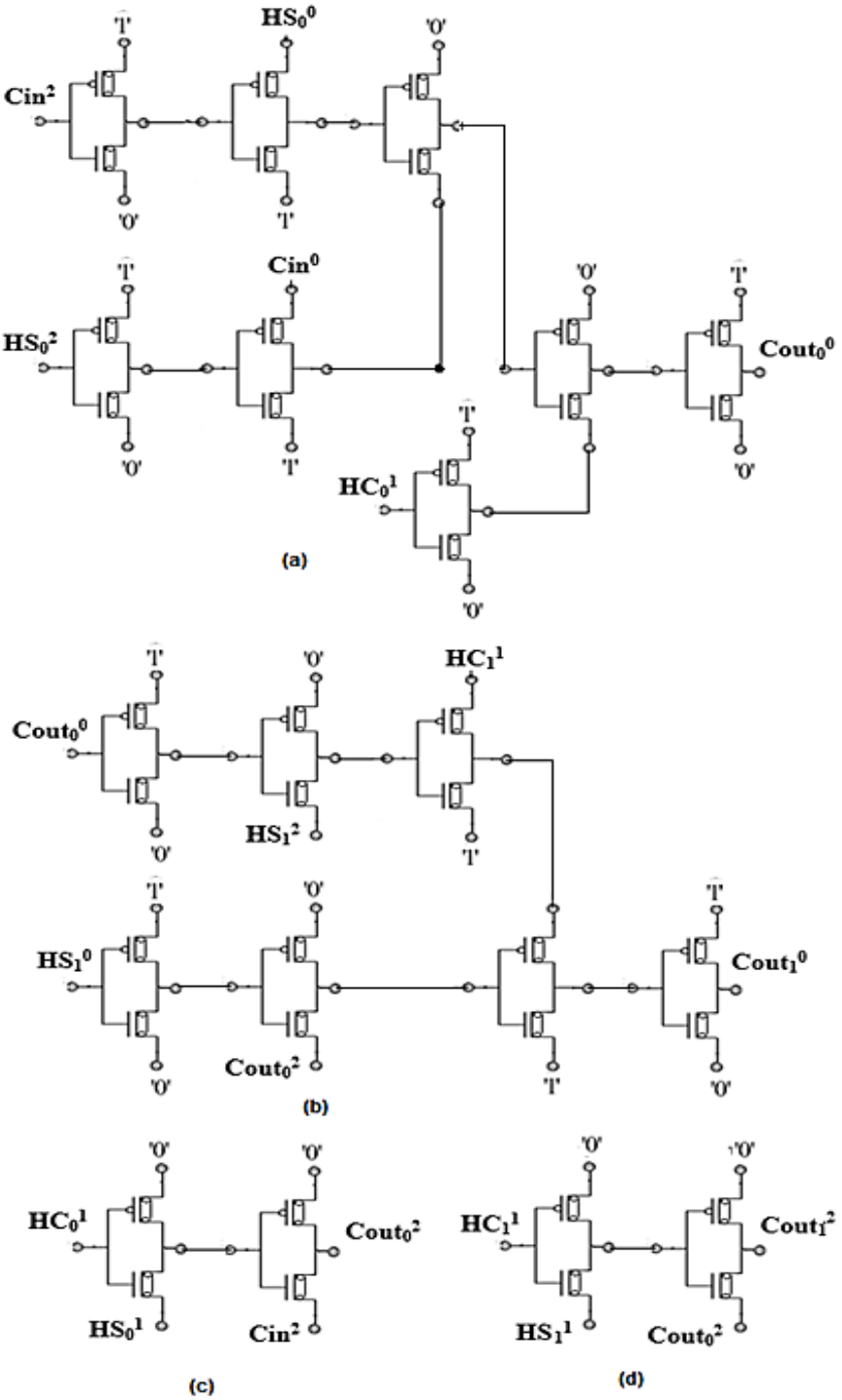

Fig.6. The proposed carry generator in the 0th and 1th GDI-binary sum/carry generator block. All the CNTFETs have the chirality of (19,0).

Table 3: The truth table of the ith stage output carry ($Cout_i$)

Sum (A_i,B_i)	HC_i	HS_i	$Cout_i$ | $Cout_{i-1=0}$	$Cout_i$ | $Cout_{i-1=1}$	$Cout_i$ | $Cout_{i-1=2}$
0	0	0	0	0	0
1	0	1	0	0	1

In the GDI-binary sum/carry generator block, a CNTFET based GDI circuit, which is similar to the HS calculation circuit in the half adder block, is used to generate the final ternary Sum (Sum_i^2, Sum_i^1).

In this case, the intermediate binary signals (HS) and the input carry of the stage is used to generate the final sum. Fig. 7(a), (b) represent the transistor level implementation to generate Sum_i^2 and Sum_i^2, while Fig. 7(c) is the implementation of $Cout_{i-1}^1$.

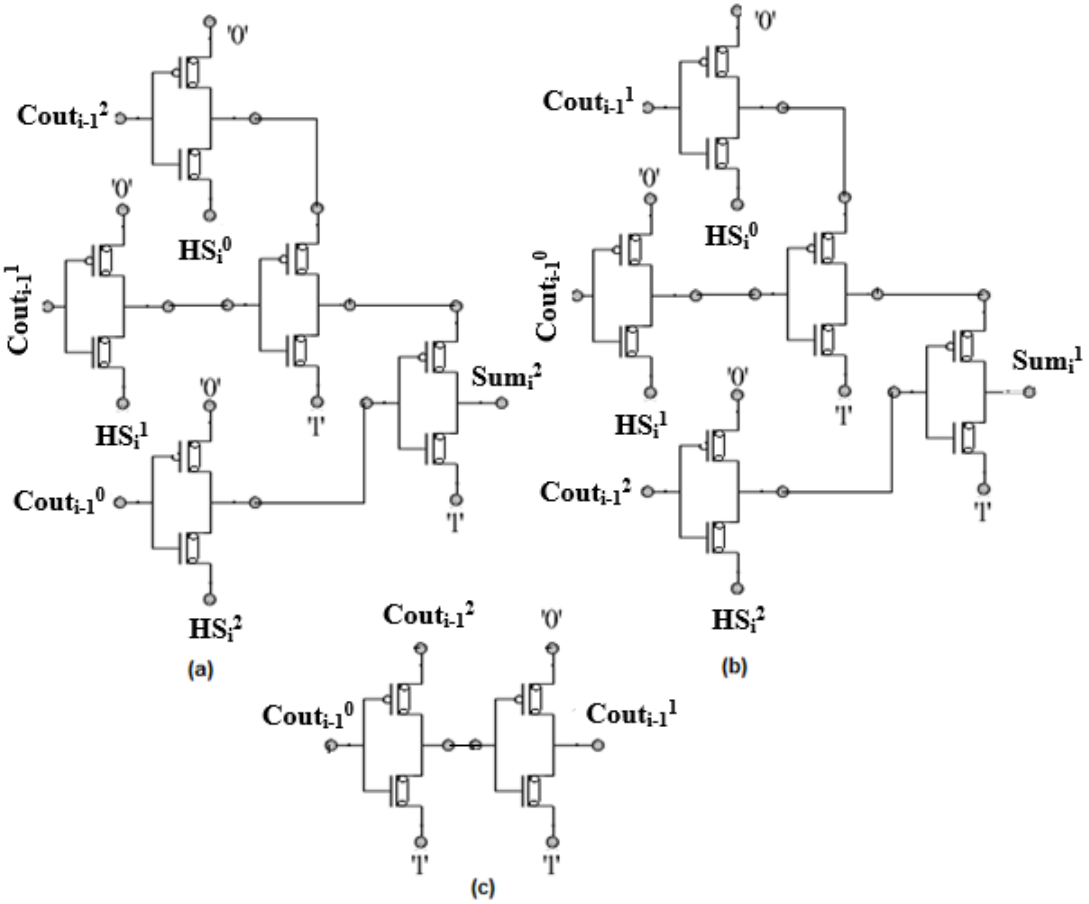

Fig. 7: The proposed final sum generator in the GDI-binary sum/carry generator block. All the CNTFETs have the chirality of (19,0).

The GDI basic cell, which is comprises of a P-CNTFET and an N-CNTFET with the chirality of (19,0), is used to implement the design. Encoder is an essential element in the architecture of a ternary adder that uses binary operations to estimate the binary intermediate signals. In this work, the power optimized encoders that are presented in [39] are applied to generate the ternary sum : stage. The implementation of the encoder which is used in the proposed design for the ternary sum generation at each stage (Sum_i) is presented by Fig. 8. Similarly, Fig. 8(b) represents the encoder which is used to implement the ternary final carry at the last stage ($Cout_{N-1}$).

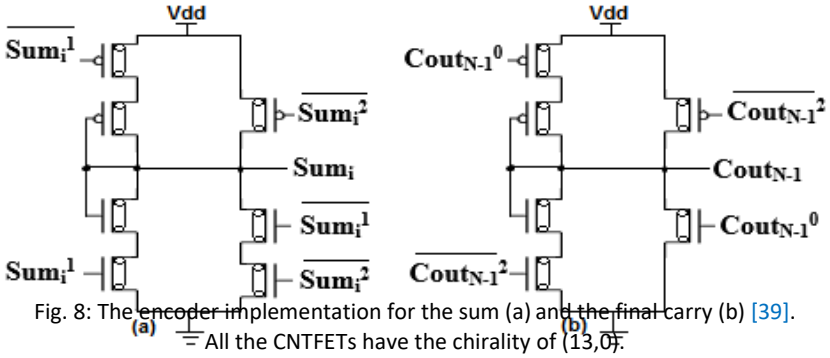

Fig. 8: The encoder implementation for the sum (a) and the final carry (b) [39].
All the CNTFETs have the chirality of (13,0).

All the CNTFETs for the both encoders have the chirality of (13,0). In the encoder circuit, which is applied in this work, when Sum_i^2 is equal to logic 2, logic 2 is generated at the output. In this case, if Sum_i^1 is equal to logic 2, a direct path between VDD and GND is created that forces the output to change to logic 1. If neither of Sum_i^2 and Sum_i^1 are logic 2 then the output is pulled down to logic 0. In this work, gate diffusion input is a method which is used to reduce the power dissipation, the propagation delay time, and the occupation area. The basic GDI cell is used to implement the GDI-decoder, GDI-binary half adder and GDI-binary sum/carry generator.

Due to this, the implementation of the proposed circuit is expected to be more efficient than previous works.

The Simulation Results and Discussion

The proposed designs are simulated in synopsis HSPICE simulator [49]. The Stanford 32 nm CNTFET technology is applied while the power supply is 0.9 v and the simulation is performed at room temperature. In this case, the pitch value of 20nm are chosen where the number of the tubes taken are 3. The main simulation parameters of the CNTs in Hspice simulator are included in Table 7. To have a meaningful comparison with the previous works, the proposed decoder, the proposed single digit adder and the proposed multi-digit adder are investigated in terms of the average power consumption, the power-delay product (PDP) and the fan out of 4 (FO4) delay. In this simulation the average power consumption is achieved by applying a random input pattern with the switching frequency of 500 MHz. The average power is composed of two types: dynamic and static. For instance, the static power consumption of the proposed single-digit adder is 0.51 uW while the average power is reported 0.88 uW. Table 4 is a comparison of the decoders.

Table 4: A comparison of the decoders

Decoder	Power (μW)	Delay-FO4 (ps)	PDP (10^{-18} J)
[38]	0.061	18.9	1.15
[37]	0.053	16.80	0.88
Proposed	0.042	15.28	0.64

Table 5: A comparison of the encoders

Encoder	Power (μW)	Delay-FO4 (ps)	PDP (10^{-18} J)
[38]	0.99	25.2	25.2
[12]	9.31	5.09	47.3
[6]	0.78	7.62	5.94
[39]	0.37	8.53	3.15

Table 6: A comparison of the single-digit adders

Single-digit adder	Power (μW)	Delay-FO4 (ps)	PDP (10^{-18} J)
[12]	32.9	37.27	1.225
[6]	2.47	26.85	0.066
[5]	1.51	134.7	0.204
[10]	7.43	34.28	0.255
[14]	2.11	29.23	0.062
[37]	1.14	37.78	0.043
Proposed	0.88	36.37	0.032

The proposed decoder design results in a reduction of 21% in power consumption, 9% in propagation delay and 22% in PDP compared with [37]. Furthermore, the fan-out requirement of the decoder in [37] is more than the proposed architecture. Hence, a circuit connected to the input of the decoder consumes lower energy in our work. The decoder which is used in the proposed design has lower power spending more delay time while the PDP is improved. Table 5 shows the simulation results of the several already provided encoders where 4 STI gate are connected as the load and a random pattern waveform as the input that results in the same output is applied. An implementation of a single-stage adder, which has no carry chain, could be done applying one stage of the proposed multi-digit adder. In some cases, it is called a full adder (FA). To have an exact consideration of FO4 delay, power and PDP, the output of the single-digit adder is connected to 4 STI as in [37] and the simulation waveform is the same as in [37]. [37] improves the results in terms of the average power and the PDP, but delay is 40% worse. The main reason for the defect is the high delay of the encoder. Although the same encoder is used in the proposed design, the overall delay is greatly reduced due to the GDI-encoder, GDI-binary half adder and GDI-binary sum/carry generator. The single-digit adder of [6] gains lower propagation delay time due to the simple encoder structure. However, the proposed single-digit adder has improved delay by 10% than [6]. In terms of the average power and the PDP, the proposed design could improve the results by 23% and 26% respectively compared with [37]. It's very important to study the effect of voltage variation on the behavior of the proposed CNT based design. Hence, the two graph of the propagation delay and the power consumption are plotted in term of the supply variation for the proposed design, [37] and [14]. Fig. 9 (a) shows that when the current of CNTFETs

increase due to the increase in voltage, the propagation delay decreases. On the other hand, as shown in Fig. 9(b), a positive change in supply voltage reduces the power consumption. Fig. 9(c) and Fig. 9(d) show how the temperature changes affect the design performance. Clearly, the temperature has a direct relation with the propagation delay and a reverse relation with the average power consumption. A metric describes the noise variation immunity

It is used to investigate the noise effect on the performance of a logic circuit. The NIC calculation is presented by [40].

The noise pulses are simply categorized by their width and amplitude [37].

A pulse with an adequate width and amplitude may cause a glitch (spurious switching).

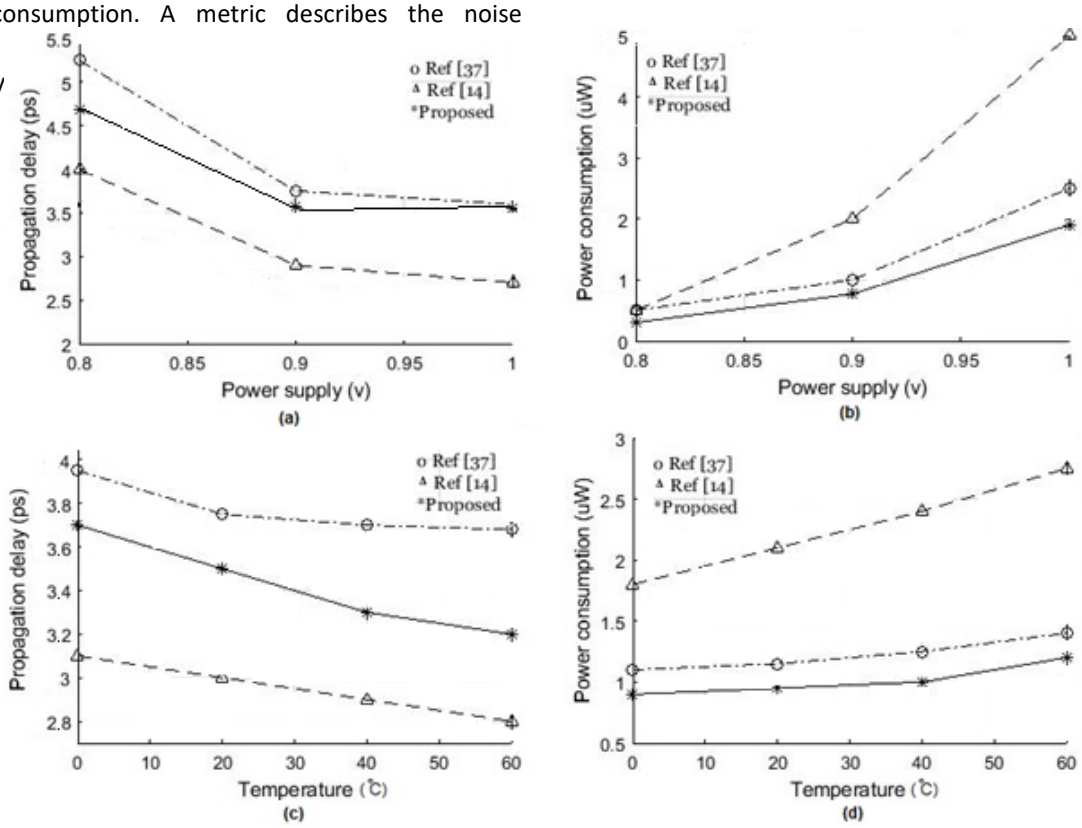

Fig. 9: The effect of the power supply (a, b) and temperature (c, d) variation on delay and power.

Fig. 10 is the NIC of the single-digit adders. Any point above the curve represents a glitch at the output. Fig. 10 clearly illustrates that the proposed single-digit adder has better noise immunity compared with [14] and [37].

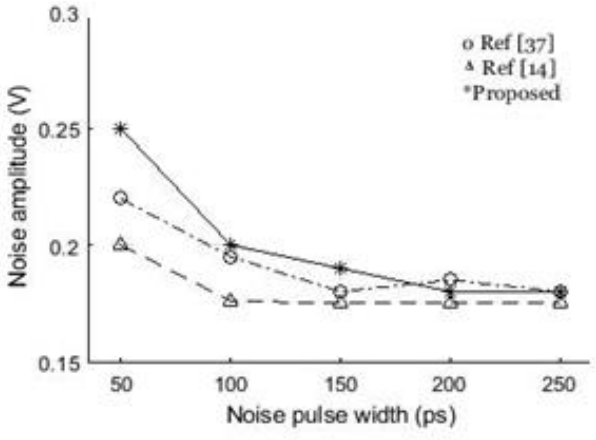

Fig. 10: NIC of single-digit adders.

To evaluate the improvement achieved in the proposed CNT-based multi-digit ternary adder, the main parameters including the power consumption, the propagation delay and the PDP are reported. In order to have a favorable comparison with previous works, two ripple carry multi-digit adder [6]-[12], two ripple carry adder which apply single-digit adder for multi-digit operations [5]-[10], and a conditional sum adder proposed by [14] are completely investigated by the same test patterns. Moreover, a lately published add/sub ternary circuit is investigated [48]. Table 8 reports the average power consumption of the several N-digit adders for N= {3,6,9,12}. According to the results, the proposed 3-digit, 6-digit, 9-digit and 12-digit adders improve the results by 10%, 25%, 27% and 19%, respectively, compared to the best design [37] in Table 8. In addition to the proposed power efficient GDI-CNT based circuits, the proposed power efficient decoder and the power efficient encoder [39], there is no encoder-decoder pairs in the carry propagation chain of the architecture [37]. There are the main reasons for the reduction of the power

consumption. A comparison of the multi-digit adders in term of the propagation delay are reported by Table 9.

Table 7: The simulation parameters of the CNTs [49]

Parameters	Descriptions	Value
Lch	Physical channel length	32nm
Lss	The length of doped CNT source-side extension region	32nm
Ldd	The length of doped CNT source-side extension region	32nm
Lgeff	The mean free path in the intrinsic CNT channel	100nm
Pitch	The distance between the centres of the two adjacent CNTs within the same device	20nm
Tox	The thickness of high-k top gate dielectric material	4nm
Csub	The coupling capacitance between the channel region and the substrate	40 uF/um
Efi	The Fermi level of the doped S/D tube	0.6 eV

Table 8: Power consumption of multi-digit adders

Power consumption (uW)				
(N)-digit adder	3	6	9	12
[12]	51.10	103.7	134.3	212.4
[6]	8.20	16.69	23.41	31.85
[5]	5.69	12.18	17.61	22.64
[10]	28.88	60.89	83.62	117.0
[14]	6.68	13.36	20.17	27.07
[37]	3.21	5.83	8.41	11.37
[48]	1.30	4.93	8.91	14.30
Proposed	2.89	4.32	6.11	9.21

Table 9: Propagation delay of multi-digit adders

Propagation delay (ps) _FO4				
(N)-digit	3	6	9	12
[12]	63.76	117.2	170.7	223.7
[6]	97.52	205.4	313.4	422.6
[5]	290.5	526.9	762.5	997.9
[10]	108.7	206.1	303.3	381.4
[14]	64.5	93.1	125.9	132.5
[37]	62.8	93.7	124.4	155.6
[48]	290.22	607.1	752.4	820.3
Proposed	53.40	74.21	101.3	122.7

In this case, the worst-case propagation delay is measured for all of the adders so that the signal changes propagate through the carry path and finally affect the $Cout_{N-1}$ and Sum_{N-1}. Unlike [5] and [6], [14] and [37] have lower complexity. Hence, an efficient carry generation/propagation results in lower propagation delay for each of them. The FO4 delay is calculated when four STI gates are connected at each output node of the critical path as in [37].

The simulation depicts that the proposed GDI based method improves the FO4-delay by 15% for N=3, 20% for N=6, 19% for N=6 and 8% for N=12 compared to the best design for each value of N. Although the overall structure of the proposed design is similar to [37], the proposed low-delay decoder and the low-complexity half adder has a great effect on reducing the overall propagation delay. The effect of the load capacitance on the propagation delay, is investigated. 1F, 2F and 3F capacitors are placed at the output node of the proposed multi-digit adder and two of the existing designs for N=6 and N=12. Fig. 11 shows the propagation delay against the load capacitance for 6-digit and 12-digit adders where the FO4- delays are also included.

The simulation reveals that there is lower dependency on the load capacitance for the both proposed 6-digit and 12-digit adders compared with the other designs. [14] has the worse result due to the limited driving capability. The product of the propagation delay and the power consumption (PDP) is the most widely used metric to validate the performance of a design. The PDP of the proposed multi-digit adder are compared with the other existing designs by Table 10. The proposed delay and power optimized decoder, half adder and carry/sum generator play an important role to reach the more efficient structure. So that the PDP is improved by 25% for N=3, 41% for N=6 and N=9 and 36% for N=12. Since the PDP is a well-known metric to evaluate the efficiency of a digital design, it is widely used in this work to compare the proposed architecture with the other existing designs. However, a circuit with low PDP (i.e. a very energy efficient design) may do the operations in a very slow manner. In this case, the energy-delay product (EDP) may be used as a much more preferable metric in some cases. To meet all aspects the EDP of the proposed and the other existing designs are reported by Table 11.

That is clear by the results that the proposed design is the most energy efficient design.

A CNTFET circuits consists of various diameter size CNTs. Due to that, it is so important to investigate the effect of the size variation. In this case Monte Carlo simulation is performed on the proposed single-digit adder and two other existing designs.

The simulation is performed with up to +-15% Gaussian distribution +- 3σ variations and 30 iterations for each

simulation. The simulation results are plotted in Fig. 12 where the power and delay variation are considered versus the diameter variation. That's clear that the proposed design depicts lower power variation compared with [14] and [37].

In term of the delay variation [14] gains the best performance.

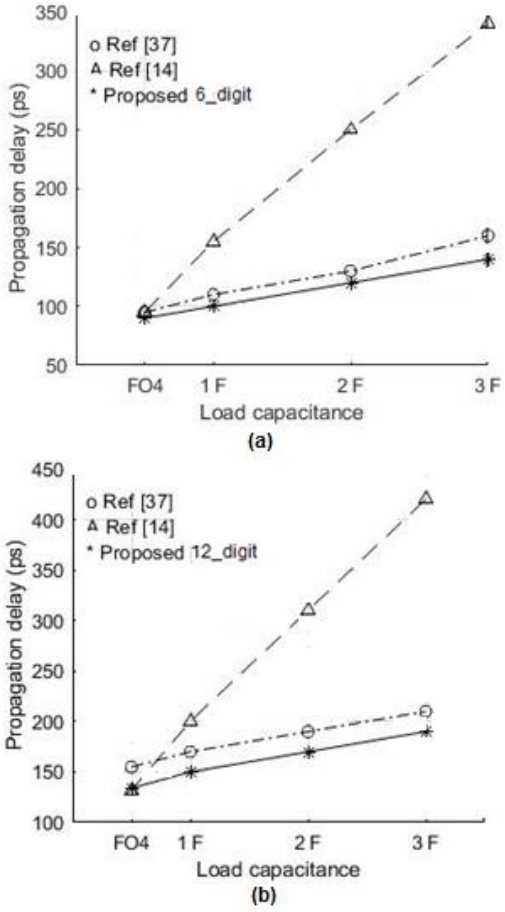

Fig. 11: Propagation delay vs load capacitance for 6-digit (a) and 12-digit (b) adders.

Table 10: PDP of multi-digit adders

Power-delay product (fJ)				
(N)-digit adder	3	6	9	12
[12]	3.26	12.2	22.9	47.5
[6]	0.80	3.43	7.34	13.4
[5]	1.66	6.42	13.4	22.6
[10]	3.14	12.6	25.4	44.6
[14]	0.43	1.24	2.54	3.59
[37]	0.20	0.55	1.05	1.77
[48]	0.38	2.99	6.70	11.73
Proposed	0.15	0.32	0.62	1.13

Table 11: EDP of multi-digit adders

Energy-delay product (x 10^-24 J.s)				
(N)-digit adder	3	6	9	12
[12]	0.21	1.43	3.9	10.6
[6]	0.08	0.7	2.3	5.6
[5]	0.48	6.42	3.4	22.5
[10]	0.34	2.6	7.7	17.01
[14]	0.03	0.12	0.32	0.48
[37]	0.012	0.051	0.13	0.27
[48]	0.11	1.1	5.04	9.6
Proposed	0.008	0.023	0.063	0.138

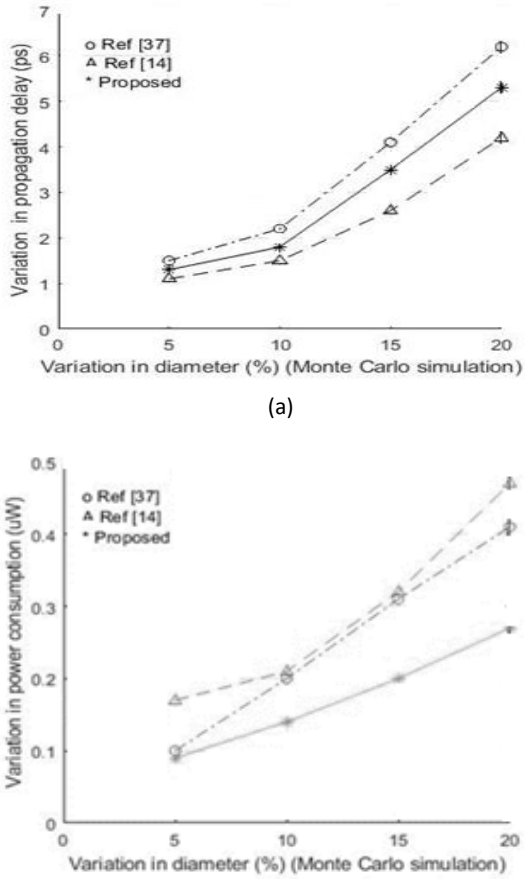

Fig. 12: Monte Carlo simulations for delay (a) and power (b).

Conclusion

A CNTFET based power and delay efficient multi-digit ternary adder has been presented in this paper. At each stage, a decoder converts the ternary inputs to the binary signals. The proposed structure includes a novel half adder to generate the intermediate binary signals. The binary signals have been used to calculate the final sum

and carry in the proposed sum/carry generator unit. The basic GDI cell has been widely used as an implementation method for the decoder, the half adder and the sum/carry generator designs.

The proposed design has been simulated in HSPICE with Stanford 32 nm CNTFET technology [49]. The simulation reveals a significant improvement in terms of power consumption (up to 27%), PDP (up to 41%) and FO4 delay (up to 20%).

Abbreviations

FA	Full Adder
MVL	Multi-Valued Logic
HS	Half Sum
HC	Half Carry
NIC	Noise Immunity Curve
GDI	Gate Diffusion Input

Author Contributions

The main idea of the paper is proposed by M.Dehyadegari and F.Razaghian and design and implementation and any of other simulation proposed by N.Ahmadzadeh Khosroshahi.

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Disclosure Statement

No potential conflict of interest was reported by the author(s).

References

[1] M. Rezaei Khezeli, M. H. Moaiyeri, A. Jalali, "Analysis of crosstalk effects for multiwalled carbon nanotube bundle interconnects in ternary logic and comparison with cu interconnects," IEEE Trans. Nanotechnology, 16(1): 107-117, 2017

[2] A. Naeemi, R. Sarvari, J. D. Meindl, "On-Chip interconnect networks at the end of the roadmap: Limits and Nanotechnology opportunities," in Proc. 2006 International Interconnect Technology Conference, 2006.

[3] P. C. Balla, A. Antoniou, "Low power dissipation MOS ternary logic family," IEEE J. Solid-State Circuits, 19(5): 739-749, 1984.

[4] L. Yu-Ming, J. Appenzeller, J. Knoch, P. Avouris, "High-performance carbon nanotube field-effect transistor with tunable polarities," IEEE Trans. Nanotechnology, 4(5): 481-489, 2005.

[5] P. Keshavarzian, R. Sarikhani, "A Novel CNTFET-based ternary full adder," Circuits Syst. Signal Process., 33: 665–679, 2014.

[6] R. Faghih Mirzaee, K. Navi, N. Bagherzadeh, "High-Efficient circuits for ternary addition," VLSI Des., 2014: 534587, 2014.

[7] S. K. Sahoo, K. Dhoot, R. Sahoo, "High performance ternary multiplier using CNTFET," 2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI): 269, 2018.

[8] B. Srinivasu, K. Sridharan, "A synthesis methodology for ternary logic circuits in emerging device technologies," IEEE Trans. Circuits Syst I: Regul. Pap., 64(8): 2146-2159, 2017.

[9] G. Hills, C. Lau, A. Wright, et al. "Modern microprocessor built from complementary carbon nanotube transistors," Nature, 572: 595–602, 2019.

[10] S. L. Murotiya, A. Gupta, "Design of high speed ternary full adder and three-input XOR circuits using CNTFETs," in Proc. 2015 28th International Conference on VLSI Design, 2015.

[11] M. H. Moaiyeri, A. Doostaregan, K. Navi, "Design of energy efficient and robust ternary circuits for nanotechnology," IET Circuits Devices Syst., 5(4): 285-296, 2011.

[12] K. Sridharan, S. Gurindagunta, V. Pudi, "Efficient multiternary digit adder design in CNTFET technology," IEEE Trans. Nanotechnology, 12(3): 283-287, 2013.

[13] C. Vudadha, S. Katragadda, P. S. Phaneendra, "2:1 Multiplexer based design for ternary logic circuits," in Proc. 2013 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), 2013.

[14] B. Srinivasu, K. Sridharan, "Carbon nanotube FET-based low-delay andlow-power multi-digit adder designs," IET Circuits Devices Syst., 11(4): 352-364, 2017.

[15] S. L. Murotiya, A. Gupta, "A novel design of ternary full adder using CNTFETs," Arab J. Sci. Eng., 39: 7839–7846, 2014.

[16] C. Vudadha, S. Phaneendra Parlapalli, M. B. Srinivas, "Energy efficient design of CNFET-based multi-digit ternary adders," Microelectronics J., 75: 75-86, 2018.

[17] B. Srinivasu, K. Sridharan, "Low-Complexity multiternary digit multiplier design in CNTFET technology," IEEE Trans. Circuits Systems II: Express Briefs, 63(8): 753-757, 2016.

[18] C. Vudadha, M. B. Srinivas, "Design of high-speed and power-efficient ternary prefix adders using CNFETs," IEEE Trans. Nanotechnology, 17(4): 772-782, 2018.

[19] C. Vudadha, P. S. Phaneendra, G. Makkena, V. Sreehari, N. M. Muthukrishnan, M. B. Srinivas, "Design of CNFET based ternary comparator using grouping logic," in Proc. 2012 IEEE Faible Tension Faible Consommation, 2012.

[20] C. Vudadha, P. S. Phaneendra, M. B. Srinivas, "An efficient design methodology for CNFET Based ternary logic circuits," in Proc. 2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), 2016.

[21] N. Ahmadzadeh Khosroshahi, M. Dehyadegari, F. Razaghian, "A high-efficiency Wallace tree based multi-trit multiplier in CNTFET technology," Int. J. Electron., 1(19): 1244-1257, 2022.

[22] S. Lata Murotiya, A. Gupta, "Hardware-efficient low-power 2-bit ternary ALU design in CNTFET technology," Int. J. Electron., 103(5): 913-927, 2016.

[23] S. L. Murotiya, A. Gupta, S. Vasishth, "Novel design of ternary magnitude comparator using CNTFETs," in Proc. 2014 Annual IEEE India Conference (INDICON), 2014.

[24] G. Hills et al., "Understanding energy efficiency benefits of carbon nanotube field-effect transistors for digital VLSI," IEEE Trans. Nanotechnology, 17(6): 1259-1269, 2018.

[25] Y. Xie, Z. Zhang, D. Zhong et al., "Speeding up carbon nanotube integrated circuits through three-dimensional architecture," Nano Res., 12: 1810–1816, 2019.

[26] A. P. Dhande, V. T. Ingole, " Design and implementation of 2-bit ternary ALU slice," in Proc. Int. Conf. IEEE-Sci. Electron., Technol. Inf. Telecommun: 17-21, 2005.

[27] S. Lata Murotiya, A. Gupta, “Design of CNTFET-based 2-bit ternary ALU for nanoelectronics”, Int. J. Electron., 101(9): 1244-1257, 2014.

[28] S. Lata Murotiya, A. Gupta, “Hardware-efficient low-power 2-bit ternary ALU design in CNTFET technology”, Int. J. Electron., 103(5): 913- 927, 2016.

[29] T. Sharma, L. Kumre, “Energy-Efficient ternary arithmetic logic unit design in CNTFET technology,” Circuits Syst. Signal Process. 39: 3265–3288, 2020.

[30] A. Morgenshtein, A. Fish, A. Wagner, "Gate-diffusion input (GDI)-a novel power efficient method for digital circuits: a design methodology," in Proc. 14th Annual IEEE International ASIC/SOC Conference (IEEE Cat. No.01TH8558), 2001.

[31] M. Shaveisi, A. Rezaei, “Design and implementation of CNTFET-Based reversible combinational digital circuits using the GDI Technique for ultra-low power applications,” BioNanoSci. 10: 1063–1083, 2020.

[32] I. Sutherland, S. Fairbanks, "GasP: a minimal FIFO control," in Proc. Seventh International Symposium on Asynchronous Circuits and Systems. ASYNC 2001, 2001.

[33] R. O. Ozdag, P. A. Beerel, "High-speed QDI asynchronous pipelines," in Proc. Eighth International Symposium on Asynchronous Circuits and Systems, 2002.

[34] A. Morgenshtein, M. Moreinis, R. Ginosar, "Asynchronous gate-diffusion-input (GDI) circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 12(8): 847-856, 2004.

[35] K. Sridharan, S. Gurindagunta, V. Pudi, "Efficient multiternary digit adder design in CNTFET technology," IEEE Trans. Nanotechnology, 12(3): 283-287, 2013.

[36] R. Faghih Mirzaee, K. Navi, N. Bagherzadeh, "High-efficient circuits for ternary addition," VLSI Design, 2014: 534587, 2014.

[37] C. Vudadha, S. Phaneendra Parlapalli, M. B. Srinivas, “Energy efficient design of CNFET-based multi-digit ternary adders,” Microelectronics J., 75: 75-86, 2018.

[38] S. Lin, Y. Kim, F. Lombardi, "CNTFET-Based design of ternary logic gates and arithmetic circuits," IEEE Trans. Nanotechnology, 10(2): 217-225, 2019.

[39] C. Vudadha, P. S. Phaneendra, M. B. Srinivas, "An efficient design methodology for CNFET based ternary logic circuits," in Proc. 2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), 2016.

[40] F. Sharifi, M. H. Moaiyeri, K. Navi, N. Bagherzadeh, “Robust and energy-efficient carbon nanotube FET-based MVL gates: A novel design approach”, Microelectronics J., .46(12): Part A, 2015.

[41] P. Soleimani Abhari, F. Razaghian, "A novel median based image impulse noise suppression system using spiking neurons on FPGA," Comput. Methods Biomech. Biomed. Eng.: Imaging Visualization, 8(6): 631-640, 2020.

[42] P. Soleimani Abhari, F. Razaghian, "Hardware implementation of LIF and HH spiking neuronal models," Signal Process. Renewable Energy, 3(1): 35-42, 2019.

[43] P. Soleimani ABHARI, M. Dosaranian Moghadam, "Design and Simulation of a modified 32-bit ROM-based direct digital frequency synthesizer on FPGA," AUT J. Electr. Eng., 47(1): 23-29, 2015.

[44] P. Soleimani Abhari, F. Razaghian, S. Talebi Toti, "Single spiking neuron as direct digital frequency synthesizer," Signal Process. Renewable Energy, 3(3): 73-81, 2019.

[45] P. Keshavarzian, R. Sarikhani, “A novel CNTFET-based ternary full adder”, Circ. Syst. Signal Process. 33 (3): 665-679, 2014.

[46] S. L. Murotiya, A. Gupta, “Design of high speed ternary full adder and three-input XOR circuits using CNTFETs, in Proc. 2015 28th International Conference on VLSI Design, 2015.

[47] R. F. Mirzaee, K. Navi, N. Bagherzadeh, “High-efficient circuits for ternary addition”, VLSI Des., 2014: 534587, 2014.

[48] S. Rani, Suman, B. Singh, "Cntfet based 4-trit hybrid ternary adder-subtractor for low power & high-speed applications," Silicon, 14: 689–702, 2022.

[49] J. Deng, H. S. P. Wong, “A compact SPICE model forcarbon-nanotube field-effect transistors including nonidealitiesand its application—Part II: Full device model and circuitperformance benchmarking,” IEEE Trans. Electron. Devices, 54(12): 3195–3205, 2007.

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