Journal of Electrical and Computer Engineering Innovations
(JECEI)
Journal homepage: http://www.jecei.sru.ac.ir

Research paper

Novel Ultra-Low-Power Mirrored Folded-Cascade Transimpedance Amplifier

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Article Info

Article History:

Received 06 June 2022
Reviewed 15 July 2022
Revised 18 August 2022
Accepted 26 September 2022

Keywords:

Trans-impedance amplifier
Folded-mirror
Optical receiver
Folded-cascade
Ultra-low-power

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Abstract

Background and Objectives: In this paper, a novel structure as a Folded-Mirror (FM) Trans-impedance Amplifier (TIA) is designed and introduced for the first time based on the combination of the current-mirror and the folded-cascade topologies. The trans-impedance amplifier stage is the most critical building block in a receiver system. This novel proposed topology is based on the combination of the current mirror topology and the folded-cascade topology, which is designed using active elements. The idea is to use a current mirror topology at the input node. In the proposed circuit, unlike many other reported designs, the signal current (and not the voltage) is being amplified till it reaches the output node. The proposed TIA benefits from a low input resistance, due to the use of a diode-connected transistor, as part of the current mirror topology, which helps to isolate the dominant input capacitance. So, as a result, the data rate of 5Gbps is obtained by consuming considerably low power. Also, the designed circuit employs only six active elements, which yields a small occupied chip area, while providing 40.6dBΩ of trans-impedance gain, 3.55GHz frequency bandwidth, and 664nArms input-referred noise by consuming only 315µW power using a 1V supply. Results justify the proper performance of the proposed circuit structure as a low-power TIA stage.

Methods: The proposed topology is based on the combination of the current mirror topology and the folded-cascade topology. The circuit performance of the proposed folded-mirror TIA is simulated using 90nm CMOS technology parameters in the Hspice software. Furthermore, the Monte-Carlo analysis over the size of widths and lengths of the transistors is performed for 200runs, to analyze the fabrication process.

Results: The proposed FM TIA circuit provides 40.6dBΩ trans-impedance gain and 3.55GHz frequency bandwidth, while, consuming only 315µW power using a 1V supply. Besides, as analyzing the quality of the output signal in the receiver circuits for communication applications is vital, the eye-diagram of the proposed FM TIA for a 50µA input signal is opened about 5mV, while, for a 100µA input signal the eye is opened vertically about 10mV. So, the vertical and horizontal opening of the eye is clearly shown. Furthermore, Monte-Carlo analysis over the trans-impedance gain represents a normal distribution with the mean value of 40.6dBΩ and standard deviation of 0.4dBΩ. Also, the value of the input resistance of the FM TIA is equal to 84.4Ω at low frequencies and reaches the value of 75Ω at -3dB frequency. The analysis of the effect of the feedback network on the value of the input resistance demonstrates the input resistance in the absence of the feedback network reaches up to 1.4MΩ, which yields the importance of the existence of the feedback network to obtain a broadband system.

Conclusion: In this paper, a trans-impedance amplifier based on a combination of the current-mirror topology and the folded-cascade topology is presented, which amplifies the current signal and converts it to the voltage at the output node. Due to the existence of a diode-connected transistor at the input node, the input resistance of the TIA is comparatively small. Furthermore, four out of six transistors are PMOS transistors, which represent less thermal noise in comparison with NMOS transistors. Also, the proposed Folded-Mirror topology occupies a relatively small area on-chip, due to the fact that no passive element is used in the feedforward network. Results using 90nm CMOS technology parameters show 40.6dBΩ trans-impedance gain, 3.55GHz frequency bandwidth, 664nArms input-referred noise, and only 315µW power dissipation using a 1volt supply, which indicates the proper performance of the proposed circuit as a low-power building block.

Introduction

The beam of light, as the fastest signal carrier, was always an attractive candidate for communication systems. Optical fibers, as a proper medium for transferring a beam of light, introduce better performance in terms of crosstalk, bandwidth, electromagnetic interference, and channel loss in comparison with conventional mediums [1].

Also, the rapid increase in the transit frequency of CMOS technologies made deep-submicron CMOS devices a proper candidate to provide an acceptable level of integration besides a proper level of speed and low cost.

In Fig. 1 the building block of the transmitter and the optical receiver system are demonstrated. At the receiver stage after the photodiode, the trans-impedance amplifier (TIA) stage, as the most critical building block in a receiver system, is shown in gray. The photodiode receives the optical signal and proportionally produces a weak signal current.

At the Far-end, a weak signal current in the range of microampere is detected [1], [2], which requires to be amplified with low noise and a proper bandwidth, to be detectable in the digital circuitry. Of course, nonlinearities and second-order effects besides the trade-offs among gain, bandwidth, speed, noise, power consumption, and voltage headroom are part of the challenges the designer must consider when using deep-submicron technologies. Furthermore, a large parasitic capacitance in the input node of the TIA limits the frequency bandwidth at the beginning [4]-[10].

Of course, many researchers have published many different structures such as regulated cascade (RGC) structures [3], [11]-[13] to compensate for the effect of this large parasitic capacitance. In [11]-[13] broadband circuits are introduced using passive inductors and resistors to enlarge the bandwidth, which of course requires a large occupied area on the chip.

Additionally, high voltage headroom is required for RGC structures at high-speed applications, which is not possible due to the occurrence of the quantum tunneling phenomena in nanometer CMOS technologies.

In [14] a method, which converts the transconductance of a transistor into a trans-impedance, is proposed.

In this method, no resistor is required to do the conversion, and a further degree of freedom is obtained in comparison with previously published circuit structures, but the usage of passive inductors in this structure yields a large occupied chip area. Moreover, a π-network as the TIA stage is proposed in [15] alongside a shunt amplifier based on folded-cascade structures, which benefits from a high gain and low-noise characteristic, while, suffering from high power consumption and a large occupied chip area due to the use of passive inductors.

Also inverter [5], [6]-[21] is another attractive structure used in designing TIA stages. In [5], a cascaded circuit structure is employed in a conventional inverter structure, which eliminates the Miller capacitance and enlarges the bandwidth, but limits the output swing. Furthermore, a three-stage cascaded push-pull conventional inverter, which uses a series inductive peaking technique to extend the bandwidth, is proposed in [16].

Of course, this technique also requires a largely occupied area on-chip. Additionally, an inverter employing a diode-connected NMOS and a cascaded PMOS is proposed in [17], which provides a wide dynamic range with 227MHz frequency bandwidth.

Moreover, a conventional inverter employing active feedback with an extra gain stage is proposed in [18], while, a similar circuit is proposed in [19], which uses an inverter structure in its input stage, followed by a 1.5KΩ feedback resistor.

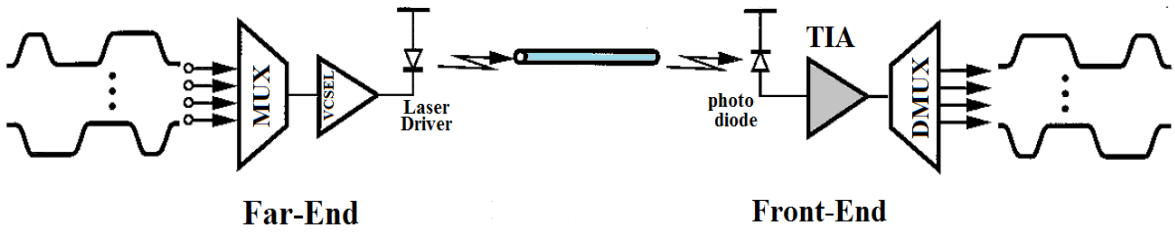


Fig. 1: Location of the TIA stage in an optical receiver system [1].

Clearly, a 1.5KΩ resistor occupies a considerable area on-chip. Also, a conventional inverter is employed as the booster amplifier in an RGC structure [19], which introduces low input resistance that isolates further the parasitic capacitance of the photodiode, while, suffering from the miller capacitance in the inverter stage.

In [7] a current-mirror-based TIA is proposed, which amplifies the current signal and covers it to the voltage at the output node, unlike many other reported TIAs, which convert the current signal to a voltage signal at the begging, and then try to amplify the voltage.

In this paper, a new trans-impedance amplifier namely "Folded-Mirror" (FM) is proposed, which benefits from a low input resistance (due to the use of a diode-connected transistor at the input node), and a relatively low noise behavior (due to the use of PMOS transistors instead of NMOS transistors). As the time constant of the dominant pole is reduced due to the small value of the input resistance, the circuit is capable of providing an extended bandwidth, without the requirement of consuming extra power.

The Proposed TIA

This novel proposed topology is based on the combination of the current mirror topology and the folded-cascade topology, which is designed using active elements.

The idea is to use a current mirror topology at the input node, as in Fig. 2-1 (a), which introduces a small value of $(gm)^{-1}$ as the input resistance. Then, the signal requires to be amplified further in a cascade stage. So, a cascade stage is added to the structure, and a current source is used as its load, as in Fig. 2-1 (b). As these two stages cannot provide proper trans-impedance gain, a folded cascade structure is used instead of the cascade structure, to fold the current signal toward M5, as it is shown in Fig. 2-1 (c).

The M5 transistor, as the diode-connected load, is used in a current mirror topology to further amplify the signal, as in Fig. 2-1 (d). So, the signal is now amplified in three steps, in which M2 and M5 are used commonly in the current mirror structure and in the folded cascade structure, simultaneously. Finally, Fig. 2-1 (e) demonstrates the active type of the proposed open-loop TIA.

Fig. 2 (b) demonstrates the final version of the proposed FM TIA. The produced signal of the photodiode amplifies in a current-mirror structure (consists of M1 and M2), a folded-cascade structure (consists of M2, M3, M4, and M5) and in the second current-mirror topology (consists of M5 and M6), respectively. Usage of a current-mirror stage at the input node introduces a low input resistance, which isolates the parasitic capacitance of the photodiode. Moreover, the proper usage of the voltage-current feedback decreases the output resistance and the input resistance even more. Also, the usage of four PMOS transistors out of six transistors yields less generated thermal noise, due to the less mobility of holes in the PMOS transistors.

Moreover, Fig. 3 shows the model of the photodiode [25], [26] and Fig. 4 demonstrates the equivalent circuit of the proposed FM TIA.

So, the open-loop trans-impedance gain (AV) of the FM TIA can be calculated as follows:

$$A_V = \frac{g_{m2}}{g_{m1}} \times \frac{g_{m6}}{g_{m5}} \times r_{o6} \tag{1}$$

which, g_m represents the transconductance, and r_o represents the drain-source resistance of the MOSFET.

Considering the fact that the gate-source voltage of M1 and M2 are equal ($V_{gs1} = V_{gs2}$) and also $V_{gs5} = V_{gs6}$, and M1, M2, M5 and M6 are PMOS transistors ($\mu_{p1} = \mu_{p2}$,$C_{ox5} = C_{ox6}$) with a same length at a specific technology ($L_1 = L_2$, $L_5 = L_6$), (1) can be simplified as follows:

$$A_V = \frac{w_2}{w_1} \times \frac{w_6}{w_5} \times r_{o6} \tag{2}$$

which $\left(\frac{w_2}{w_1} \times \frac{w_6}{w_5}\right)$ defines the current amplification.

The input resistance of the proposed TIA is comparatively small, due to the use of the diode-connected transistor M1, which yields the value of $\left(\frac{1}{g_{m1}}\right)$ as the input resistance, for the open-loop FM TIA. So, the input resistance of the closed-loop FM TIA ($R_{in,f}$) can be calculated as follows:

$$R_{in,f} = \frac{\frac{1}{g_{m1}}}{1 + A_V . \frac{1}{R_f}} = \frac{g_{m5}\, R_f}{g_{m1}\, g_{m5}\, R_f + g_{m2}\, g_{m6}\, r_{o6}} \tag{3}$$

where R_f represents the feedback resistance.

Besides, the output resistance of the open loop FM TIA is equal to (r_{o6}).

In order to calculate the closed-loop output resistance, it can be written as follows:

$$R_{out,f} = \frac{r_{o6}}{1 + A_V \frac{1}{R_f}} = \frac{g_{m1}\, g_{m5}\, R_f\, r_{o6}}{g_{m1}\, g_{m5}\, R_f + g_{m2}\, g_{m6}\, r_{o6}} \tag{4}$$

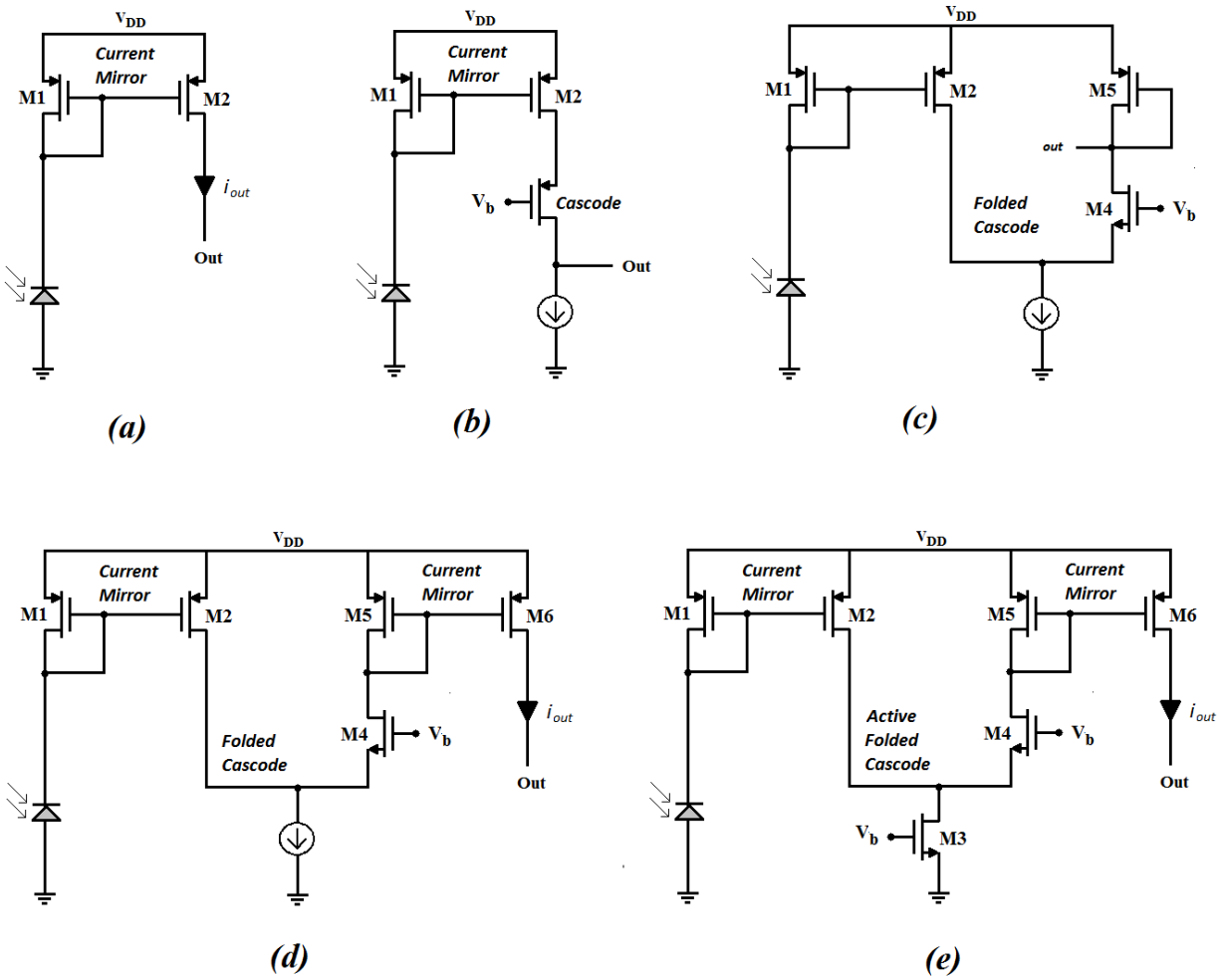


Fig. 2-1: Design Process, a) current mirror topology, b) a cascade stage is added to (a), c) a folded cascade structure instead of the cascade structure in (b), (d) a current mirror topology is added to (c), and e) the active type of the proposed open-loop TIA.

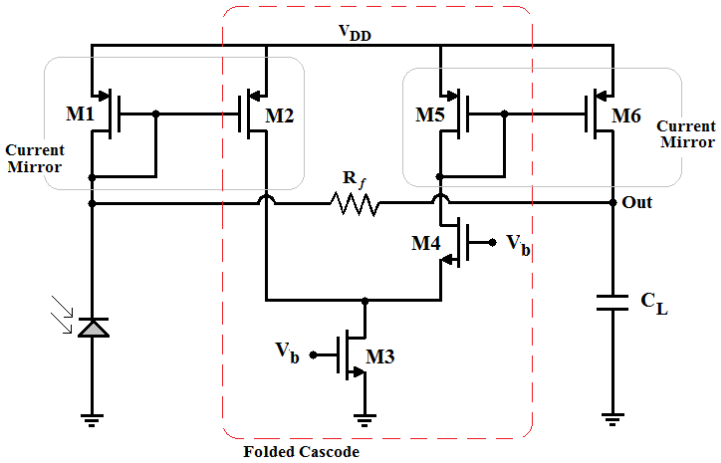


Fig. 2-2: The Final Model of the proposed TIA.

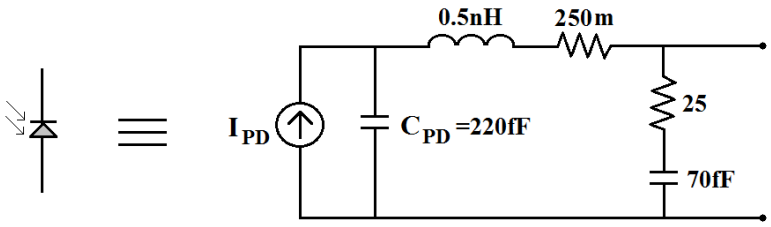


Fig. 3: Model of the Photodiode.

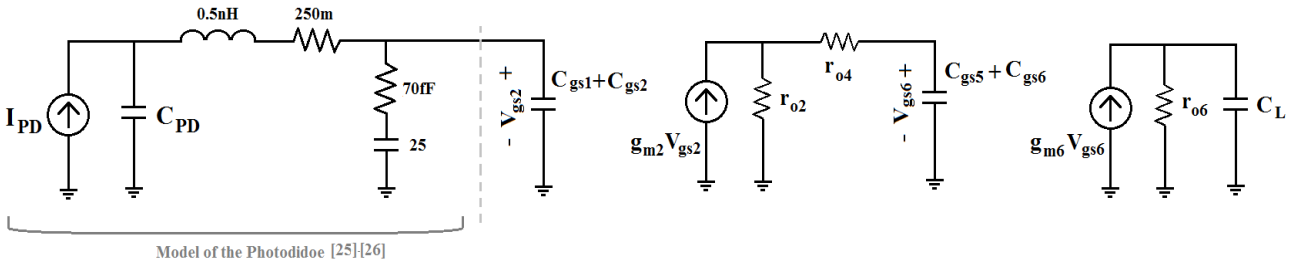


Fig. 4: Equivalent Circuit of the Proposed FM TIA.

Also, for the capacitance seen at the input and output nodes of the FM TIA, it can be written as follows:

$$C_{in} = C_{gs1} + C_{gs2} + C_{Pd} \approx C_{Pd} \tag{5}$$

$$C_{out} = C_L \tag{6}$$

which C_{gs} represents the gate-source parasitic capacitance of a MOSFET, C_{Pd} is the parasitic capacitance of the photodiode and C_L represents the load capacitance. As the parasitic capacitance of the photodiode contains comparatively a large value, it can be concluded that the input capacitance of the TIA is approximately equal to C_{Pd}.

So, in order to calculate the closed-loop trans-impedance gain of the proposed FM TIA at low frequencies, it can be written as follows:

$$A_{V,f} = \frac{A_V}{1 + A_V \frac{1}{R_f}} = \frac{g_{m2}\, g_{m6}\, R_f\, r_{o6}}{g_{m1}\, g_{m5}\, R_f + g_{m2}\, g_{m6}\, r_{o6}} \tag{7}$$

And hence, the transfer function of the proposed FM TIA can be achieved as follows:

$$A_V(S) = \frac{A_{V,f}}{\left(1 + S.C_{in}.R_{in,f}\right)\left(1 + S.C_{out}.R_{out,f}\right)} \tag{8}$$

By using (3) to (7) and considering the fact that $C_{in} \gg C_{out}$, (8) can be re-written as follows:

$$A_V(S) = \frac{g_{m2}\, g_{m6}\, R_f\, r_{o6}}{\left(g_{m1}\, g_{m5}\, R_f + g_{m2}\, g_{m6}\, r_{o6}\right)} \frac{1}{\left(1 + S.C_{Pd}\, \frac{g_{m5}\, R_f}{g_{m1}\, g_{m5}\, R_f + g_{m2}\, g_{m6}\, r_{o6}}\right)} \tag{9}$$

As (9) reveals, the proposed FM TIA is approximated as a single pole circuit, with its pole equal to $S \approx -\frac{g_{m1}.g_{m5}.R_f + g_{m2}.g_{m6}.r_{o6}}{C_{pd}.g_{m5}.R_f}$. So, the -3dB frequency can be written as follows:

$$f_{-3dB} \approx \frac{g_{m1}.g_{m5}.R_f + g_{m2}.g_{m6}.r_{o6}}{2\pi.C_{pd}.g_{m5}.R_f} \tag{10}$$

Results and Discussions

In the following, the circuit performance of the proposed folded-mirror TIA is simulated using 90nm CMOS technology parameters. The frequency response of the proposed TIA up to 10GHz is demonstrated in Fig. 5. As Fig. 5 presents, the proposed FM TIA circuit provides 40.6dBΩ trans-impedance gain and 3.55GHz frequency bandwidth, while, consuming only 315µW power using a 1V supply.

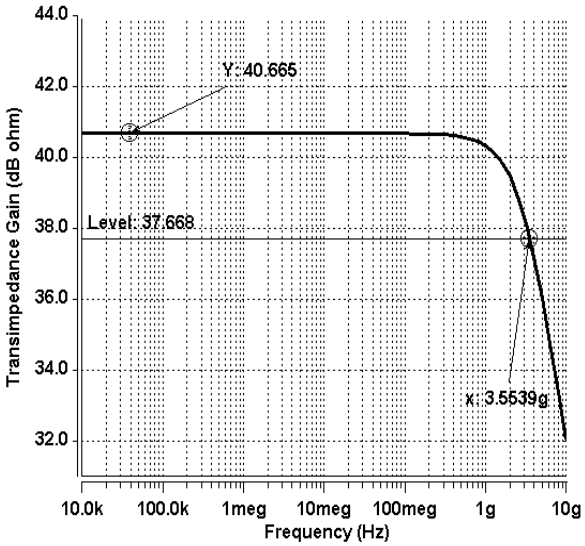
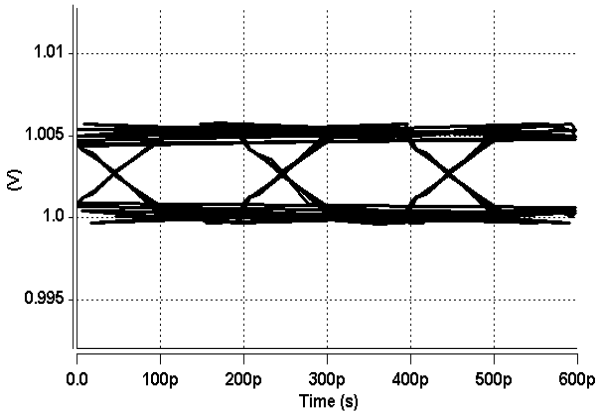


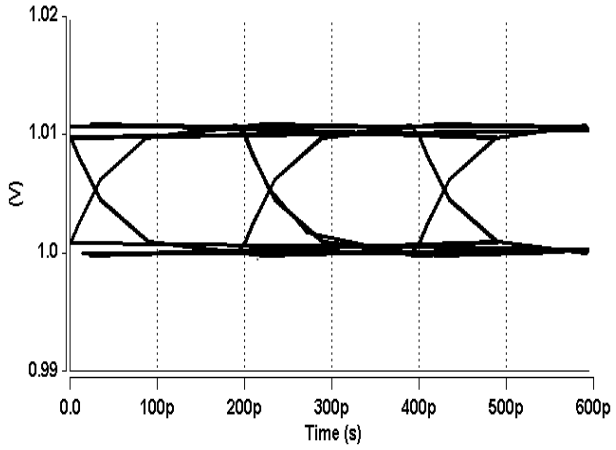
Fig. 5: Frequency Response of the proposed FM TIA.

As analyzing the quality of the output signal in the receiver circuits for communication applications is vital, the eye-diagram of the proposed FM TIA is demonstrated in Fig. 6, using Non-Return to Zero (NRZ) Pseudo-Random Bit Sequence (PRBS) 2^7-1 for two different values of 50µA and 100µA input signals, respectively. As Fig. 6 suggests for a 50µA input signal, the eye is opened about 5mV, while, for a 100µA input signal the eye is opened vertically about 10mV. So, the vertical and horizontal opening of the eye is clearly shown.

Furthermore, the Monte-Carlo analysis over the size of the widths and lengths of the transistors is performed for 200runs, to analyze the fabrication process. Fig. 7 demonstrates the results over frequency response, while, Fig. 8 demonstrates the results over the trans-impedance gain. Monte-Carlo analysis over the trans-impedance gain represents a normal distribution (the red line) with the mean value of 40.6dBΩ and standard deviation of 0.4dBΩ, as in Fig. 8.



(a)



(b)

Fig. 6: The eye-diagram of the FM TIA using NRZ PRBS for (a) 50µA and (b) 100µA input signal.

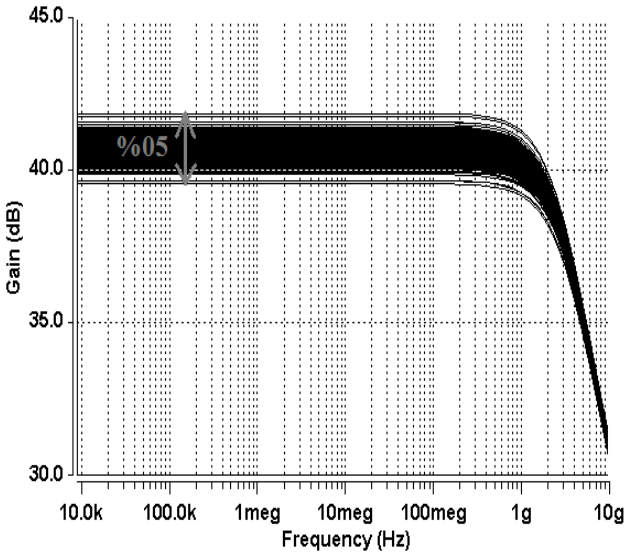


Fig. 7: Monte-Carlo Analysis over frequency response.

Also, the input resistance of the optical receivers (the TIA stage) is a challenging parameter, as discussed before. So, the input resistance of the proposed FM TIA versus frequency is shown in Fig. 9.

As it was theoretically discussed before, the input resistance of the FM TIA should be relatively small due to the existence of a diode-connected transistor at the input node, and the use of a voltage-current feedback. So, Fig. 9 displays the value of the input resistance of the FM TIA, which is equal to 84.4Ω at low frequencies and reaches the value of 75Ω at -3dB frequency.

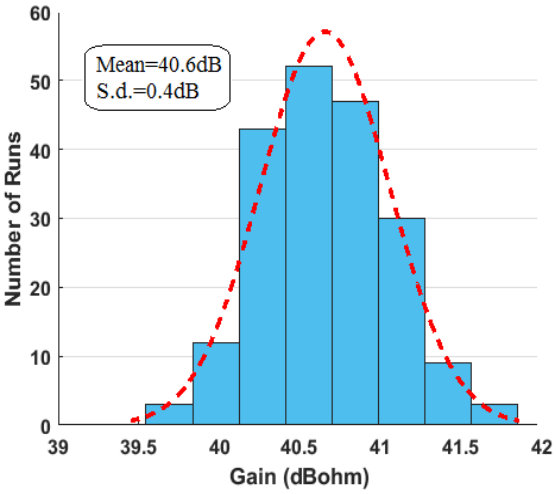


Fig. 8: Monte-Carlo Analysis over transimpedance gain.

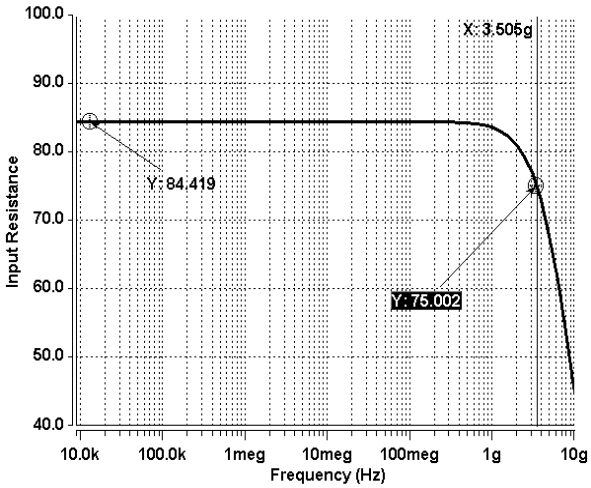


Fig. 9: Input resistance of the FM TIA.

Furthermore, the effect of the feedback network on the value of the input resistance is analyzed and summarized in Table 1. As it can be concluded from Table 1, the input resistance in the absence of the feedback network reaches up to 1.4MΩ, which yields the importance of the existence of the feedback network to obtain a broadband system.

Table 1: effect of the feedback network on the input resistance

	The Open-loop TIA	The Closed-loop TIA
Input resistance (@low freq.)	84.4Ω	1.4MΩ

As it is important that a broadband system can operate properly in a reasonable range of temperature, the effect of temperature variations on the frequency response of the proposed FM TIA is analyzed, and the results are given for three different values of -30ºC, +30ºC, and +90ºC in Fig. 10. As Fig. 10 suggests, increasing the temperature results in an increased gain while resulting in a decreased frequency bandwidth, which shows the trade-off between the trans-impedance gain and the frequency bandwidth. Table 2 numerically summarizes this analysis.

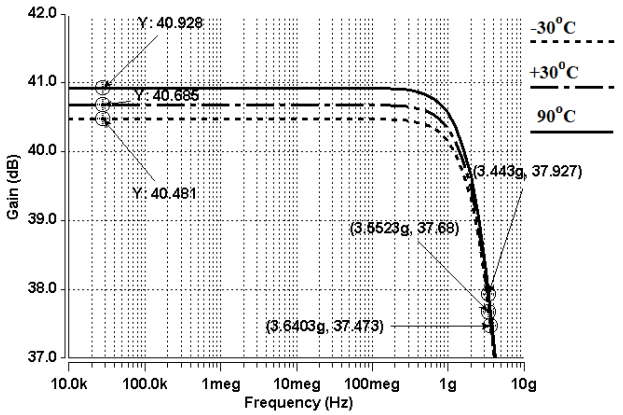


Fig. 10: Effect of temperature variations on frequency response.

Table 2: Effect of temperature variation on transimpedance gain, frequency bandwidth and power consumption

	-30ºC	+30ºC	+90ºC
Transimpedance Gain	40.4dBΩ	40.6dBΩ	40.9dBΩ
Frequency Bandwidth	3.64GHz	3.55GHz	3.44GHz
Power Consumption	274µW	318µW	355µW

Moreover, the sensitivity of the proposed FM TIA to VDD is analyzed and the results are given in the following. In Fig. 11, the result of %10 variations of the supply voltage (VDD) is shown over frequency response. According to Fig. 11, the trans-impedance gain varies from 40.34dBΩ to 41.02dBΩ (varies about 0.68dB), while, the frequency bandwidth varies from 3.425GHz to 3.695GHz (270MHz). Also, Table 3 summarizes the numerical analysis of supply voltage variations. As Table 3 reveals, a %10 reduction in the value of the supply voltage (from VDD to 0.9VDD), results in 0.06 less power dissipation, and 0.04 less bandwidth, while, 0.01 more gain value can be achieved.

Table 3: Effect of V_{DD} variation on Transimpedance gain, frequency bandwidth and power consumption

	$1.1V_{DD}$	V_{DD}	$0.9V_{DD}$
Transimpedance Gain	40.34dB	40.66dB	41.02dB
Frequency Bandwidth	3.69GHz	3.56GHz	3.42GHz
Power Consumption	413µW	315µW	298µW

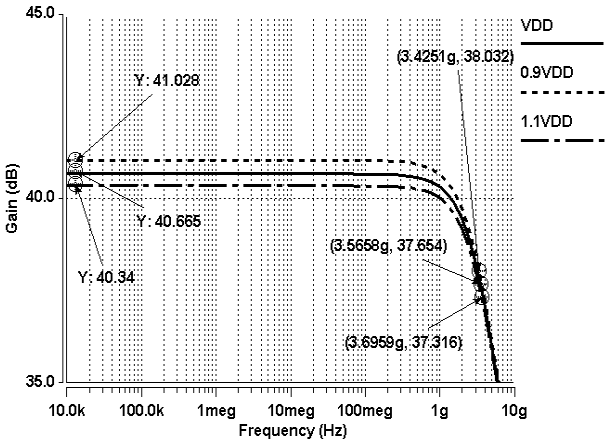


Fig. 11: Supply voltage variations Vs. frequency response.

Noise Analysis

The demonstration of noise sources in the block diagram of the proposed FM TIA as in Fig. 12, provides a better understanding of the noise performance in this circuit. According to (11), input-referred noise of the proposed FM TIA circuit structure can be calculated as the sum of noise in the core of the TIA, and the feedback network, as follows [1]:

$$\overline{I_{n,in}^2} = \overline{I_{n,Rf}^2} + \frac{\overline{V_{n,Core}^2}}{R_f^2} \tag{11}$$

which

$$\overline{I_{n,Rf}^2} = \frac{4KT}{R_f} \tag{12}$$

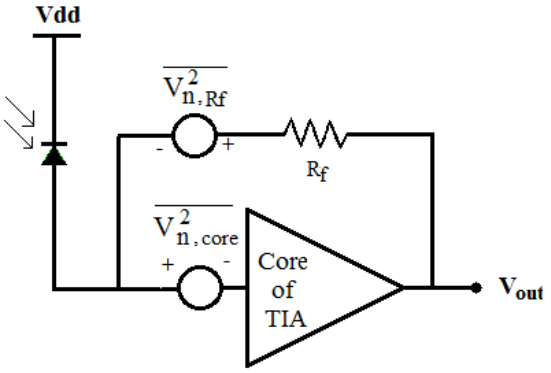


Fig. 12: Demonstration of noise sources in the block diagram of the FM TIA.

Now, according to (11) calculation of the noise of the TIA core is required. So, a current source is put in parallel with the drain-source terminals of transistors, to demonstrate the produced thermal noise in each transistor, as in Fig. 13. First of all, it should be noted that M1 is operating in the triode region, due to the fact that it is used as a diode-connected transistor. Hence, the generated noise of M1 is shunted to the ground [27]. So, according to the shunted parasitic capacitance of the photodiode, the produced thermal noise of M1 can be calculated as follows:

$$\overline{I_{n,M1}^2} = \frac{KT}{C_{Pd}} \tag{13}$$

which, K is the Boltzmann constant and T is the temperature.

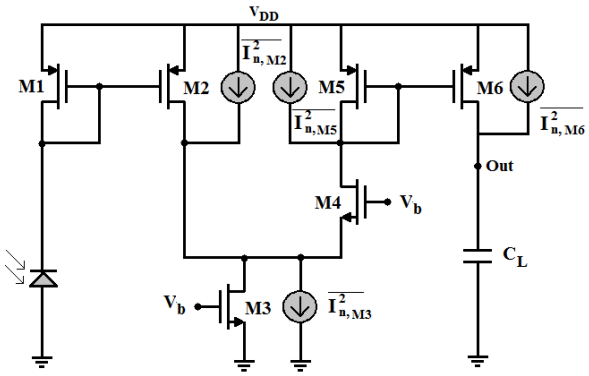


Fig. 13: representation of noise in the core of the FM TIA by current sources.

Besides, as M4 forms a cascade structure, the thermal noise generated by M4 is negligible [27]; due to the fact that if the channel length modulation of M4 is neglected, it can be said that $I_{n2} + I_{D2} = 0$, and hence M4 does not affect $V_{n,out}$.

So, considering (11) and Fig. 13, $\overline{V_{n,Core}^2}$ can be calculated as follows:

$$\overline{V_{n,Core}^2} = 4KT\gamma\left[\frac{g_{m2}+g_{m3}+g_{m5}}{|g_{m2}|^2} + \frac{g_{m6}}{\left|\frac{g_{m6}}{g_{m5}}.\frac{g_{m2}}{g_{m1}}\right|^2}\right] \tag{14}$$

where γ refers to the channel noise factor of a MOSFET.

So, in order to calculate the input-referred noise of the TIA, considering (11), (12), and (14), it can be written as follows:

$$\overline{I_{n,in}^2} = \frac{4KT}{R_f}\left[1 + \frac{\gamma}{R_f.|g_{m2}|^2}\left(g_{m2}+g_{m3}+g_{m5} + \frac{(g_{m5}.g_{m1})^2}{g_{m6}}\right)\right] \tag{15}$$

As (15) suggests, by increasing the transconductance of g_{m2}, it is possible to decrease the input referred noise of the proposed FM TIA. Additionally, the input referred noise and the output noise of the proposed TIA are shown in Fig. 14 and Fig. 15, respectively. As Fig. 14 shows, the input referred noise at low frequencies is equal to 10pA/√Hz, and reaches the value of 11.1pA/√Hz at -3dB

frequency. Also, the total input referred noise current of the proposed FM TIA is equal to 10.4pA/√Hz (664nA$_{rms}$).

As it was discussed before, the employed feedback resistor decreases the thermal noise of the FM TIA. Table 4 compares the value of the input referred noise of the proposed FM TIA with and without the feedback network. As Table 4 reveals, the feedback network considerably decreases the thermal noise current of the FM-TIA.

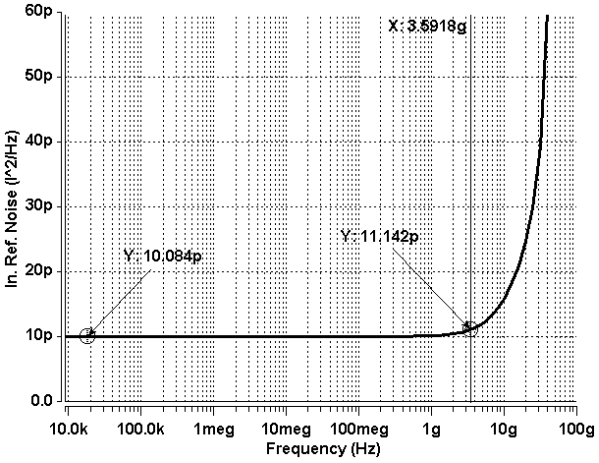


Fig. 14: Input referred noise of the FM TIA.

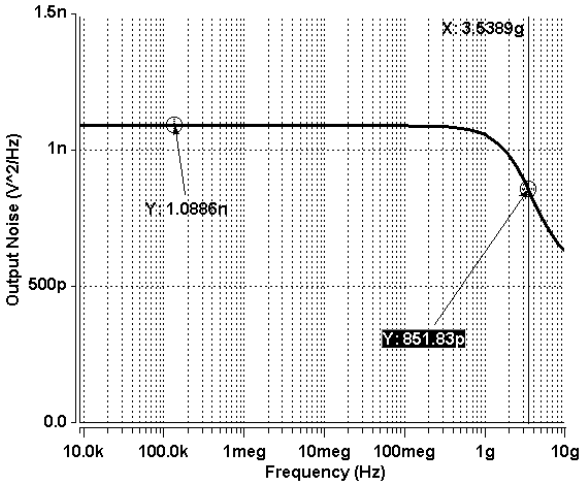


Fig. 15: Output noise of the FM TIA.

Table 4: Effect of the feedback network on the input referred noise current density

	The Open-loop TIA	The Closed-loop TIA
Input referred noise current density	664nA$_{rms}$	9.5mA$_{rms}$

Table 5: Performance comparison among the proposed TIA and other reported designs

	[14]	[15]	[22]	[23]	[24]	[28]	[29]	[30]	[31]	This Work
Year	2017	2016	2021	2016	2021	2015	2016	2017	2016	
Technology (CMOS)	0.18µm	0.18µm	90nm	0.13µm	90nm	0.13µm	0.13µm SiGe BiCMOS	0.13µm SiGe BiCMOS	0.18µm	90nm
Gain(dBΩ)	59	58	41	54	42.3	50.1	72	83.7	55-69	40.6
Bandwidth (GHz)	7.9	8.1	6.5	11.5	5	7	38.4	32.1	1	3.55
Power Consumption (W)	18m	34.8m	1.67m	45m	2.7m	7.5m	261m	150m	6m	315µ
Cpd (fF)	300	300	250	-	250	250	-	-	-	220
Supply Voltage (V)	1.8	1.8	1	1.5	1	1.5	3.3	3.3	1.8	1
Input referred noise(pA/√Hz)	23	15	33.4	6.8	32.5	31.3	14.8	-	9.33	10.4
No. of passive inductors	2	2	0	2	0	0	0	0	0	0
FoM1	425	184.8	436	128	167	299	585	3276	417	1206
FoM2	5.54	3.69	3.25	-	1.3	2.4	-	-	-	25.5
Area	0.11 mm^2	-	-	0.048 mm^2	312 µm^2	16200 µm^2	-	2.345 mm^2	7500 µm^2	98 µm^2
Work*	Sim	Sim	Sim	Exp	Sim	Exp	Exp	Exp	Sim	Sim

* Sim and Exp refer to experimental and simulation results, respectively.

Moreover, Fig. 16 demonstrates the layout of the FM TIA.

As the proposed circuit contains only six transistors in the feedforward network, and a small resistance equal to 50Ω as the feedback network, the occupied chip area of the proposed TIA is only 98µm^2, which is a small area.

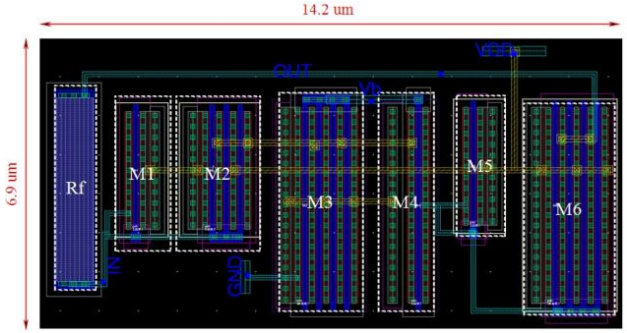


Fig. 16: The circuit layout of the proposed FM TIA.

Table 5 provides a summary of performance and compares the parameters of the proposed TIA circuit with other reported designs. The power consumption value of the proposed TIA is shown to be significantly less than other reported designs. However, in order to provide a fair comparison, two Fig.s of Merit (FOMs) are defined in Table 5, as follows:

$$FOM1 = \frac{Gain \times B.W.}{P_{DC}} \left(\frac{\Omega.GHz}{mW}\right) \quad (16)$$

$$FOM2 = \frac{Gain \times B.W. \times C_{in}}{P_{DC} \times In.Ref.Noise} \left(\frac{\Omega.GHz.pF}{mW.\left(\frac{pA}{\sqrt{Hz}}\right)}\right) \quad (17)$$

Conclusion

In this paper, a trans-impedance amplifier based on a combination of current-mirror topology and folded-cascade topology is presented, which amplifies the current signal and converts it to the voltage at the output node.

Due to the existence of a diode-connected transistor at the input node, the input resistance of the TIA is comparatively small.

Furthermore, four out of six transistors are PMOS transistors, which represent less thermal noise in comparison with NMOS transistors. Also, the proposed Folded-Mirror topology occupies a relatively small area on-chip, due to the fact that no passive element is used in the feedforward network.

Results using 90nm CMOS technology parameters show 40.6dBΩ trans-impedance gain, 3.55GHz frequency bandwidth, 664nArms input-referred noise and only 315µW power dissipation is using 1volt supply, which indicates the proper performance of the proposed circuit as a low-power building block.

Author Contributions

Authors have had an equal contribution in the problem and data analysis, interpreting the results and writing the manuscript.

Acknowledgement

The authors gratefully thank the anonymous reviewers and the editor of JECEI for their useful comments and suggestions.

Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the ethical issues including plagiarism, informed consent, misconduct, data fabrication and, or falsification, double publication and, or submission, and redundancy have been completely witnessed by the authors.

Abbreviations

TIA	Trans-impedance Amplifier
FM	Folded-Mirror
RGC	Regulated Cascode
PMOS	Positive Metal-Oxide Semiconductor
NMOS	Negative Metal Oxide Semiconductor
CMOS	Complementary metal–oxide–semiconductor
NRZ	Non-Return to Zero
PRBS	Pseudo-Random Bit Sequence
MOSFET	metal-oxide semiconductor field-effect transistor

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How to cite this paper:
S. Sadeghi, M. Nayeri, M. Dolatshahi, A. Moftakharzadeh, "Novel ultra-low-power mirrored folded-cascade transimpedance amplifie," J. Electr. Comput. Eng. Innovations, 11(1): 217-228, 2023.

DOI: 10.22061/jecei.2022.9015.568

URL: https://jecei.sru.ac.ir/article_1785.html