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Research Paper

# Application of Grey Wolf Optimization Algorithm with Aggregation Function on Designing Interleaved Boost Converter

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**Abstract**

**Background and Objectives:** The interleaved approach has a long history of use in power electronics, particularly for high-power systems. The voltage and current stress in these applications exceed the tolerance limit of a power element. The present paper introduces an improved version of an interleaved boost converter, which uses voltage mode control. The objectives of this research are improvement in the interleaved boost converter's performance in terms of the temporal parameters associated with settling duration, rising time, and overshoot.

**Methods:** An improved PI controller (proportional integral controller) is used for adjusting the proposed converter's output voltage. In the present work, the Grey Wolf Optimization algorithm with aggregation function definition (GWO_AF) is utilized to adjust the free coefficients of the PI controller. The closed-loop dynamic performance and stability can be improved by designing and implementing an optimized PI controller.

**Results:** The improvement of the freedom degree in the interleaved boost converter resulted from the existence of a few power switches in a parallel channel in the proposed circuit. An additional advantage of the interleaved boost converter, compared to the conventional one, is that it produces a lower output voltage ripple.

**Conclusion:** The usage of multi-objective optimization algorithms in designing a PI controller can significantly improve the performance parameters of an interleaved boost converter. Also, our findings indicated the excellent stability of the proposed converter when connected to the network.



## Introduction

The interleaved boost converters have a wide range of usage in industry and high-power electronics systems. The voltage and current stress in these applications exceed the tolerance limit of a power element. Utilizing numerous five sources of power in parallel or series is one approach to solve this issue. This approach will result in voltage and current split in parallelization of the power elements. Parallelization of the power converters is another method that deserves mention for addressing this issue [1], [2]. If there is a proper control for the converter and several boost converters in parallel, it can improve the performance of the interleaved boost converter. Controlling the switch on each boost converter is performed using the interleaved pulse gates [3], [4]. The switching frequency is closely related to the frequency of the gate pulses. However, the phases of the control signals can be changed. The input current is across the switches of the interleaved boost converter, all of which are connected in parallel. As a result, the converter significantly outperforms the conventional boost converter in terms of reliability and effectiveness. In the

interleaved boost converter, the freedom degree is enhanced because of the existence of a few power switches in a parallel path. This feature leads to the enhancement of numerous crucial characteristics, such as the elimination of harmonics, enhanced effectiveness, reduced conductive loss, improved power density, and line tolerance [5].

In addition, the interleaved boost converter yields a lower output voltage ripple. As a result, the output filter's size and losses can considerably decrease compared to the ordinary boost converter. The control signals in the interleaved method are separated typically based on the similarity of the switching frequencies. Thus, the waveforms resulting from input and output currents are associated with lower ripples and fewer harmonics compared to the ordinary boost converter. The elimination of the low-frequency harmonics leads to a considerable reduction in the switching and conductive losses and the electromagnetic interface surfaces in the interleaved boost converter.

A two-phase converter includes two output stages with a 180o phase difference. If the current is divided into two paths, the power of the conductive loss will decrease, resulting in an increase in the total efficiency compared to the single-phase converter. The combination of two phases in the output 35 capacitor leads to doubling the effective frequency and reducing the voltage ripple. Similarly, the pulses of the power derived from the input capacitor are alternated, causing a reduced current ripple. For achieving the specific requirement in high-power applications, it is better to use the interleaved multi-channel converter, especially in cases where there are power pieces with limited function. To give practical examples of such cases, we can mention designing the switch-mode power supplies, power modules of spaceships, automobile engineering, hybrid electrical vehicles, and satellite applications [6]-[8]. For the use of the photovoltaic solar panels' maximum power, the best solution is to utilize the interleaved boost converters. In such a case, it is necessary to consider its rapid transient response and the absence of high-frequency ripple since they might interfere with the SPV system. These converters can be highly useful for those applications in which there is a demand for a low ripple or a very high tolerance by the consumer.

So far, several studies have been conducted on the two-phase interleaved boost converters published in scientific journals. Increasing the number of phases in the interleaved boost converter makes the circuit design more complicated.

Thus, in the present work, for simplicity, the two-phase interleaved boost converter has been assumed in the continuous conduction mode (CCM) [9]. In recent years, many changes have been made to the technology of DC-DC switching converters. The switch-mode power converters require a rapid transient response to supply the new-generation modern microprocessors, electrical vehicles, DPSs, and the integration of renewable energy resources in a grid.

Therefore, in closed-loop converters, the transient performance is a major factor in designing the power supplies in practice. However, there is a pole on the right side of the panel in some of the converters, for instance, interleaved boost converters and boost converters. This pole exists in the function of control-to-output transfer for the CCM performance [10]. Thus, an initial undershoot has been observed for the step input in these converters, which exhibit a poor dynamic performance attributed to the non-minimum phase. These unwanted undershoots have a higher importance in the cases where the RHP zero approaches the origin. Such an RHP zero restricts the closed-loops bandwidth and yields a slower dynamic for the converter [11]-[17].

Many researchers have attempted for several years to improve the power performance of the converters based on improving their efficiency, decreasing the losses, and removing the noise. However, the old methods failed to provide the desired results.

This prompted the researchers to search for new techniques and modify and improve the old ones. Improving the control performance could lead to some success. Because of their simplicity, the validity of the design method, and well-known behaviors, PI controllers are widely used in industries. Nevertheless, the commonly used PI controllers cannot fully solve the non-minimum phase problem [18]. The current paper evaluates the classic 80 PI controller's performance for a boost interleaved converter. For this purpose, the controller parameter regulation method, accompanied by the GWO_AF algorithm, aims to achieve the proposed closed-loop performance by modifying the reference voltage and comparing it with the PI controller. This process led to the stability of the converter [19]-[23].

Several physical mechanisms inspire the algorithms for designing the optimized controllers, some of which include the biological molecular behavior and characteristics of the insect's swarm and photo and biological systems.

So far, no specific algorithm has been presented to obtain the optimal solution for the problems related to the optimization issue [24]. Yet, some of the algorithms may yield better solutions compared to others. As demonstrated in Fig. 1, we employed the controller feedback loop, which measures the output voltage $V_{out}$ and its comparison with the desired reference voltage $V_{ref}$.

$E^{(t)}$ error is obtained by measuring the converter output voltage and comparing $V_{out}$ with the reference

voltage responsible for error minimization control by generating the desired control signal U(t).

If there is no use of optimization algorithms for choosing optimized parameters of $K_p$ and $K_i$, overshoot, rise time error, settling time error, and steady-state error will happen to the converter output voltage. This controller mitigates the mentioned errors in a wide range of variations and differences in the input, output, and reference. In this research paper, the GWO_AF method has been employed for designing the PI controller of the two-phase boost interleaved converter [25], [26]. The GWO_AF algorithm is based on the swarm intelligence optimization methods, simply implemented [27]-[29], and has higher efficiency compared to other optimization methods of the converter controllers.

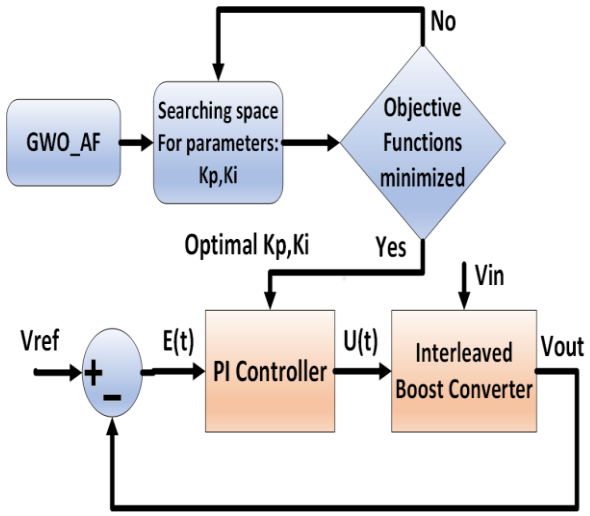


Fig. 1: Controller system process schematic.

In this study, we introduced the optimized GWO_AF-based PI controller for the boost interleaved converter. In the proposed approach, obtaining the optimized $K_p$ and Ki is followed by comparing four different objective functions, integral absolute error (IAE), integral square error (ISE), integral time square error (ITSE), and integral time absolute error (ITAE) to find the best performance of the cost functions. The simulation results have been given in this paper to demonstrate the effect of the optimized controller on the proposed controller.

The rest of the paper is organized as follows: The small-signal analysis of two-phase interleaved boost converters is described in section 2.

Section 3 is devoted to the controller system design. The evaluation method and forming of the objective functions are stated in section 4. The calculative implementation of GWO_AF is covered in section 5. Section 6 presents the simulation results and investigation. Section 7 concludes the paper and provides future trends. Finally, section 8 is for compliance with Ethical Standards.

## Description of the Two-Phase Interleaved Boost Converters

Fig. 2 shows a schematic view of the two-phase interleaved boost converter. This schematic image includes the inductor $L_1$ connected to $L_2$ in parallel, the switch $Q_1$ connected to $Q_2$ in parallel, and the diode $D_1$ connected to $D_2$ in parallel. On this basis, there are two input and output circuits in parallel. All similar pieces have been designed for better performance of the interleaved converter. The switching operation by the gate signals of the two switches is such that when one switch is in the maximum state, the other is in the minimum state with a phase difference of 180 degrees [28].

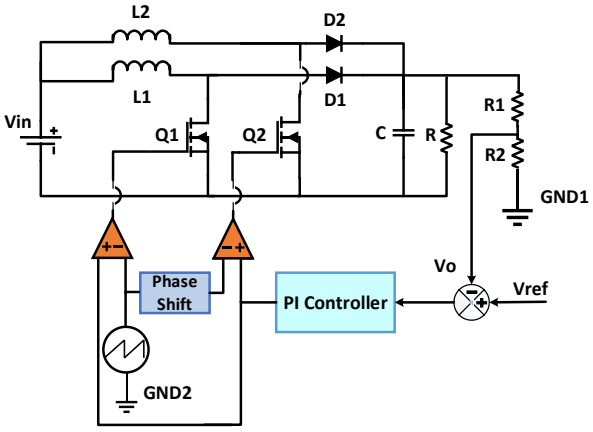


Fig. 2: Schematic diagram of the interleaved boost circuit with two-phase control.

If we assume that the inductor's current ripple is equal to 20% of the inductor's average current, we can obtain the value of the inductor from (1). $D_{max}$ is the maximum value of the duty coefficient, which is 0.75, and $V_{min}$ is the minimum value of the input voltage (48V).

$$L_{phase} = \frac{V_{in} \times D}{f_S \delta_{il}} \quad (1)$$

Considering 2% of the peak-to-peak capacitor ripple, the value of the capacitor can be obtained using (2).

$$\delta V_{out} = \frac{V_{in} \times D}{T_S C_{out} R} \quad (2)$$

## Operation Modes

The state space averaging technique is used for analyzing the interleaved boost converter. By applying this mathematical model, the converter's switching function is defined in four switching methods. The state equations obtained for the converter's operation mode of Fig. 3 are as follows [28].

In Mode 1, Switches $Q_1$ and $Q_2$ are in the on mode, but diodes $D_1$ and $D_2$ are in the Off mode. Fig. 5 shows the

equivalent circuit for this mode. The following formulas define the function of Mode 1, in which the current of Inductor $i_{Li}$ is assumed as the state variable, and the voltage of Capacitor V0 is assumed as the third mode variable.

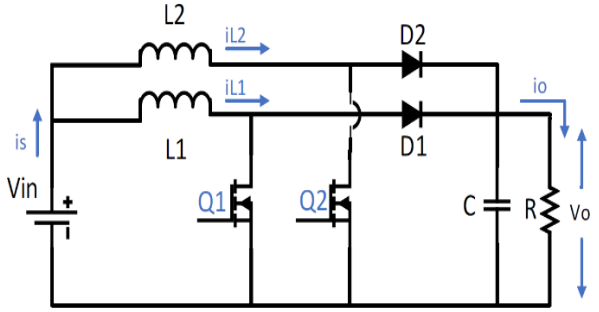


Fig. 3: Schematic diagram of the interleaved boost circuit.

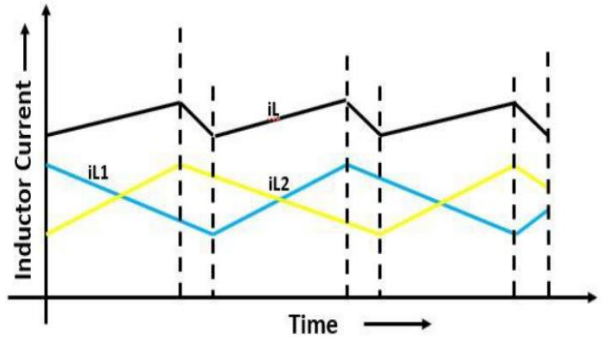


Fig. 4: Ideal waveform for the interleaved boost converter.

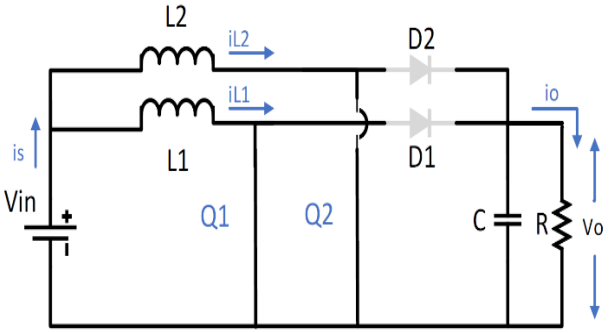


Fig. 5: Equivalent circuit for Mode 1.

$$\frac{di_{L1}}{dt}=\frac{V_s}{L_1} \tag{3}$$

$$\frac{d_{vo}}{dt}=\frac{V_O}{RC} \tag{4}$$

$$\frac{di_{L2}}{dt}=\frac{V_s}{L_2} \tag{5}$$

$$A=\begin{bmatrix}0 & 0 & 0\\ 0 & 0 & 0\\ 0 & 0 & \frac{-1}{RC}\end{bmatrix} B_1=\begin{bmatrix}\frac{1}{L_1}\\ \frac{1}{L_1}\\ V_O\end{bmatrix} \tag{6}$$

In Mode 2, Switches $Q_1$ and $Q_2$ are in the On and Off modes, respectively. Also, Diodes $D_1$ and $D_2$ are in the Off and on modes, respectively. Mode 2 is shown in Fig. 6.

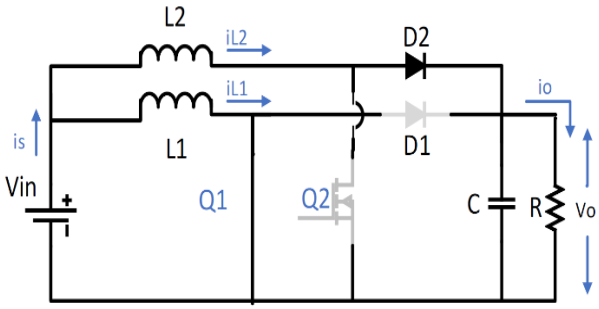


Fig. 6: Equivalent circuit for Mode 2.

$$\frac{di_{L1}}{dt}=\frac{V_s}{L_1} \tag{7}$$

$$\frac{di_{L2}}{dt}=\frac{V_s}{L_2}-\frac{V_0}{L_2} \tag{8}$$

$$\frac{d_{vo}}{dt}=\frac{i}{L_2}-\frac{V_0}{RC} \tag{9}$$

$$A=\begin{bmatrix}0 & 0 & \frac{1}{L_1}\\ 0 & 0 & 0\\ 0 & \frac{1}{C} & \frac{-1}{RC}\end{bmatrix} B_1=\begin{bmatrix}\frac{1}{L_1}\\ \frac{1}{L_1}\\ 0\end{bmatrix} \tag{10}$$

In Mode 3, Switch $Q_1$ is in the off mode, but Switch $Q_2$ is in the on mode. Also, Diodes $D_1$ and $D_2$ are in the on and off modes, respectively. Fig. 7 shows the performance of the interleaved boost converter in Mode 3.

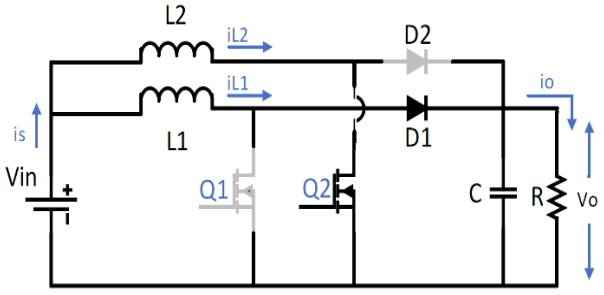


Fig. 7: Equivalent circuit for Mode 3.

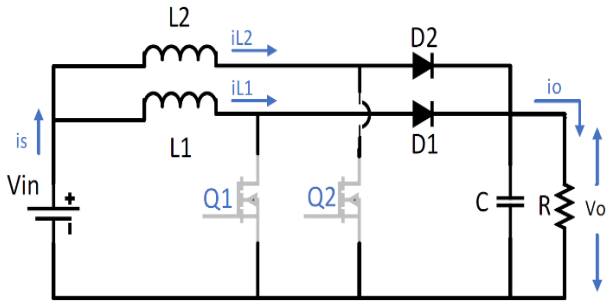


Fig. 8: Equivalent circuit for Mode 4.

$$\frac{di_{L1}}{dt} = \frac{V_S}{L_1} - \frac{V_O}{L_1} \tag{11}$$

$$\frac{di_{L2}}{dt} = \frac{V_S}{L_2} \tag{12}$$

$$\frac{dv_O}{dt} = \frac{i_{L1}}{C} - \frac{V_O}{RC} \tag{13}$$

$$A_3 = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & 0 \\ \frac{1}{C} & 0 & \frac{-1}{RC} \end{bmatrix} B_3 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} \tag{14}$$

In Mode 4, Switches $Q_1$ and $Q_2$ are in the Off mode, but Diodes $D_1$ and $D_2$ are in the on mode. Fig. 8 displays the equivalent circuit for this mode.

$$\frac{di_{L1}}{dt} = \frac{V_S}{L_1} - \frac{V_O}{L_1} \tag{15}$$

$$\frac{di_{L2}}{dt} = \frac{V_S}{L_2} - \frac{V_O}{L_2} \tag{16}$$

$$\frac{dv_O}{dt} = \frac{i_{L1}}{C} + \frac{i_{L2}}{C} - \frac{V_O}{RC} \tag{17}$$

$$A = \begin{bmatrix} 0 & 0 & \frac{1}{L_1} \\ 0 & 0 & \frac{1}{L_2} \\ 0 & \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} B_4 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} \tag{18}$$

The state equations and matrix coefficients for the interleaved boost converter are as follows:

$$X = AX + BU \tag{19}$$

$$Y = CX + DU \tag{20}$$

$$[A] = A_1 d_1 + A_2 d_2 + A_3 d_3 + A_4 d_4 \tag{21}$$

$$[B] = B_1 d_1 + B_2 d_2 + B_3 d_3 + B_4 d_4 \tag{22}$$

$$D = d_1 + d_2 + d_3 + d_4 \tag{23}$$

Using the SSA method, the interleaved boost converter's output control transfer function in its final form is obtained as follows. do is the duty coefficient, and N is the number of phases in the interleaved converter. It is evident that there is an RHP zero in the interleaved boost converter's transfer function [30]. By substituting the converter's parameters from Table 1, the interleaved boost converter's transfer function is found, which is as follows: The transfer function of the interleaved boost converter is as follows:

$$\frac{V_{O(S)}}{V_{in(S)}} = \frac{1 + sRC}{(1-D)\left[1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2}\right]} \tag{24}$$

$$\frac{V_{in(S)}}{d_{(S)}} = \frac{1 + sRC}{(1-D)\left[1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2}\right]} \tag{25}$$

$$T_{P-IBC(S)} = \frac{V_{O(S)}}{d_{(S)}} = \frac{2NV_{in}}{\left(r + 2Nd^2R_L\right)C} * \frac{-s + (2Nd^2R_L - r)/L_C}{(s + \frac{r}{L_C})(s + \frac{1}{R_L C}) + \frac{2Nd^2}{L_C C}} \tag{26}$$

$$T_{P-IBC(S)} = \frac{V_{O(S)}}{d_{(S)}} = \frac{-1.666^5 s + 7.675^9}{s^2 + 328.5s + 1.441^7} \tag{27}$$

Table 1: The interleaved boost converter design values

| No. | Description | Design parameter value |
|---|---|---|
| 1 | Input voltage | 48 V |
| 2 | Output voltage | 240 V |
| 3 | Output power | 54.8 W |
| 4 | Load current | 0.23 A |
| 5 | Switching frequency | 20 KHz |
| 6 | $L_1$ and $L_2$ inductance | 1 mH |
| 7 | Capacity | 1 µF |
| 8 | Load resistance | 3200 Ω |

## Designing the Controller

For achieving the desired closed-loop performance of the converter necessitates the controller's presence. Besides, the controller can facilitate the circuit transfer function's formation for obtaining the system's general stability and the rapid transient response. There are several kinds of analog compensators, namely the RC network and amplifier.

The forward controller, which is also known as the (PD) controller, is commonly used for the phase margin enhancement in a bipolar system (two-pole system). This type of controller exhibits sensitivity to the noise resulting from the derivative function in it. The use of reverse PI controller (proportional-integral controller) causes increase in the low-frequency gain in loops, leading to stronger output at DC and the frequencies that are lower than the frequency of loop crossover [31], [32].

There are various types of classic controllers, namely forward-backward, PI, PID, etc. These controllers have been developed aiming to make sure of the converters' desirable performance under special conditions. However, for the CCM performance in the interleaved boost controller, there exists an RHP zero in the output control transfer function.

Thus, the non-minimal phase problem results in the poor dynamic effectiveness of the interleaved boost converter. Because of the RHP zero, the closed-loop system's bandwidth is restricted and the converter's dynamics is decreased. Hence, exhibiting a good response to the uncertainty of parameters, line, and instant load changes would be very difficult for the ordinary PID controller. According to the reports, the optimal PI controllers, which are based on the metaheuristic algorithms, can enhance the DC-DC converters' dynamic performance [33], [34].

## Designing the GWO_AF-Based Optimal PI Controller

It sould be mentioned that many of other hyper heuristic algorithms can be employed for designing PI cotroller. In this paper GWO algorithm has been chosen due to its good performance in this research area [36]-[41].

As can be seen in Fig. 9, the converter's output voltage is compared to the reference voltage, and the generated error signal passes through the optimal classic controller, the coefficients of which are obtained by using the GWO_AF algorithm. Subsequently, to generate the pulse width modulation (PWM) signal, the created control signal is compared to the high-frequency triangle waveform [32].

This PWM signal, after passing the Astable multi-vibrator and optoisolator, produces the signal of the MOSFET switches $Q_1$ and $Q_2$.

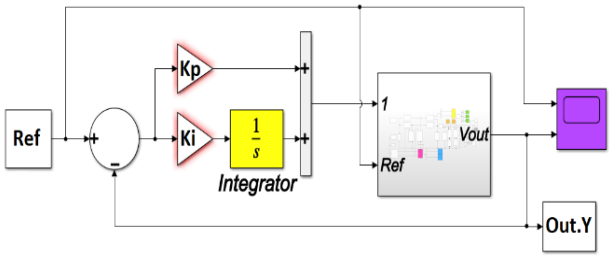


Fig. 9: Circuit of PI controller.

The optimal parameters of the PI controller are obtained using the GWO_AF algorithm considering the best performance of the fitness function to optimize the overshoot ($M_p$), the rise time ($T_r$), and the settling time (Ts).

Fig. 10 shows the diagram of adjusting the coefficients of the PI controller by the GWO_AF algorithm.

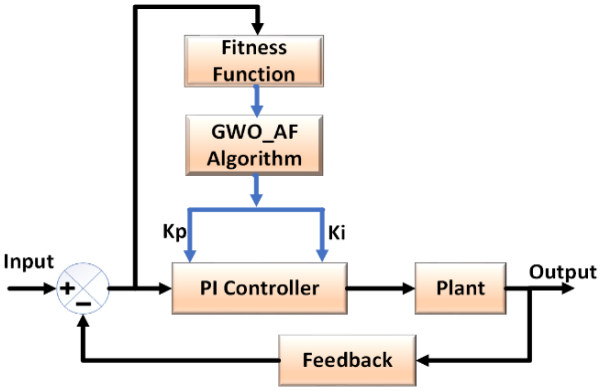


Fig. 10: Flowchart of the circuit of the optimal PI controller.

## Fitness Function Definition

The proportion function containing normal effectiveness is the initial step in the process of designing the optimal controller relying on metaheuristic algorithms with favored characteristics and restrictions under the step input signal to reach optimal effectiveness. Some of the major time-related features include overshoot ($M_p$), rise time ($T_r$), settling time ($T_s$), and permanent state error. The minimum value of the proportion function is related to time, and values of the parameters are optimal. Selecting the proportion function is the most important step in applying the algorithm. In general, there are four types of performance: integral absolute error, integral squared error, weighted squared error integral, and weighted absolute error integral at the ITAE performance time. As shown by Jagatheesan and Anand, to confirm the optimal selection of a fitness function for the multi-objective grey wolf optimization algorithm, the ITAE yields the fastest response with minimum overshoot for the methods of optimization, which is the best choice for the optimization of a proportional integral controller [23]. Ansari et al. came to conclusion that utilizing the ITAE as

the fitness function for finding the best gins for traditional PI is in fact to select the multi-objective optimizer. In the study conducted by Kishnani et al., another optimization technique, which is known as the (election-survey optimization), was used. In this technique, the ISE is chosen to obtain the PI gains [33]. Though the gain resulting from merging the errors has been utilized as the assessor of performance, a weighted ISE and an overshoot was considered by Kumar et al., leading to the results in which the overshoot values were above the permitted level. In this paper, the ISE, IAE, and ITSE were applied for confirming the better case. This problem can be mathematically represented as follows [33], [34]:

$$ISE = \int_0^\infty \delta^2(t)dt \tag{28}$$

$$IAE = \int_0^\infty \left|\delta(t)\right| dt \tag{29}$$

$$ITSE = \int_0^\infty t\delta^2(t)dt \tag{30}$$

$$ITAE = \int_0^\infty t\left|\delta(t)\right| dt \tag{31}$$

where τ indicates the upper bound, which is chosen as the steady-state value and δ represents the error of reference to the output. Though the assessment of the old methods is an integrated technique, a novel technique has been suggested recently, in which both the settling time and the overshoot are considered. Therefore, these values must be combined appropriately in the fitness function. This function is defined as follows [33]:

$$Cop = T_s\left(1 + \alpha M_p^2\right) + \beta T_r \tag{32}$$

where MP indicates the overshoot, α represents the adjustable weight for the squared overshoot, and $T_S$ and Tr indicate the settling time and rise time Respectively [21]. To obtain a suitable selection for this weight, the desired percentage must be considered for the overshoot (M%) in which the square root should be unique:

$$\alpha = \left(\frac{1}{M_{\%}}\right)^2 \tag{33}$$

The fitness function, unlike the cost function, is commonly maximized. For this purpose, the following equation is utilized:

$$fit = 1/\mathrm{Cos}\,t \tag{34}$$

## Computational Implementation of GWO_AF

Proposed by Mirjalili & Lewis in 2014, the GWO algorithm has been inspired by the grey wolves' leadership and group hunting technique. When designing the GWO algorithm, to transform the hierarchy of the grey wolves into a mathematical model, the readiest solution is considered as the Wolf α. Subsequently, the second and third solution, respectively, are indicated by β and δ. The rest of the suggested solutions are considered as the Wolves ω. The optimization in the GWO algorithm is led by α, β, and δ. Then, these three wolves are followed by the Wolves ω towards the global optimization. In addition to the social leadership, the following equations are used to prompt the surrounding behavior of the grey wolves during the optimization [26].

$$D = \left|C.X_P(t) - X(t)\right| \tag{35}$$

$$X(t+1) = X_P(t) - A.D \tag{36}$$

where t represents the current iteration, C and A are vector coefficients, $X_P$ is the position of the hunting vector, and X indicates the position of the grey wolf's vector. Vectors A and C are calculated as follows:

$$A = 2a.r_1 - 1 \tag{37}$$

$$C = 2.r_2 \tag{38}$$

In this formula, during the periods, the iteration of Component a is linearly reduced from 2 to 0 and $r_1$ and $r_2$, which are random vectors within the range of [0, 1] in the GWO algorithm in Fig. 11, find the optimal solutions to the optimization problems by exciting of social leadership and surrounding mechanisms. This algorithm keeps the first three good solutions and forces the other Factors to update their positions, to stimulate, search, and identify the dedicated areas of the search space; the continual optimization process employs the accompanying formulas for any search factor:

$$D_\alpha = \left|C_1.X_a - X\right| \tag{39}$$

$$D_\beta = \left|C_2.X_\beta - X\right| \tag{40}$$

$$D_\delta = \left|C_3.X_\delta - X\right| \tag{41}$$

$$X_1 = X_a - A_1.D_\alpha \tag{42}$$

$$X_2 = X_\beta - A_2.D_\beta \tag{43}$$

$$X_3 = X_\delta - A_3.D_\delta \tag{44}$$

$$X(t+1) = \frac{X_1 - X_2 - X_3}{3} \tag{45}$$

The search by A, the random value of which is above 1 or below −1, has been guaranteed; so that, the search factor is force to deviate from the prey. Another part of the grey wolf optimization algorithm is C, which facilitates the search process. Vector C created a value between 0 and 2 so that [0, 2] is indicative of the prey's random weight for the non-emphasis (C < 1) or statistical emphasis (C > 1) on the prey's impact on the definition of distance. With the help of this, the GWO algorithm will exhibit further random values in the optimization process, resulting in a search that is better than the limited optimum. Here, it is notable that C is not reduced linearly in comparison with A.

To ensure that the search is prioritized not only during the preliminary repetitions but also during the ultimate iterations, it is necessary to use parameter C when generating the random value in every scenario. Particularly in the last iterations, this component is quite useful for the ideal recording.

In the case that |A| < 1, processing with the grey wolf optimization algorithm will start. Whenever Vector A' s random value falls within the [−1, 1] range, the search factor's next position will be somewhere between its current position and the position of the prey. This will facilitate the convergence of the search factor to the estimated position of the prey, which has been given by the problem' alpha, beta, and delta.

The first step in the GWO algorithm is optimizing the random generation of solutions that are part of the preliminary population. Alpha, Beta, and Gamma are the three remaining good solutions that have been maintained as a part of the optimization process. For each Wolf ω (the searcher factor), the position of updating the equations [39] to [45] has been excited; while, Parameters A and a decrease linearly during a period. Therefore, when |A| > 1, the search factors incline toward divergence from hunting but when |A| < 1, they tend toward convergence.

The location and score of Solution Alpha are ultimately returned as the optimum solution found throughout the optimization process after the ultimate criterion is attained. To execute the optimization process of multiple objectives, we combined two new components with it. The MOPSO-like components are those that have been utilized for this particular objective. The initial part of the system is an archive that oversees keeping the optimal solutions that do not include ray domination. The leader's approach, which aids the alpha, beta, and delta in choosing the best option from the archive, makes up the second element [35]. The archive is, in fact, straightforward storage that allows for the safe archiving and retrieval of optimal solutions independent of ray domination. As the best instance of the archives, the controller archive can be mentioned, which can control the archive when a solution is entered or when the archive runs out of capacity. Notice that an archive has several sections. During iteration, the obtained non-dominated solutions are compared with sections of the archive. This might lead to four different cases:

* In the case that the new member has been controlled by at least one of the archive sections, the solution should not be imported into the archive.

* The newly developed solution can regulate any number of previously implemented solutions. In these cases, the controlled solutions in the archive should be eliminated in order that the new solution can be imported into the archive.

* If neither the new solution nor the old one controls the other one, then it is better to add a new solution to the archive.

* If the archive has run out of capacity, the mechanism network should resort the components of the search space, find the most populated piece, and delete its solutions. Subsequently, to advance the ultimate optimal Estimated Pareto front, the novel solution must be imported into the least-populated component.

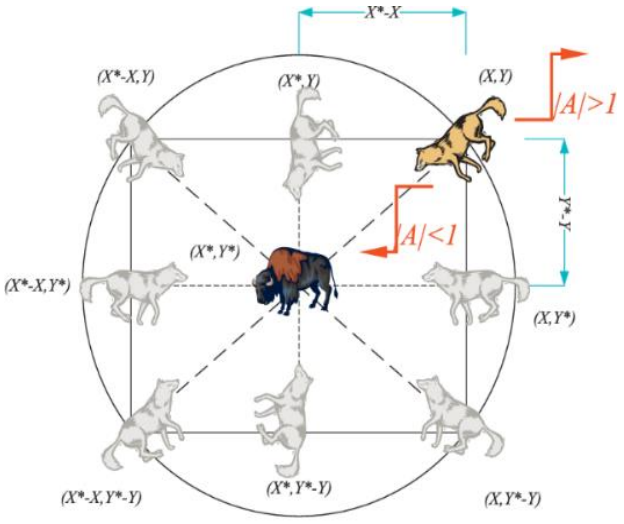


Fig. 11: The search agents' position-updating process and how A affects it [26].

## Results and Discussion

The extensive simulation performed in this work aimed to find the interleaved boost converter's dynamic performance. This was done with an optimal proportional-integral controller under SIMULNIK environment in MATLAB. Considering the step input and frequency response speed of the interleaved boost converter with classic controllers, the dynamic performance implies the better dynamic response of the studied converter with GWO_AF-based PI controller in

comparison with the ordinary boost converter.

Table 2: PI parameters

| PI parameters | Value |
|---|---|
| $K_p$ | $3^{-3}$ |
| $K_i$ | 4 |

The step input response to the interleaved boost converter with optimized PI controller has the fastest response with less overshoot error. It should be noted that the optimization approach is indeed a standard method for designing classic PI controllers; besides, it also exhibits a good performance regarding the close loop of the interleaved boost converter.

The PI controller's parameters, which have been designed using GWO_AF metaheuristic algorithm, are presented in Table 2.

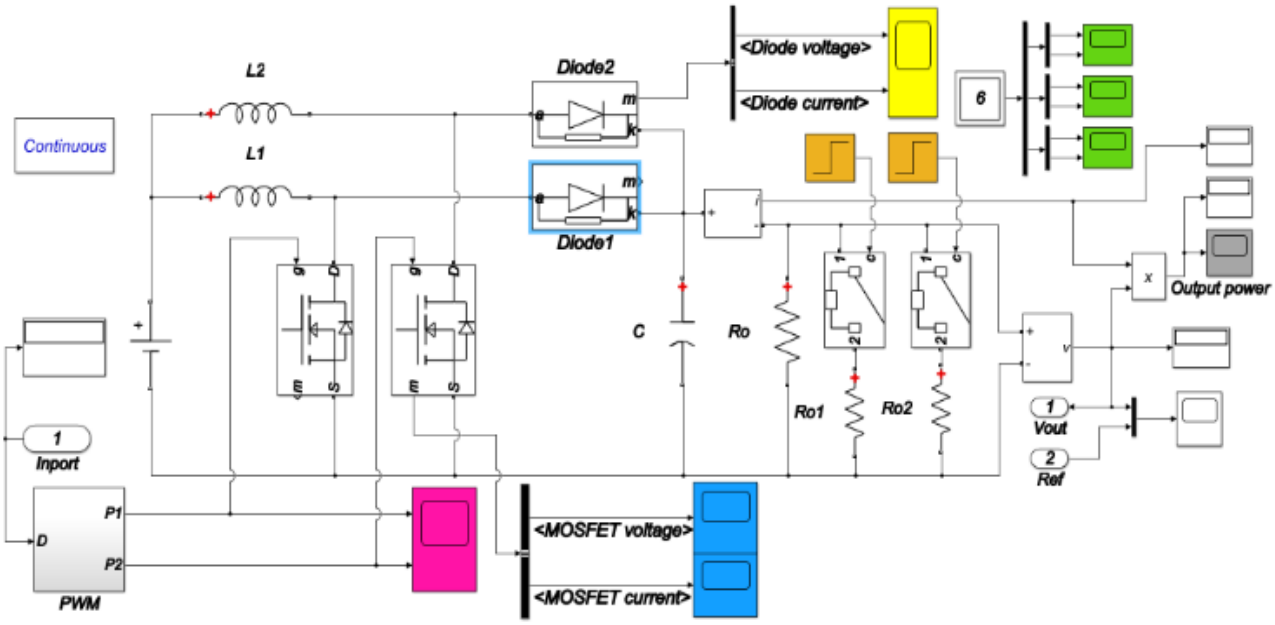


Fig. 12: Schematic of the interleaved boost converter with the proposed controller.

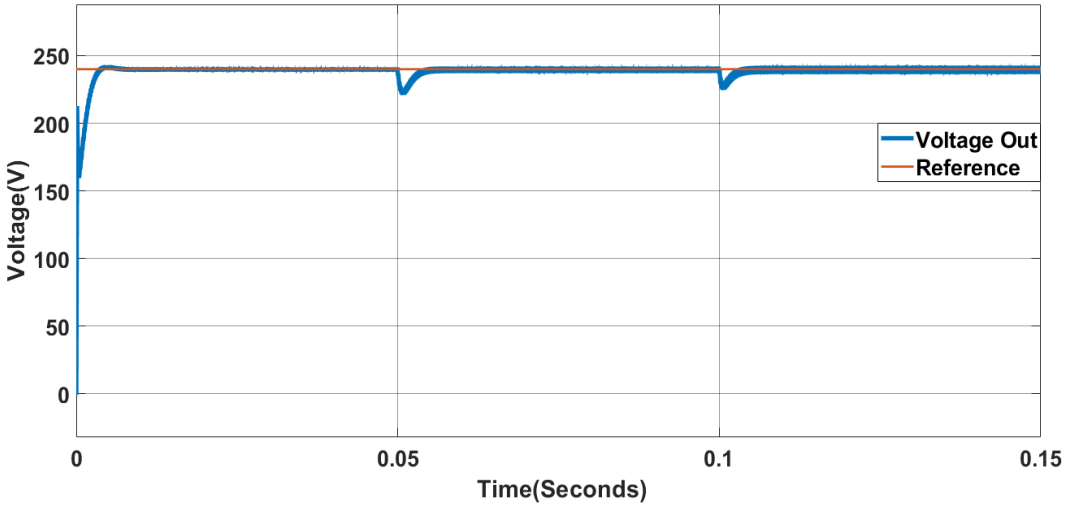


Fig. 13: The waveform of the optimized converter's output voltage.

Fig. 13 shows the optimal output voltage of the converter. After applying a momentary load at times of 0.05 and 0.1 to the converter, the output voltage generally achieves stability compared to the reference voltage 240 by the PI_GWO_AF controller.

Fig. 22 displays the voltage stability and performance against the sudden changes in the load connection to the network when the output voltage increases to 240V for the steady state.

The best closed-loop dynamics (settling time, rise time, and overshoot) exhibited by the GWO_AF-based PI controller with interleaved boost converter were lower than that of the classic PI controller with a boost converter.

In comparison with the boost converter with the optimal controller, the best tracking performance was exhibited by the interleaved boost converter with a PI controller based on the GWO_AF algorithm.

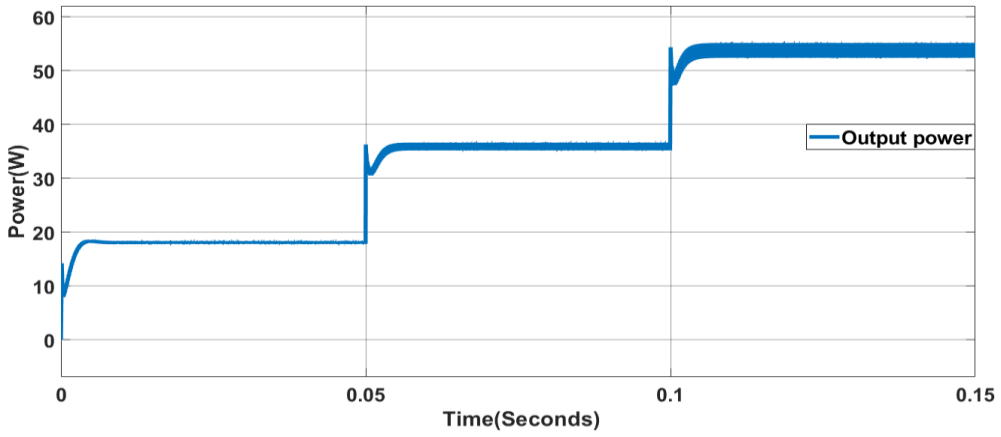


Fig. 14: The waveform of the optimized converter's output power.

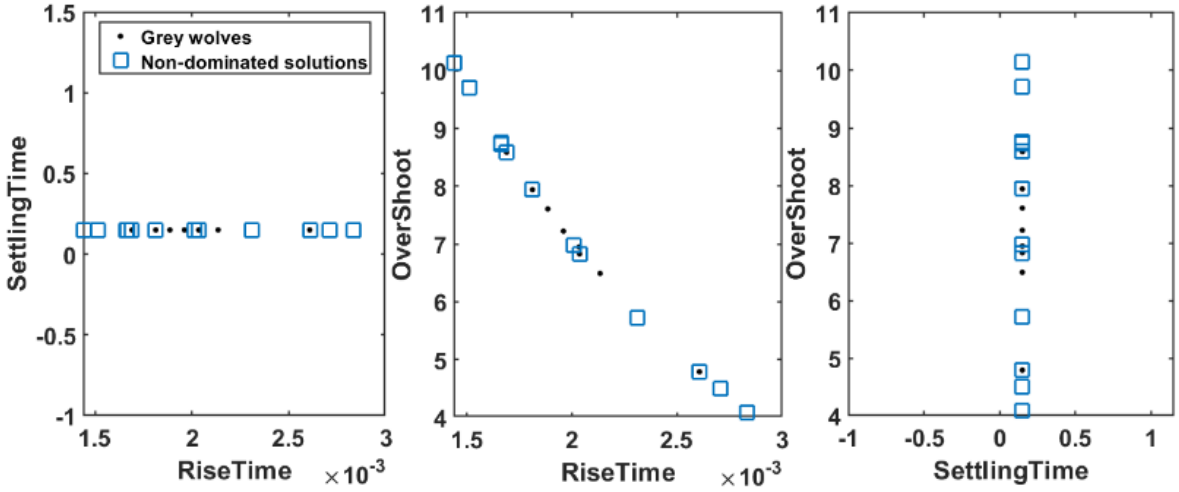


Fig. 15: Estimated Pareto front of the optimized parameters' performance relative to each other.

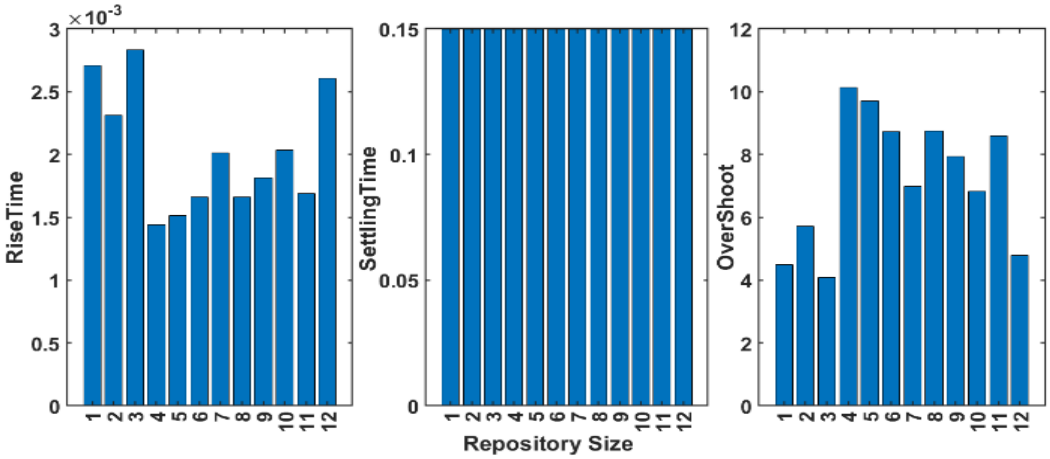


Fig. 16: The bar graph of the optimized parameters' performance in the circuit relative to each other.

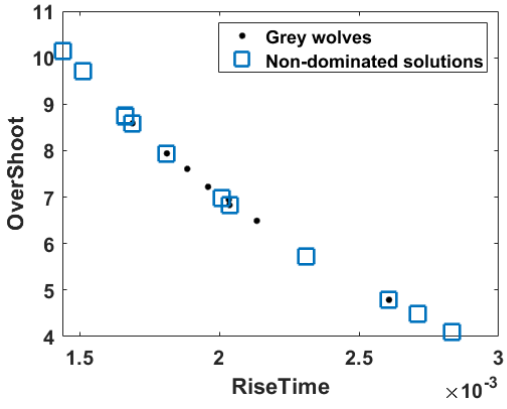


Fig. 17: Estimated Pareto front, Overshoot performance and Rise Time towards each other.

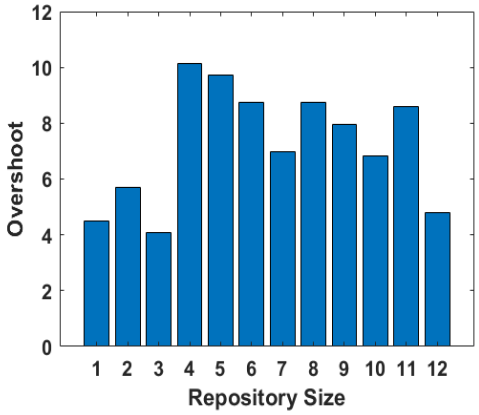


Fig. 19: The optimization performance of the "Overshoot" parameter by the controller.

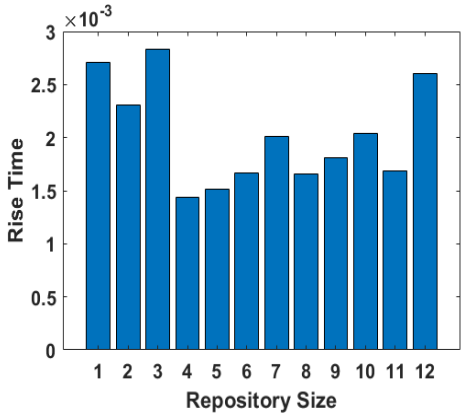


Fig. 18 : The optimization performance of the "Rise Time" parameter by the controller.

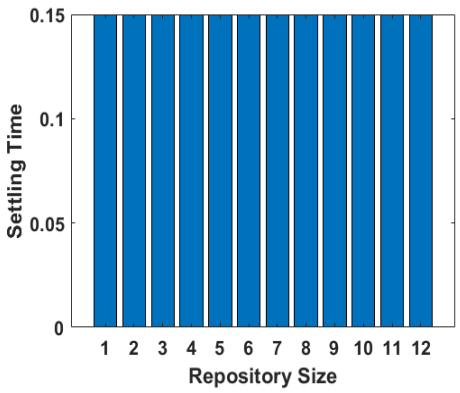


Fig. 20: The optimization performance of the "Settling time" parameter by the controller.

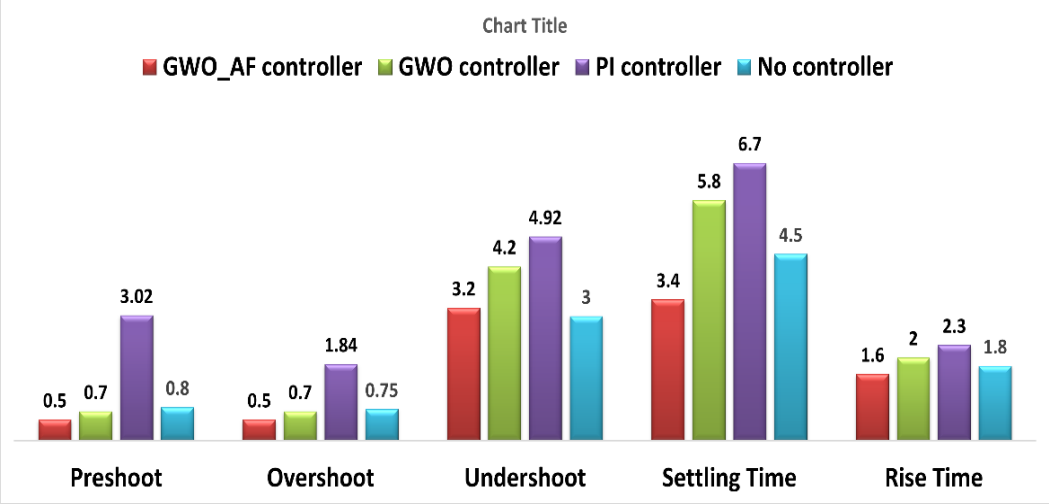


Fig. 21: Comparison of the effect of controller performance on optimized parameter.

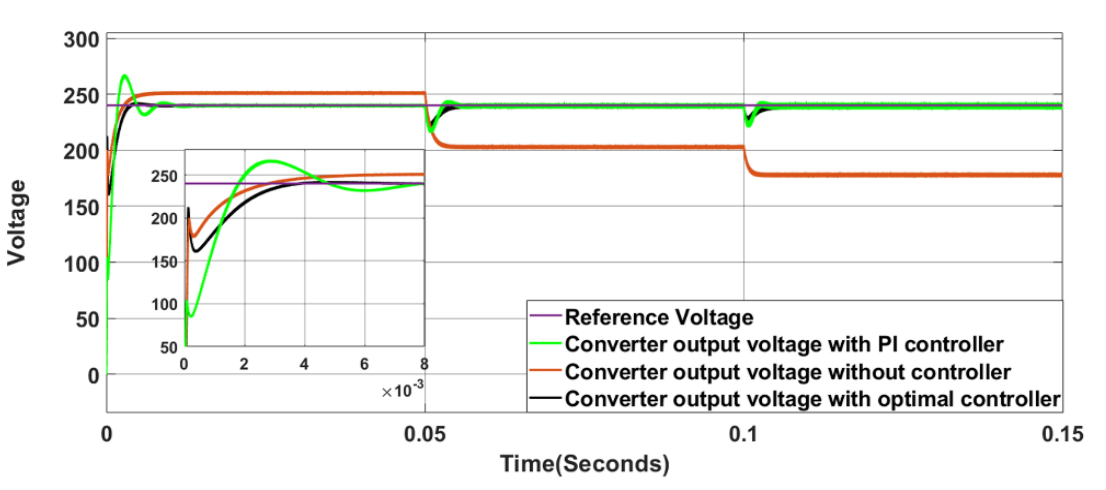


Fig. 22: The Effect of controller performance on the output voltage of converter.

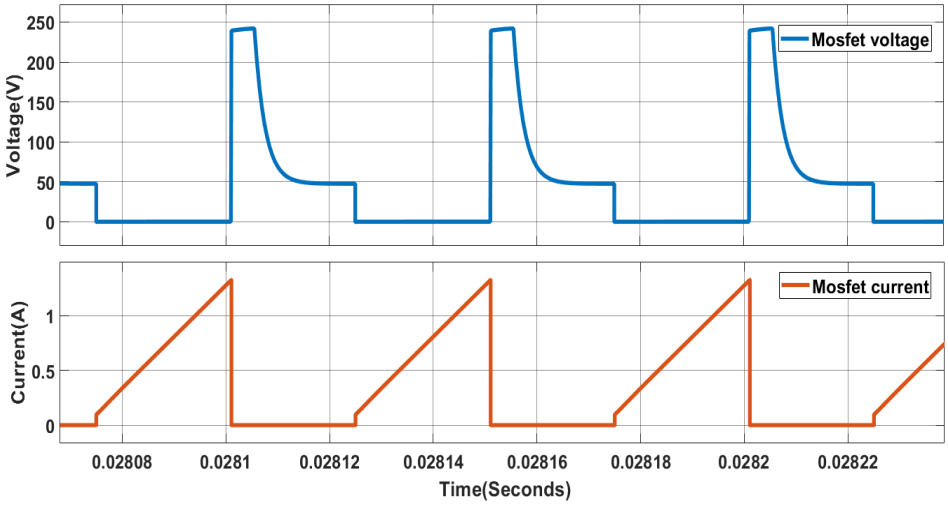


Fig. 23: Current waveform and MOSFET output voltage.

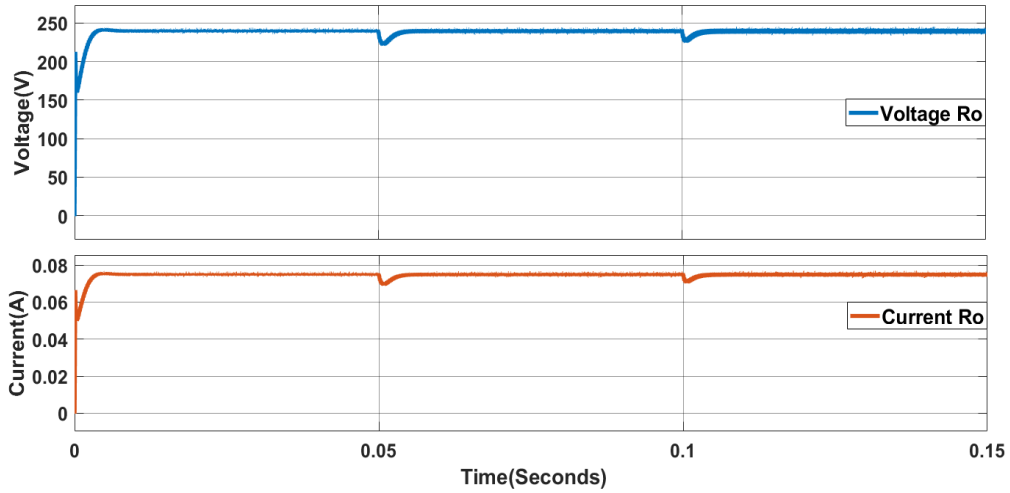


Fig. 24: Current waveform and output resistance voltage.

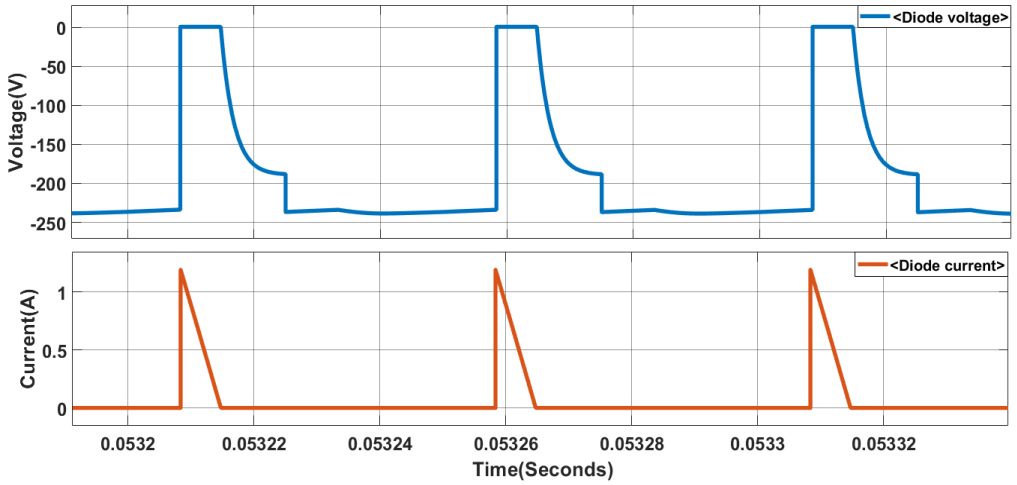


Fig. 25: Current waveform and Diode output voltage.

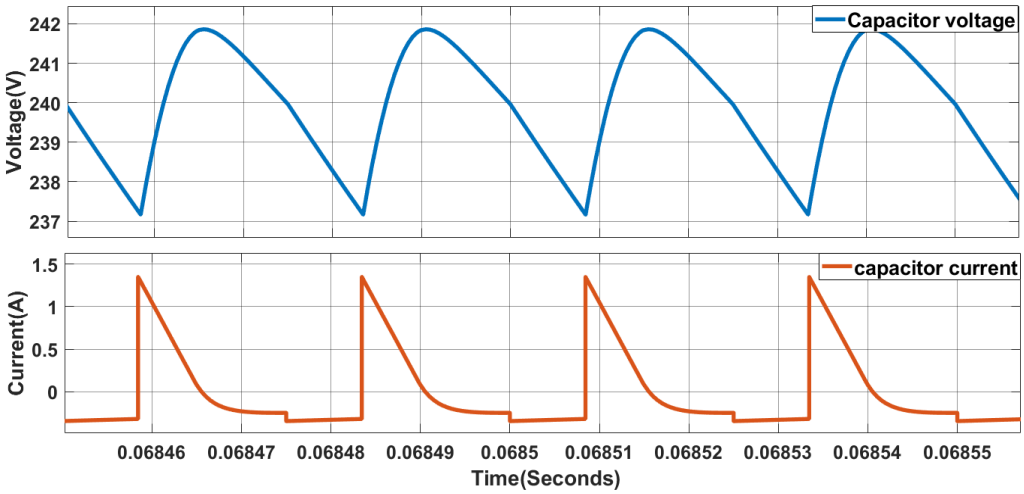


Fig. 26: Output capacitor current waveform.

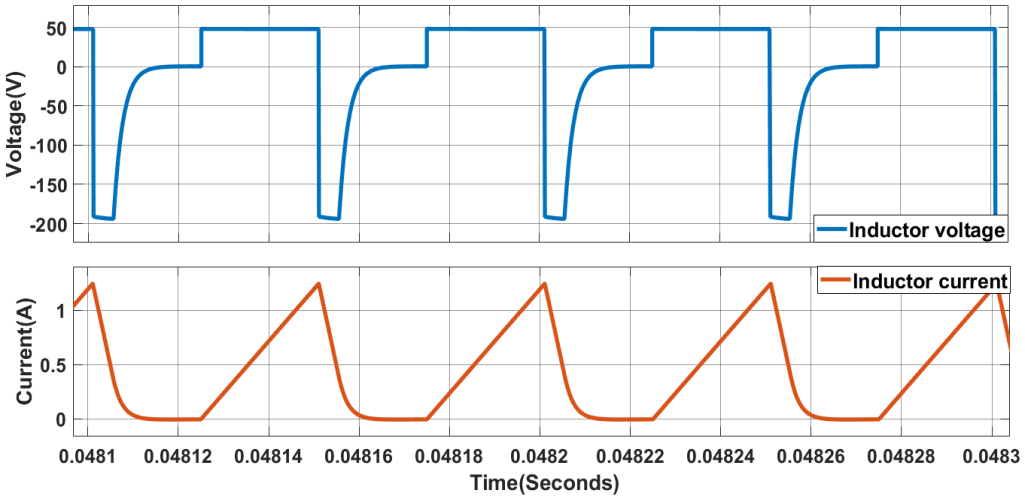


Fig. 27: Current waveform and inductor output voltage.

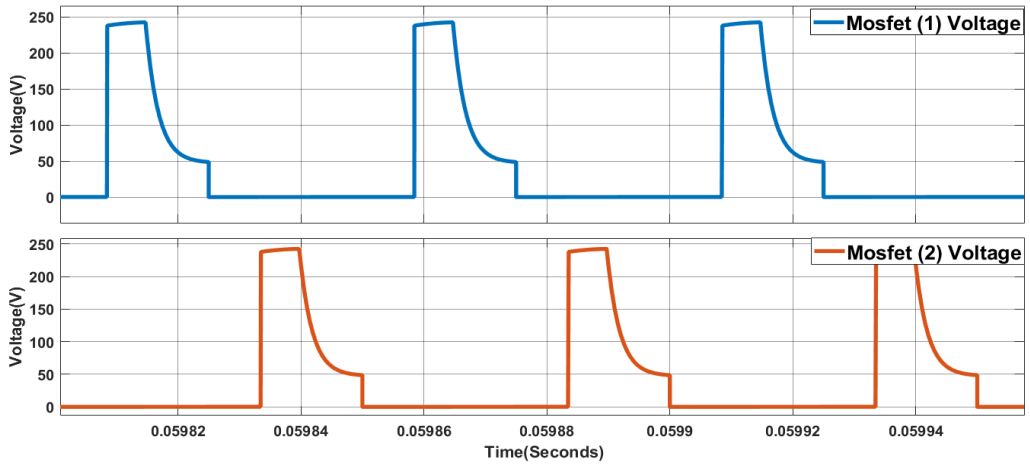


Fig. 28: MOSFET output voltage waveform.

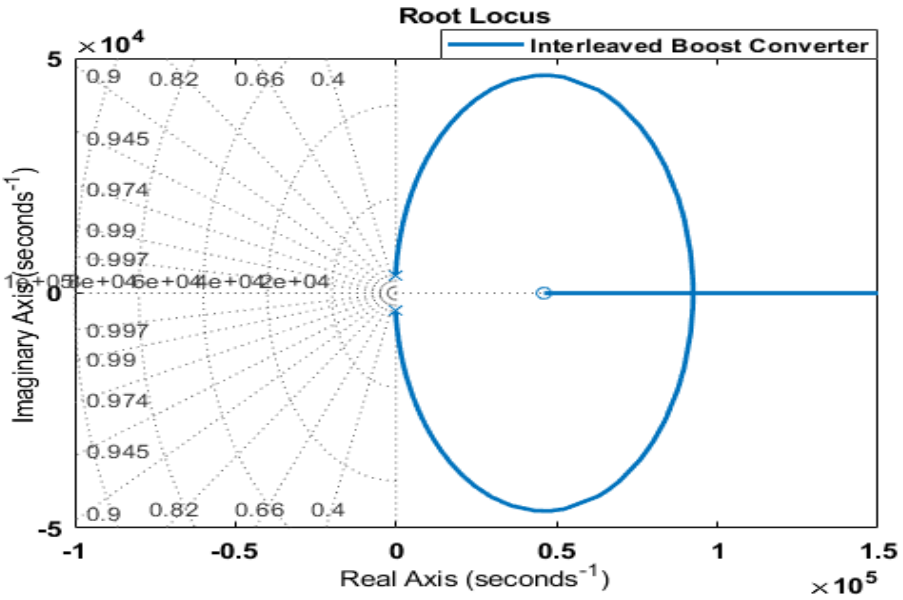


Fig. 29: The pole and zero of the interleaved boost converter.

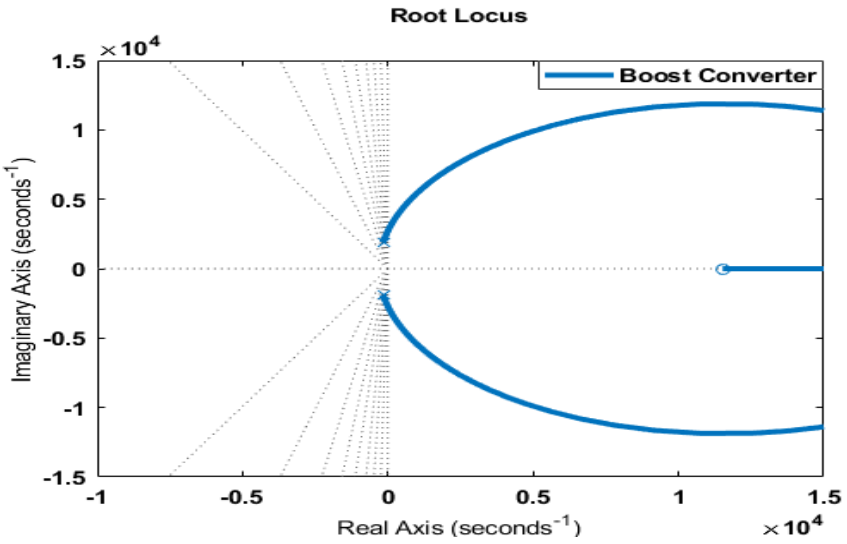


Fig. 30: The pole and zero of the boost converter.

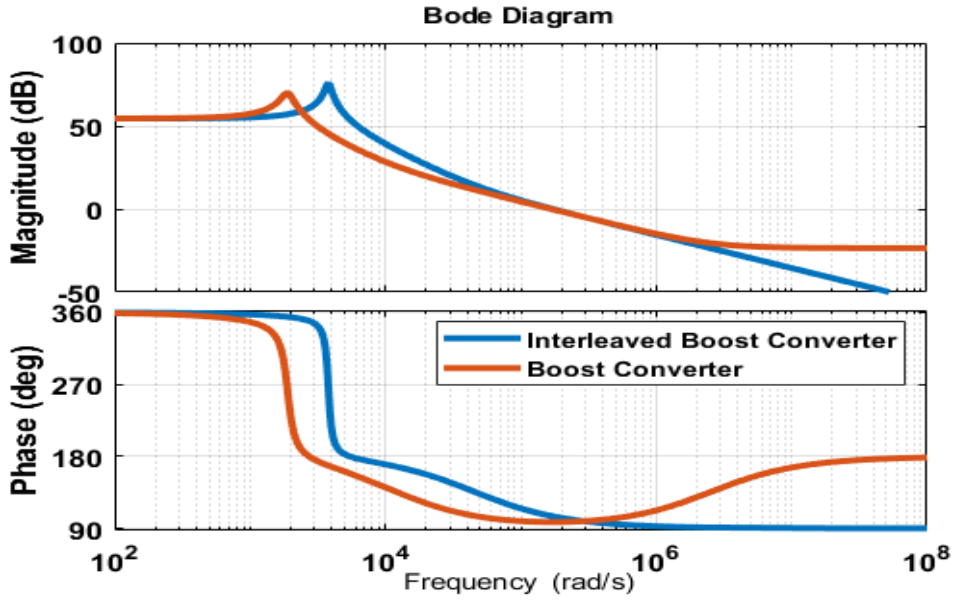


Fig. 31: The bode diagram of the interleaved boost converter.

In the optimal controller based interleaved boost controller, the load voltage followed the reference voltage (Ref), was set rapidly, and preserved the zero steady-state error. Therefore, the simulation results are indicative of the satisfactory tracking performance of the "interleaved boost converter" with optimal controller and its good load adjustment in the closed-loop mode. The simulated response of the input current, the pulse gate for S1, the currents of the Inductors $i_{L1}$ and $i_{L2}$, and the pulse gate for S2 along the steady state are shown in Fig. 27. As can be inferred from Fig. 28, the inductor's two currents and the two pulse gates are located at a 180◦ angle relative to each other. In comparison with the current of the single inductor, the input current, which results from the inductor's two currents, is made of a smaller ripple. Fig. 29 shows the location of the zero and pole of the interleaved boost converter based on (27). As can be seen, the stability of the proposed converter controller is superior to that of the boost converter (shown in Fig. 30).

## Conclusion

This study is aimed at designing and executing a two-phase interleaved boost converter based on an optimal PI controller. This converter is going to be designed and executed for decomposable applications. For this purpose, the controller was initially designed using the classic technique.

Subsequently, the controller's parameters were adjusted by means of the GWO_AF-based optimization method aiming to obtain better performance and stability. Then, simulations were performed to investigate

the interleaved boost converter in terms of comparative analysis and closed-loop performance. Regardless of the operating cycle, the obtained results indicated the lower ripple content of the studied converter in the inductor, input current, and output voltage I comparison with the boost converter.

According to the results, it could be concluded that the proposed converter has exhibited the highest system bandwidth, the best closed-loop performance, and the largest stability margin compared to the converter's open-loop mode. Accordingly, it was decided to utilize the GWO_AF-based PI controller for designing and executing the SMPS by the interleaved boost converter in order that the overall stability and closed-loop performance can be improved. The proposed optimal controller can be utilized for different applications with high degree power converters, including hybrid electrical vehicles and MES, which has not been reported before and has been introduced in this paper for the first time. It can be also executed for the extraction of the maximum power and other objectives. Notably, the proposed converter with very fast transient response and without high-frequency ripples can be also executed for the extraction of the maximum power from the SPV panel.

## Author Contributions

S.M Naji Esfahani simulated the converter and controller in MATLAB.

S. H. Zahiri and M. Delshad have supervised the performance optimization and converter controller design. All authors discussed the results and contributed to the final manuscript.

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## Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the ethical issues including plagiarism, informed consent, misconduct, data fabrication and, or falsification, double publication and, or submission, and redundancy have been completely witnessed by the authors.

## Abbreviations

| | |
|---|---|
| *PI* | Proportional Integral |
| *CCM* | Continuous Conduction Mode |
| *GWO_AF* | Grey Wolf Optimization with Aggregation Function |
| *PWM* | Pulse Width Modulation |

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