Journal of Electrical and Computer Engineering Innovations
(JECEI)
Journal homepage: http://www.jecei.sru.ac.ir

Research paper

A Merged LNA-Mixer with Wide Variable Conversion Gain and Low Noise Figure for WLAN Direct-Conversion Receivers

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Article Info

Article History:
Received 08 June 2023
Reviewed 07 August 2023
Revised 29 September 2023
Accepted 08 October 2023

Keywords:
Variable conversion gain
Low noise transconductance amplifier (LNTA)
Active mixer
Noise figure

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Abstract

Background and Objectives: In wireless communications, receivers play an essential role. Among receiver architectures, the direct-conversion receiver (DCR) architecture has been selected due to its high level of integration and low cost. However, it suffers from DC offset due to self-mixing, I/Q imbalance, and flicker noise.

Methods: This paper presents a new LNA-mixer with variable conversion gain (VG-LM) for wireless local area network (WLAN) applications. A low noise transconductance amplifier (LNTA) is used as the transconductance stage in the Gilbert cell mixer. The wide variable conversion gain range is achieved by the change in LNTA's transconductance and transconductance of the mixer switching transistors.

Results: The proposed LNA-mixer is designed and simulated using 0.18µm CMOS technology in Cadence Spectre RF. The post-layout simulations exhibit the proposed circuit operates at 2.4 GHz with a bandwidth of 10 MHz. In addition, the conversion gain is changed from -3.9 dB to 23.9 dB with the variation of the controlled DC voltage from 0.5 to 1.8. At the high gain, the double-sideband noise figure (DSB-NF) is less than 3.7 dB, and its third-order intermodulation point (IIP3) is -9 dBm. The power consumption is 22 mW from the supply voltage of 1.8 V. The circuit occupies 743 µm×775 µm of core chip area.

Conclusion: Using the proposed circuit, the RF front end receiver does not need the low noise amplifier (LNA) and variable gain amplifier (VGA).

Introduction

In recent years, wireless communications have considerably developed, and the designers have sought to address the RF front-ends with higher level of integration and lower cost [1]-[7]. A direct conversion receiver (DCR) front-end suffers from DC offset due to self-mixing, I/Q imbalance, and flicker noise. However, it still is used widely due to small size, low cost, low power consumption, and the fewer number of external components [8], [9]. As illustrated in Fig. 1, the DCR front-end consists of RF bandpass filter (BPF), low-noise amplifier (LNA), I/Q mixer, variable gain amplifier (VGA), and lowpass filter (LPF).

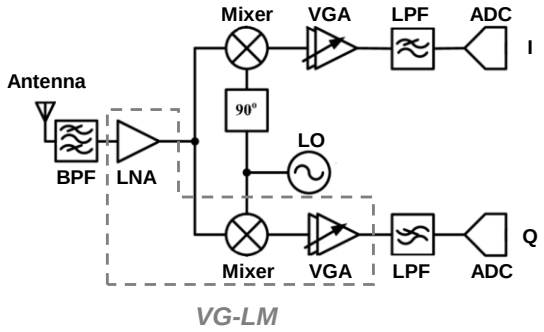


Fig. 1: Direct conversion front-end architecture.

As seen, the variable gain amplifier (VGA) is inserted between the mixer and the LPF to compensate the low conversion gain of the mixer and control the signal power level. Consequently, the VGA increases the dynamic range of the DCR [10]. The VGA is typically used along with the auxiliary circuits, such as common-mode feedback (CMFB), DC offset voltage cancellation, and the exponential current generator. The circuits provide a constant signal amplitude for the analog to digital converter (ADC) and eliminate the undesirable DC offset voltage [11].

Merging some blocks in RF front-end is an effective method to achieve high integration level and low cost. Martines et al. [12] designed a combined LNA and mixer with low power consumption and chip area. However, the proposed LNA-mixer exhibits low conversion gain and high noise figure (NF). Ryu et al. [13] proposed a variable gain mixer with automatic gain control (AGC). This proposed design achieves a wide variable conversion gain range with a maximum conversion gain of 10 dB. In addition, the AGC circuit suffers from the design complexity to obtain the dB linear function with MOS transistors. Kolios and Kalivas [14] used the dynamic current bleeding technique to realize the variable-conversion gain mixer (VCG-mixer). Moreover, they applied the inter-stage inductors to cancel the parasitic capacitances seen at the source of switching transistors. However, the circuit presents a low conversion gain range and occupies a large chip area. Wang and Saavedra [15] employed a Gilbert-Cell mixer with the reconfigurable gate widths in the RF transconductance transistor, thereby varying the conversion gain. However, the mixer does not obtain a continuous conversion gain range. Wu and Chou [16] applied forward body bias control to a body terminal of the RF transconductance and LO switching stages to achieve a mixer with variable conversion gain. The proposed mixer consumes low power, but it suffers from low conversion gain and a narrow tunable range. Kalamani [17] employed the double balanced mixer and the differential LNA to achieve high conversion gain, but it consumes high power. Hu et al. [18] offered a LNA-mixer with improved conversion gain and NF. The gain boosted and the current bleeding techniques are exploited to achieve a high gain and an appropriate NF. Gladson et.al. [19] used a low-noise transconductance amplifier (LNTA) in the RF transconductance stage of the down conversion mixer to reduce the noise of the switching stage. Moreover, the linearity of the low-noise stage is improved by using post-distortion based harmonic cancellation technique, that provides an enhanced spurios free dynamic range (SFDR) of up to 81.88 dB. Cao et al. [20] proposed a digitally controlled dedicated short range communications (DSRC) receiver operating at 5.8 GHz, specifically designed for the Chinese electronic toll collection system. The design utilizes a digital baseband for controlling LNA and mixer circuits. However, the LNA cannot exhibit a continuously variable gain, and it is characterized by four discrete modes. Guo et al. [21] employed a highly linear wideband differential LNTA for current-mode SAW-less receiver architecture. The design is developed by using an active-combiner feedback and complementary multi-gated transistor (MGTR) configurations, that provides high linearity with simultaneous compensations for the second- and third-order nonlinearity of transistors.

In this paper, the structural innovation is done to merge the LNA with down-conversion mixer, and VGA. The proposed variable gain LNA-Mixer (VG-LM) can control the conversion gain, translate the RF input to IF output with low noise performance, simultaneously, and exhibits higher level of integration. In the proposed circuit, an LNTA is inserted in the RF transconductance stage to control the conversion gain continuously by up to 20 dB. In addition, the proposed LNTA enhances LNA-mixer conversion gain (CG), thereby improving the noise performance effectively. The proposed VG-LM is designed over the RF frequency of 2.4 GHz for WLAN applications. The remainder of the paper is organized as follows. Section 2 presents the VG-LM structure and details the proposed LNTA. In Section 3, the simulation results are discussed, and the performance of the VG-LM is compared with previous studies. Finally, the conclusion is presented in Section 4.

Design of Proposed VG-LM

A. Conventional Gilbert Cell Mixer

Fig. 2 illustrates the double-balanced active mixer based on the Gilbert cell. As illustrated, it consists of the RF input, current switch, and load sections. The RF input is called the RF transconductance, which converts a voltage to a current signal by transistors of MRF. The RF signal passes from the LO switching for frequency translation, and it is commutated by transistors of MSW. Finally, the IF current converts to IF voltage by load resistors [22], [23].

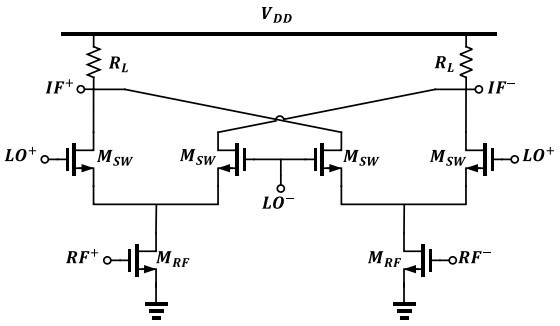


Fig. 2: Schematic of the conventional downconversion active mixer.

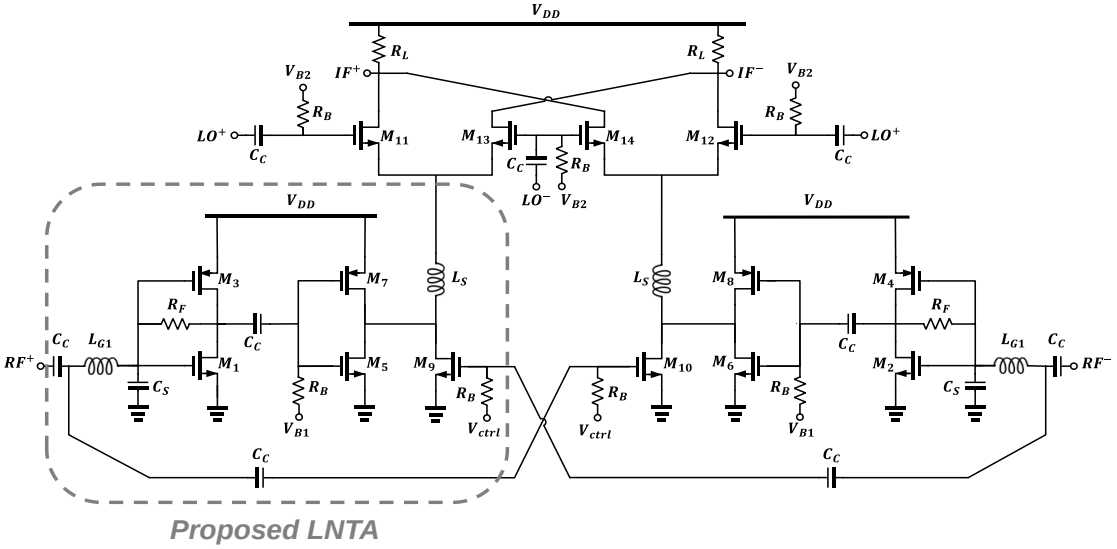


Fig. 3: Schematic of the proposed VG-LM.

The voltage conversion gain (CG) of the mixer is reduced by gradual LO transitions and the parasitic capacitor (C_P) that is seen at the source of switching transistors [17]. Therefore, the CG of the active mixer is defined as follows:

$$CG = \frac{2}{\pi} g_{m,RF} R_L \frac{g_{m,SW}(1-\alpha)}{\sqrt{C_P^2\,\omega^2 + g_{m,SW}^2}} \quad (1)$$

where $g_{m,RF}$ and $g_{m,SW}$ are the transconductances of the RF input and LO switching, respectively. α is equal to $2\Delta T/T_{LO}$, where ΔT is a fraction of each half cycle of the LO period (T_{LO}), that the LO transistors act as a balanced differential pair.

B. Proposed VG-LM

Fig. 3 illustrates the schematic of the proposed VG-LM. The proposed circuit exploits a low noise transconductance amplifier (LNTA) in the RF input stage of the mixer. The variable conversion gain can be realized by changing the LNTA's transconductance ($G_{m,LNTA}$) and transconductance of the mixer switching transistors through the DC control voltage (V_{ctrl}).

As shown in Fig. 4, the proposed LNTA consists of cascaded stages of a resistive shunt–shunt feedback amplifier (M_1 and M_3) and an inverter-based amplifier (M_5 and M_7). When the controllable bias voltage (V_{ctrl}) is low enough, M_9 operates in the saturation region, and the input signal is amplified with the common-source amplifier. Since the DC current of M_3 is reused by M_1, the power consumption of the input stage is reduced. This stage is self-biased by the feedback resistor of R_F and coupled to the second stage by the large *ac* coupling capacitance of C_C. The input stage of LNTA is designed to achieve the high voltage gain and low noise figure (NF), while the second stage provides linear-in-dB gain control characteristics. The inverter-based amplifier is loaded by M_9 with controllable bias voltage.

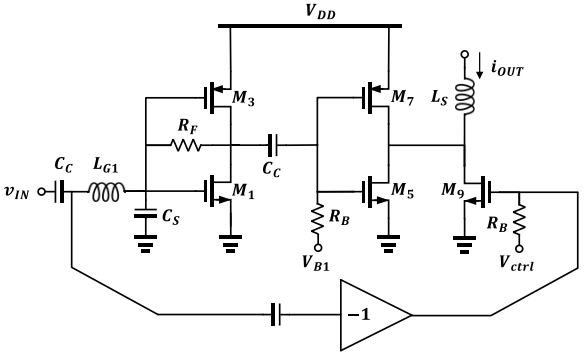


Fig. 4: Schematic of the proposed LNTA.

The current passing through M_9 can control the effective transconductance of the second stage. The transconductance of the LNTA can be degraded by the parasitic capacitances seen at the source of mixer switching transistors at high frequency. Therefore, an inductive series peaking L_S is inserted at the output.

C. Input Matching

The *LC* (L_{G1} and C_S) and resistive feedback techniques are inserted in the proposed input matching network. The series inductor, L_{G1}, is used to extend the RF bandwidth and reduce the noise contributed by LNTA. Assuming that the total impedance due to the gate-drain capacitances of M_1 and M_3 (C_{gd1}+C_{gd3}) is relatively higher than R_F, the small-signal equivalent circuit of the proposed LNTA is simplified, as illustrated in Fig. 5. As illustrated, the capacitor of C_S and the gate-source capacitances of M_1 and M_3 are merged as C_{eq1}. The total of the gate-source capacitances of M_5 and M_7 and their input Miller capacitances is represented by C_{eq2}, and C_{eq3} is the parasitic capacitance seen at the drain of M_9.

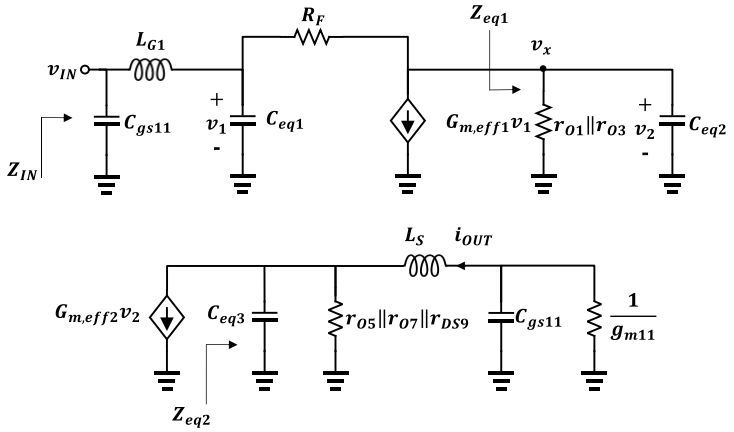


Fig. 5: Small-signal equivalent circuit of the proposed LNTA.

By neglecting the gate-drain capacitances, C_{eq3} equals C_{db5}+C_{db7}+C_{db9}. The input impedance is equal to the series combination of L_{G1} with the parallel combination of C_{eq1} and the impedance seen at the gate of M_1 and M_2 and is given by:

$$Z_{IN} = \frac{1}{C_{gs11}s} \| \left(L_{G1}s + \left(\frac{1}{C_{eq1}s} \| \frac{R_F + Z_{eq1}}{1 + G_{m,eff1}Z_{eq1}} \right) \right) \tag{2}$$

where $G_{m,eff1}$=g_{m1}+g_{m3} is the effective transconductance of the input stage, and Z_{eq1} represents the load impedance and is given by:

$$Z_{eq1} = (r_{O1}\|r_{O3}) \| \frac{1}{C_{eq2}s} \approx (r_{O1}\|r_{O3}) \tag{3}$$

where r_O represents the MOS output resistance. By substituting (3) in (2) and neglecting channel-length modulation, Z_{IN} can be rewritten as:

$$Z_{IN} = \frac{1}{C_{gs11}s} \| \left(L_{G1}s + \left(\frac{1}{C_{eq1}s} \| \frac{1}{G_{m,eff1}} \right) \right) \tag{4}$$

By assuming that C_S is high enough to satisfy $G_{m,eff1}/C_{eq1}$<<1/√($L_{G1}C_{eq1}$), the (4) reveals there is a dominant pole near dc and a resonant zero close to ω_0=1/√($L_{G1}C_{eq1}$). At the frequency of ω_0=2π×2.4 rad/s, Z_{IN} is obtained as follows:

$$Z_{IN} = \frac{L_{G1}G_{m,eff1}}{C_{eq1}} = (L_{G1}\omega_0)^2 G_{m,eff1} \tag{5}$$

According to (5), the input matching can be achieved by proper choice of $G_{m,eff1}$, and L_{G1}. Thus, $G_{m,eff1,}$ and L_{G1} values are chosen equal to 30 mA/V and 2.7 nH, respectively, to achieve input matching at 2.4 GHz.

D. Gain AnalysisSection Headings

Based on the small-signal equivalent circuit illustrated in Fig. 5 and (1), the CG of the proposed mixer can be obtained as follows:

$$CG = \frac{2}{\pi} G_{m,LNTA} R_L \frac{g_{m11}(1-\alpha)}{\sqrt{C_{gs11}^2\,\omega^2 + g_{m11}^2}} \cong \frac{2}{\pi} G_{m,LNTA} R_L (1-\alpha) \tag{6}$$

where $G_{m,LNTA}$ represents the total transconductance of LNTA and is given by:

$$G_{m,\,LNTA} = \frac{i_{OUT}}{v_{IN}} = \frac{i_{OUT}}{v_x} \times \frac{v_x}{v_{IN}} \tag{7}$$

where,

$$\frac{v_x}{v_{IN}} = \frac{-(G_{m,eff1}R_F - 1)Z_{eq1}}{C_{eq1}L_{G1}Z_{eq1x}s^2 + L_{G1}G_{m,eff1}Z_{eq1}s + Z_{eq1x}} \tag{8}$$

and,

$$\frac{i_{OUT}}{v_x} = \frac{G_{m,eff2}g_{m11}Z_{eq2}}{1 + g_{m11}Z_{eq2}} \times \frac{1}{1 + L_{G2}C_{eq2}s^2} \tag{9}$$

where Z_{eq1x}=Z_{eq1}+R_F, and $G_{m,eff2}$=g_{m5}+g_{m7} is the effective transconductance of the second stage, and Z_{eq2} represents the load impedances, and it is expressed as:

$$Z_{eq2} = \left(r_{O5}\|r_{O7}\|r_{DS9}\| \frac{1}{C_{eq3}s} \right) \| \left(L_S s + \left(\frac{1}{C_{gs11}s} \| \frac{1}{g_{m11}} \right) \right) \tag{10}$$

The channel resistance of M_9, r_{DS9}, depends on the controllable bias voltage of V_{ctrl}, and it can vary from r_{O9} to R_{ON9}=1/($\mu_n C_{OX}(W/L)(V_{ctrl}$-$V_{th})$) when M_9 is driven into the triode region. The π-network consisting of C_{eq3}, L_S, and C_{gs11} presents an infinite impedance at the frequency of 1/√($C_{eq1}C_{gs11}L_S$/(C_{eq1}+C_{gs11})), and therefore Z_{eq2} is simplified as:

$$Z_{eq2} = \left(r_{O5}\|r_{O7}\|r_{DS9}\| \frac{1}{g_{m11}} \right) \tag{11}$$

According to (11) and neglecting channel-length modulation, the (9) is approximately simplified as follows

at the resonance frequency of $1/\sqrt{(L_{G2}C_{eq2})}$:

$$\frac{i_{OUT}}{v_x} = \frac{G_{m,eff2}g_{m11}\left(r_{DS9}\|\frac{1}{g_{m11}}\right)}{\sqrt{2}\left(1+g_{m11}\left(r_{DS9}\|\frac{1}{g_{m11}}\right)\right)} \quad (12)$$

In addition, neglecting channel-length modulation and according to (3), the (8) is rewritten as:

$$\frac{v_x}{v_{IN}} = -\frac{G_{m,eff1}R_F}{C_{eq1}L_{G1}s^2 + L_{G1}G_{m,eff1}s + 1} \quad (13)$$

By proper choosing of L_{G1} and resonating with C_{eq1}, the gain peaking can be achieved, and (13) can be simplified at $\omega_0=1/\sqrt{(L_{G1}C_{eq1})}$ as follows:

$$\frac{v_x}{v_{IN}} = -\frac{R_F}{\omega_0 L_{G1}} \quad (14)$$

Consequently, by replacing (12) and (14) in (7), $G_{m,LNTA}$ is calculated as follows:

$$G_{m,\,LNTA} = \frac{i_{OUT}}{v_{IN}} \cong -\frac{G_{m,eff2}R_F g_{m11}\left(r_{DS9}\|\frac{1}{g_{m11}}\right)}{\sqrt{2}L_{G1}\omega_0\left(1+g_{m11}\left(r_{DS9}\|\frac{1}{g_{m11}}\right)\right)} \quad (15)$$

when V_{ctrl} is increased from V_{th} to supply voltage, M_9 enters from saturation to triode region, and v_{DS9} is decreased. Thus, r_{DS9} is reduced as well as $1/g_{m11}$. Moreover, the bias current of M_9 is effectively enhanced by increasing V_{ctrl}, and therefore, $G_{m,eff2}$ is reduced. Fig. 6 illustrates the g_{m11} and $G_{m,LNTA}$ versus V_{ctrl} under the input matching condition of Z_{IN}=50 Ω and operating M_5 in the triode region.

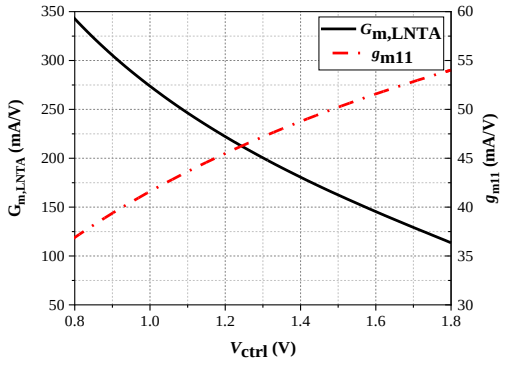


Fig. 6: Theoretical $G_{m,LNTA}$, and g_{m11} versus controllable bias voltage of M_9.

As can be seen, the conversion gain exhibits a wider range of variations than $G_{m,LNTA}$ due to increasing g_{m11} with V_{ctrl}.A primary section heading is enumerated by a Roman numeral followed by a period and is centered above the text. A primary heading should be in capital letters.

E. Noise Analysis

The thermal noise of all transistors and resistors and the flicker noise of the switching transistors are considered the noise sources of the downconversion active mixer. However, the flicker noise of the RF input section is translated up by ω_{LO}, and it does not appear at the baseband [22]. Therefore, the flicker noise contributed by LNTA is not considered in the noise analysis of the proposed VG-LM. The output thermal noise of the conventional downconversion active mixer is expressed as [17]:

$$\overline{v_{n.OUT}^2} = \overline{I_{n.M_{RF}}^2}R_L^2(1-\alpha) + \overline{v_{n.M_{SW}}^2}\left(2\,g_{m,SW}^2\alpha + C_P^2\omega^2(1-\alpha)\right)R_L^2 + 8kTR_L \quad (16)$$

where,

$$\overline{I_{n.M_{RF}}^2} = 4kT\gamma g_{m,RF} \quad (17)$$

$$\overline{v_{n.M_{SW}}^2} = \frac{4kT\gamma}{g_{m,SW}} \quad (18)$$

where k and T are Boltzmann constant, and the absolute temperature, respectively, and γ represents the MOS transistor thermal noise coefficient. For the proposed VG-LM, the first term in (16) should be substituted by the output thermal noise current contributed by LNTA ($I^2_{n,LNTA}$) as follows:

$$\overline{v_{n.OUT}^2} = \overline{I_{n.LNTA}^2}R_L^2(1-\alpha) + \overline{v_{n.M_{SW}}^2}\left(2\,g_{m,SW}^2\alpha + C_P^2\omega^2(1-\alpha)\right)R_L^2 + 8kTR_L \quad (19)$$

The simplified model for LNTA noise analysis is derived as illustrated in Fig. 7. Based on Fig. 7 and neglecting the channel-length modulation, $I^2_{n,LNTA}$ is calculated as:

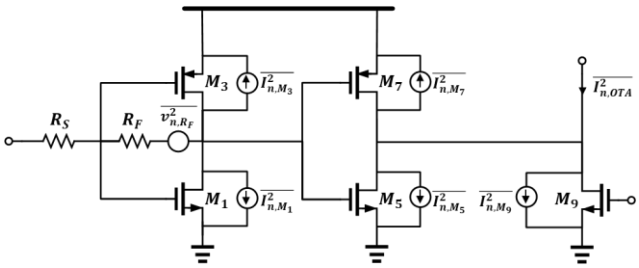


Fig. 7: Simplified equivalent circuit of LNTA for noise calculation.

$$\overline{I_{n.LNTA}^2} = \left(\left(\overline{v_{n.R_F}^2} + \left(\overline{I_{n.M_1}^2} + \overline{I_{n.M_3}^2}\right)\left(\frac{R_F + R_S}{1 + G_{m,eff1}R_S}\right)^2\right)G_{m,eff2}^2 + \left(\overline{I_{n.M_5}^2} + \overline{I_{n.M_7}^2}\right)g_{m11}^2\left(r_{DS9} \| \frac{1}{g_{m11}}\right)^2 + \overline{I_{n.M_9}^2}\right) \quad (20)$$

Under perfect matching condition and operating M_9 in triode region, (20) is rewritten as:

$$\overline{I_{n.LNTA}^2} = 4kT\left(\left(R_F + \gamma G_{m,eff1}\frac{(R_F + R_S)^2}{4}\right)G_{m,eff2}^2 + \gamma G_{m,eff2} + \frac{1}{r_{DS9}}\right) \quad (21)$$

where r_{DS9} represents the channel resistance of M_9 when it enters the triode region. γ is the excess noise coefficient and its value is assumed 1.3 for 180 nm transistors [24]. By assuming R_F>>R_S, the single side-band noise figure contributed by LNTA ($NF_{SSB,LNTA}$) can be obtained as:

$$NF_{SSB,LNTA} \cong \frac{\pi^2\left(4 + \gamma G_{m,eff1}R_F\right)}{4G_{m,eff1}R_F(1-\alpha)} \times \frac{\pi^2\gamma}{G_{m,eff1}G_{m,eff2}R_F^2(1-\alpha)} \quad (22)$$

To theoretically evaluate the noise performance of the proposed VG-LM, Fig. 8 illustrates the double side-band NF contributed by LNTA. As can be seen, the NF is related to the effect of M_9, and increasing V_{ctrl} allows further increase of NF.

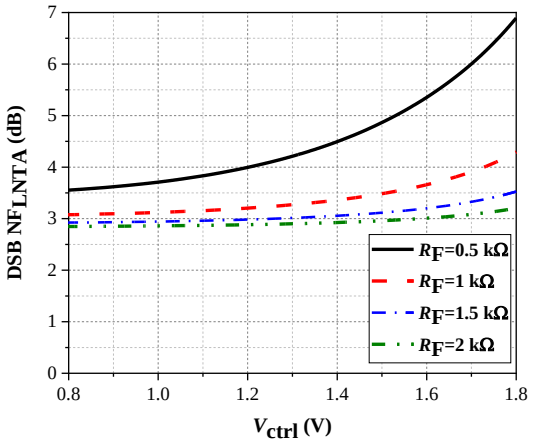


Fig. 8: Theoretical DSB NFLNTA versus controllable bias voltage of M_9 with α=0.1 and γ=1.33.

Moreover, for higher values of R_F, NF_{LNTA} exhibits less changes with increasing V_{ctrl}. However, choosing high values of R_F can degrade the input matching impedance.

Thus, the R_F value is chosen equal to 1.5 kΩ to achieve desirable input matching and noise performance along with high conversion gain. According to Fig. 6 and Fig. 8, the conversion gain of the proposed mixer can be continuously controlled by the bias voltage of M_9, while DSB NF is enhanced by less than 1 dB. However, as illustrated in Fig. 6, the transconductance of switching transistors (g_{m11}) is increased by increasing V_{ctrl}, and as a result, can enhance the flicker noise contributed by switching transistors.

Simulation Results and Discussion

The proposed VG-LM with an RF frequency of 2.4 GHz and IF frequency of 10 MHz is designed and simulated in 180 nm RF-TSMC CMOS process by Cadence Spectre RF. To reduce the effect of parasitic capacitors, the length of transistors is chosen to be 0.18 µm. Moreover, the width of transistors is designed and optimized by considering the above analysis and power consumption. Table 1 presents the optimized values of device sizes for the proposed VG-LM.

Table 1:. Device sizes of the proposed VG-LM

Device	Parameters	Value
Transistor (*W*/*L*)	$M_{1,2}$	(66 µm/0.18 µm)
	$M_{3,4}$	(32 µm/0.18 µm)
	$M_{5,6}$	(215 µm/0.18 µm)
	$M_{7,8}$	(15 µm/0.18 µm)
	$M_{9,10}$	(42 µm/0.18 µm)
	$M_{11\text{-}14}$	(408 µm/0.18 µm)
Inductor (nH)	L_{G1}	2.2
	L_S	5.9
Resistor (kΩ)	R_F	1.5
	R_B	20
	R_L	0.35
Capacitor (pF)	C_S	0.6
	C_C	5
Bias voltage (V)	V_{B1}	0.62
	V_{B2}	0.56
	V_{DD}	1.8

The VG-LM consumes 12.46 mA and 14.7 mA from a 1.8 V supply voltage when the conversion gain is maximum and minimum, respectively. The circuit layout of the proposed VG-LM is illustrated in Fig. 9. The chip area is about 0.57 mm^2 (743 µm×775 µm), including all the pads and guard rings. Fig. 10 shows the post-layout simulated input return loss. By changing the control bias voltage of M_9 (V_{ctrl}), all the simulated S_{11} are less than −10 dB over the input frequency of 2.4 GHz. This performance proves an appropriate design of input matching and demonstrates the input matching is hardly affected by changing the V_{Ctrl}.

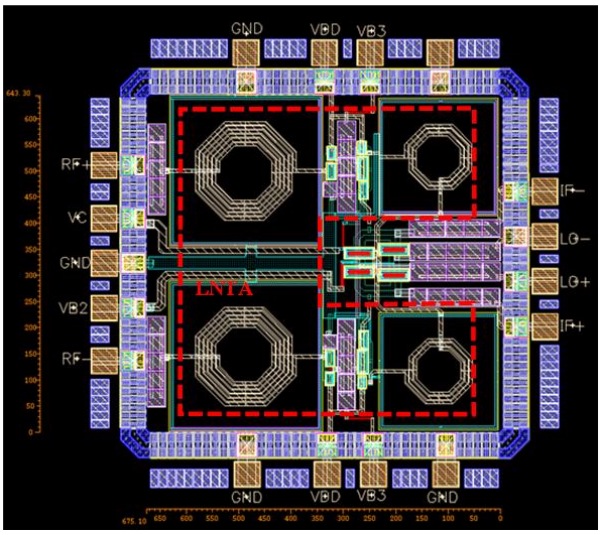


Fig. 9: Circuit layout of the proposed VG-LM.

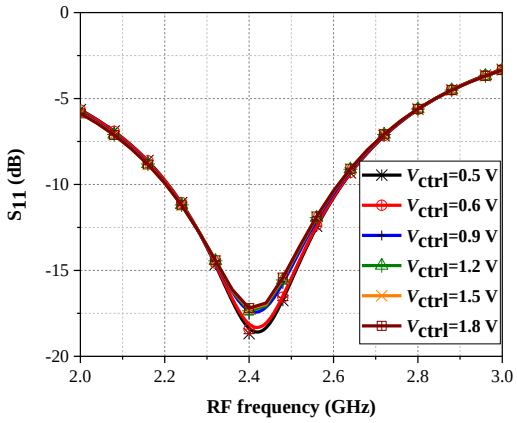
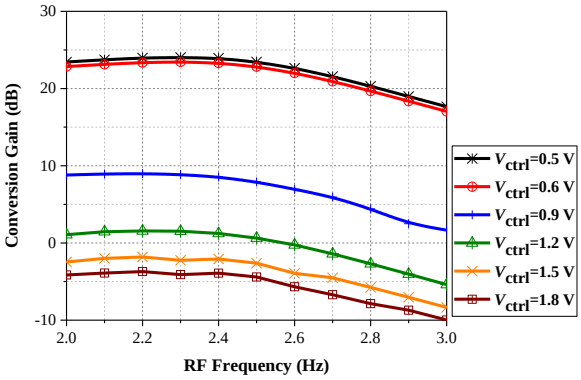


Fig. 10: Simulated results of input return loss with different values of V_{ctrl}.

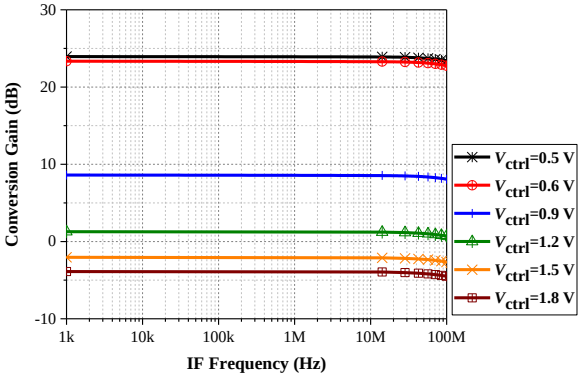
By considering P_{LO}= 0 dBm, the simulated conversion gain (CG) is illustrated in Fig. 11. As illustrated, the simulated conversion gain can be controlled continuously from 23.9 dB to -3.9 dB when V_{ctrl} is varied from 0.5 to 1.8 V at 2.4 GHz.

Fig. 12 presents the noise performance of the VG-LM in the intermediate frequency (IF) range of 1 kHz–10 MHz. At the IF frequency of 10 MHz, the simulated result indicates the DSB NF ranges from 3.74 dB to 6.71 dB when V_{ctrl} is changed from 0.5 V to 1.8. Moreover, it can be seen that DSB NF increases slightly as the conversion gain drops. As mentioned in the previous section, the flicker noise is relatively affected by V_{ctrl} changes.

To evaluate the nonlinear performance, the two tones with 4.125 MHz spacing are applied to the proposed VG-LM. Fig. 13 illustrates simulated input third-order intercept point (IIP3) at V_{ctrl}=0.5 V and V_{ctrl}=1.8 V. As illustrated, the VG-LM has IIP3 of -9 dBm and -6 dBm when the control bias voltage is 0.5 V and 1.8 V, respectively.



(a)



(b)

Fig. 11: Simulation results of the conversion gain versus (a) RF frequency and (b) IF frequency.

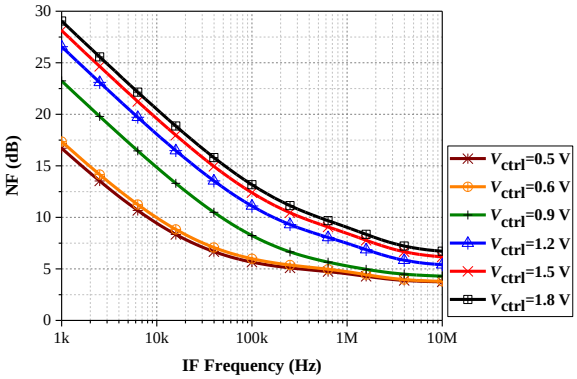


Fig. 12: Simulation results of NF versus IF frequency.

Furthermore, the output third-order intercept point (OIP3) values at the control voltages of 0.5 V and 1.8 V are equal to 17.5 dBm and 7.8 dBm, respectively. In addition, to evaluate the limitations arising from both noise and interference, the spurious-free dynamic range (SFDR) is evaluated as follows [22]:

$$SFDR\ [dB] = \frac{2}{3}(P_{IIP3}[dBm] + 174[dBm] - NF[dB] - 10\log(BW)) - SNR_{min} \quad (23)$$

By assuming minimum output SNR (SNRmin) of 10 dB and the bandwidth (BW) of 10 MHz, the resulting SFDR is equal to 50.84 dB at the control voltage of 0.5 V.

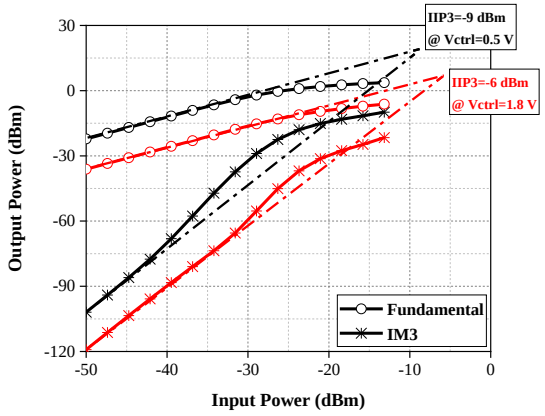


Fig. 13: Simulated IIP3 of the proposed VG-LM.

In Fig. 14, the simulated 1 dB-compression point (P_{1dB}) is illustrated for the maximum and minimum conversion gain. The results show that the VG-LM has a P_{1dB} of -21 dBm and -16 dBm at V_{ctrl}=0.5 V and 1.8 V, respectively.

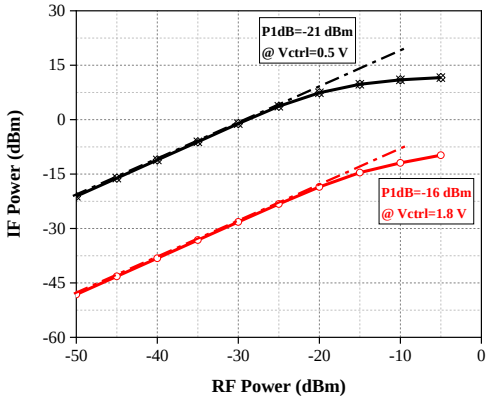
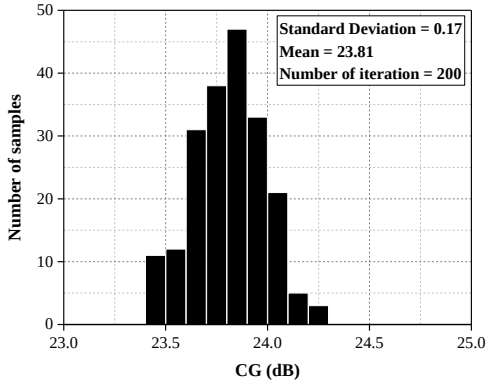
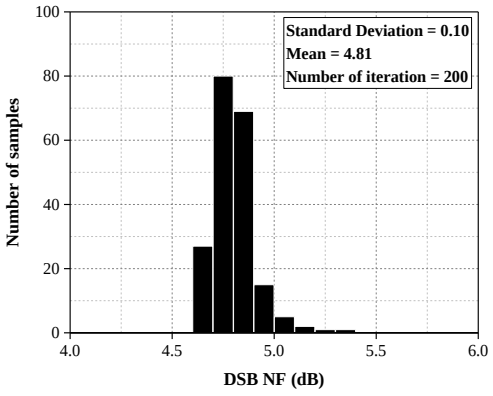


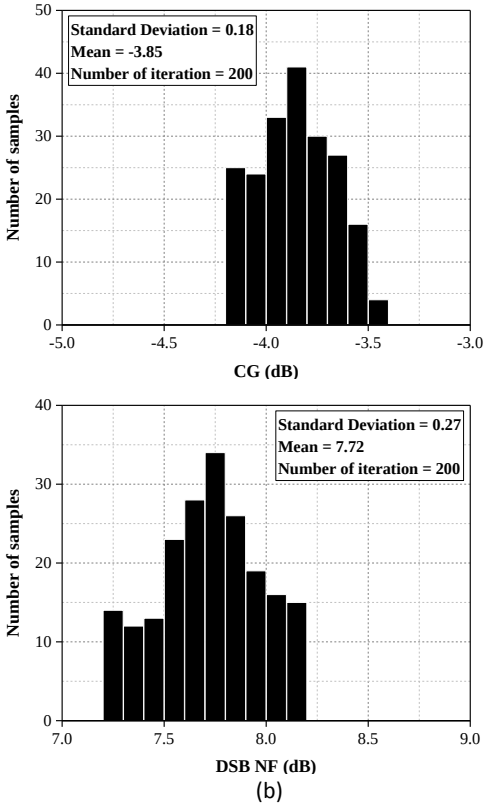
Fig. 14: Simulated P1dB of the proposed VG-LM.

The Monte Carlo results, including process variations and mismatch, are illustrated in Fig. 15 for 200 samples at the RF frequency of 2.4 GHz and the IF frequency of 10 MHz. The results show a mean CG of 23.81 dB with a standard deviation of 0.17 dB and DSB NF of 4.81 dB with a standard deviation of 0.1 dB at the maximum conversion gain. Moreovere, the mean CG is -3.85 dB with a standard deviation of 0.18 dB, and DSB NF is 7.72 dB with a standard deviation of 0.27 dB at the minimum conversion gain.





(a)



(b)

Fig. 15. Monte Carlo simulation results of 200 runs. (a) At the maximum CG. (b) At the minimum CG.

Consequently, the proposed mixer exhibits good stability against process variations and mismatch.

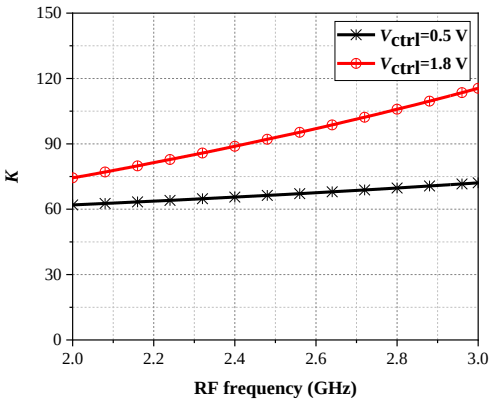
Fig. 16 (a), and (b) illustrates the stability factors based on the Sparameters to consider the stability of the proposed VG-LM. The necessary and sufficient conditions for unconditional stability are given as follows:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + \Delta^2}{2|S_{12}||S_{21}|} > 1 \quad (24)$$

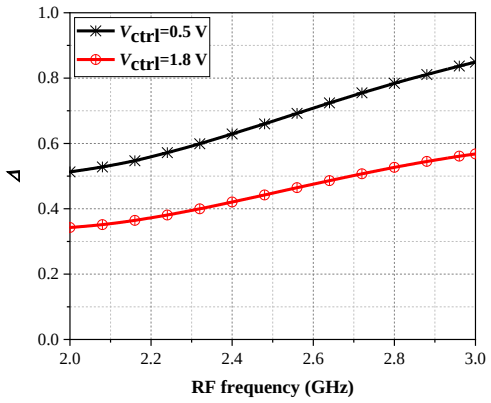
$$\Delta = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (25)$$

Table 2: Simulation results of the proposed mixer with temperature and process corners.

Parameters	CG(dB)	NF(dB)	IIP3(dBm)	S_{11}(dB)
FF@-40	23.77	4.15	-9.2	-16.48
TT@27	23.93	3.74	-9	-18.68
SS@85	16.95	5.025	-7.6	-20.35



(a)



(b)

Fig. 16: Simulated stability factor of the proposed VG-LM.

As can be seen, the proposed VG-LM satisfies the conditions for unconditional stability over the frequency band of interest at V_{ctrl}=0.5 V and V_{ctrl}=1.8 V. Also, Table 2 presents the simulation results in different corners of the process and temperature changes with V_{ctrl}=0.5 V. As can be seen, in the worst case, the conversion gain drops to 16.95 dB because it strongly relies on the transconductance of M_{11}. The simulated performance of the proposed VG-LM is summarized in Table 3, and compared with the state-of-the-art results.

As can be seen, the proposed circuit benefits from high conversion gain, good input match, and low NF when it works in the maximum conversion gain. Moreover, it exhibits a wide conversion gain range and slight variations in the NF.

The following figure of merit (FoM) is used to have a fair comparison as follows:

$$FoM = 10\log\left(\frac{10^{\frac{CG_{max}(dB)}{20}} \times 10^{\frac{GR(dB)}{20}}}{10^{\frac{NF_{min}(dB)}{10}} \times P_{DC}(mW)}\right) \quad (26)$$

where P_{DC} and GR represent the power consumption and gain range, respectively.

As seen in Table 3, the proposed VG-LM has a high conversion gain compared to the recent structure as well as low DSB NF.

It results in an outstanding FoM proving the effectiveness of using the proposed LNTA in the RF stage of the Gilbert cell mixer. Although the IIP3 is not as high as [13], [25] and [27], it is comparable with [15], [16] and [29], which is acceptable for using in WLAN applications. The mixer reported in [13] exhibits a wide gain range, but it has low conversion gain. Moreover, some RF front-end circuits [26], [28] and [30] are evaluated to present a complete comparison with recent studies.

However, these circuits do not realize the variable gain and FoM is not reported for them.

Barzgari et al. [26] proposed a quadrature and differential RF front-end receiver for low power applications. By combining balun, LNA, mixer, and oscillator in a single stage, the proposed circuit features high integration level and low power consumption. Vitee et al. [28] presented an inductively source degenerated balun-LNA mixer.

They achieve good linearity by two linearization techniques but the NF and chip are are high in comparison with other designs. Bae et al. [30] proposed a new reconfigurable front-end circuit by using a reconfigurable parallel mixing subharmonic (SHM)-based time-interleaved RF channelizer. The circuit achieves high conversion gain but the linearity is the lowest among the RF front-end designs.

Table 3: Performance summary of the proposed VG-LM and comparison with previous works

Ref.	[13]	[16]	[17]	[18]	[19]	[20]	[25]	[26]	[27]	[28]	[29]	[30]	**This work**
CMOS Tech. (µm)	0.18	0.18	0.18	0.18	0.18	0.13	0.13	0.18	0.18	0.13	0.13	0.065	**0.18**
Topology	Mixer +VGA	Mixer +VGA	LNA +Mixer	LNA +Mixer	LNTA +Mixer	RX	Mixer +VGA	RX	Reconfig. Mixer	Balun+ LNA+ Mixer	Mixer +VGA	Reconfig. LNA+Mixer	**LNTA +Mixer +VGA**
Maximum CG[a] (dB)	8	24.2	22.28	20	17.87	45	17	57	19.67	22	23.7	46.7	**23.9**
Measurement Method	Sim.	Meas.	Sim.	Sim.	Sim.	Meas.	Meas.	Meas.	Meas.	Meas.	Meas.	Meas.	**Sim.**
LO Power (dBm)	0	-8	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0	N/A	0	**0**
RF Frequency (GHz)	1.4-1.6	1.8	2.4	2-10	2.4	5.8	1-12	2.2-2.8	0.7–2.3	2.2-3	1-6	0.3-0.8	**2.2-2.6**
IF Frequency (MHz)	N/A	10	595	10	N/A	5	110	2	10	100	140	3-10	**10**
Minimum DSB NF[a] (dB)	N/A	14	1[d]	6.8	5.9	<15	11	10.5	8.03	7.2	3.8	5.2	**3.74**
Chip area (mm^2)	0.02[b]	0.93[c]	N/A	0.52[b]	0.1	0.75	0.105[b]	0.75	0.71[c]	1.16	0.43[b]	3.6[c]	**0.57[c]**
Supply voltage (V)	1.8	0.8	1.8	1.8	1.8	1.5	1.2	0.8	1.8	1.2	1.5	1.2	**1.8**
P_{DC}[a] (mW)	7.56	2	37.4	7.2	9	33	5.9	0.34	23.76	3.15	N/A	24.7	**22.46**
IIP3[a] (dBm)	7	-11	N/A	-1	11.83	-44	8.6	-15.5	8.5	16	-4	-22.3	**-9**
S_{11}[a] (dB)	N/A	N/A	N/A	-7	-9	-23.7	N/A	<-10	N/A	<-10	-15	N/A	**<-10**
GR (dB)	45	9.7	N/A	3	N/A	N/A	15.8	N/A	18	N/A	13	6.4	**27.8**
FoM	N/A	-0.06	N/A	-3.8	N/A	N/A	-2.3	N/A	-2.93	N/A	N/A	7.42	**8.59**

a. High gain
b. Core
c. Core + Pads
d. only LNA

Conclusion

In this paper, a merged LNA-mixer with 27.8 dB variable gain range is presented. Using a low noise transconductance amplifier (LNTA) in the RF stage of the active mixer, a wide conversion gain range is realized without significant degradation in the noise figure. The proposed variable conversion gain LNA-mixer (VG-LM) is designed and simulated in RF-TSMC 0.18 µm CMOS technology. The post-layout simulated results exhibit an input matching (S_{11}) less than -10 dB, the maximum conversion gain of 23.9 dB, and the minimum DSB noise figure of 3.74 dB at the input frequency of 2.4 GHz. The simulated results demonstrate that the proposed VG-LM could be suitable for the low noise and wide tunable gain range RF front-end receivers in WLAN applications.

Author Contributions

M. A. Mallaki and A. Bijari developed the theoretical idea and performed the analytic calculations. M. A. Mallaki carried out the simulations. All authors discussed the results and contributed to the final manuscript. A. Bijari supervised the project.

Acknowledgment

We thank our colleagues from the university of Mashhad (FUM) who provided insight and expertise that greatly assisted the research. We thank M. Forouzanfar assistance for comments that greatly improved the manuscript.

Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

Abbreviations

CMOS	Complementary Metal Oxide Semiconductor
LNA	Low Noise AmplifierMultispectral
VG-LM	Variable Conversion Gain LNA-Mixer
WLAN	Wireless Local Area Network
LNTA	Low Noise Tansconductance Amplifier
DSB-NF	Double-Sideband Noise Figure
VGA	Variable Gain Amplifier
DCR	Direct Conversion Receiver
BPF	Bandpass Filter
LPF	Lowpass Filter
CMFB	Common-Mode Feedback
ADC	Analog to Digital Cconverter
NF	Noise Figure
AGC	Automatic Gain Control l
VCG	Variable-Conversion Gain
SFDR	Spurios Free Dynamic Range
DSRC	Dedicated Short Range Communications
MGTR	Multi-Gated Transistor
RF	Radio Frequency
IF	Intermediate Frequency
LO	Local Oscillator
CG	Conversion Gain
GR	Gain Range

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How to cite this paper:
A. Bijari, M. A. Mallaki, "A merged LNA-Mixer with wide variable conversion gain and low noise figure for WLAN direct-conversion receivers," J. Electr. Comput. Eng. Innovations, 12(1): 175-186, 2024.

DOI: 10.22061/jecei.2023.10124.679

URL: https://jecei.sru.ac.ir/article_1987.html