Journal of Electrical and Computer Engineering Innovations
(JECEI)
Journal homepage: http://www.jecei.sru.ac.ir

Research paper

# A New High-Speed Multi-Layer Three-Bits Counter Design in Quantum-Dot Cellular Automata Technology

*G. Asadi Ghiasvand, M. Zare *, M. Mahdavi*

*Department of Electronics, Faculty of Engineering, Shahr-e-Qods Branch, Islamic Azad University, Tehran, Iran.*

**Article Info**

**Article History:**
Received 24 July 2023
Reviewed 28 September 2023
Revised 29 October 2023
Accepted 05 November 2023

**Keywords:**
Digital circuit design
Quantum-Dot-Cellular Automata
Multi-layer design
Three bits counter
T flip-flop

*Corresponding Author's Email Address:
*d.mehdi.zare@gmail.com*

**Abstract**

**Background and Objectives:** Quantum-dot Cellular Automata technology is a new method for digital circuits and systems designs. This method can be attractive for researchers due to its special features such as power consumption, high calculation speed and small dimensions.
**Methods:** This paper tries to design a three-bits counter with minimum area and delay among the other circuits. As the circuit dimensions are reduced, the area and consequently, the delay are decreased, too. Therefore, this paper tries to design a three-bits counter with minimum dimensions and delay. The proposed counter contains 96 cells and is designed in three layers. It has the least area and delay compared to the priors.
**Results:** The circuit simulation illustrates 0.08 $\mu m^2$ of area occupation and one clock cycle delay. In comparison with the best previous design, which includes 110 cells, the cells number, area and delay are decreased by 12.72%, 27.27% and 33.33%, respectively. Also, the cost of the circuit has been improved by 54.32%. The power analysis of the design shows 13% reduction in the total energy dissipation of the circuit compared to the best prior work. The circuit reliability versus temperature variations has been simulated and the results represent suitable stability. The fault tolerance of the circuit which is occurred by the displacement faults represents normal operation of the circuit.
**Conclusion:** As the counter is an element which is implemented in several digital systems, its area reduction causes the whole system area to be reduced. Also, the circuit delay has been decreased significantly which means that the circuit can be employed by high speed systems.



## Introduction

With the advancement of technology and moving towards nanotechnology, circuit speed and dimensions are becoming the important factors that need to be improved. One of the proposed technologies besides the complementary metal oxide semiconductor (CMOS) [1] is the quantum dot cellular automata (QCA), which is a novel nanoscale design method proposed by Lent in the 1993. The QCA is a nano-dimension technology and the digital circuits can be designed and implemented by this method [2]-[6].

One of these circuits is the counter which is widely used in digital systems. In [7], a counter has been presented by JK flip-flop, which has 278 cells, area of 0.33 $\mu m^2$ and delay of 2 clock cycles. The cells number and area of this circuit are high. In [8], a counter by three consecutive T flip-flops has been proposed, which has 244 cells, area of 0.346 $\mu m^2$ and delay of 4.25 clock cycles. The design advantage is a NOT gate, which prevents signal weakness. In [9], a 3-bits counter has been designed by T flip-flop, which has 238 cells, area of 0.361 $\mu m^2$ and delay of 2.25 clock cycles. In this design,

the circuit delay and cost have been improved compared to the circuit in [8].

In [10], a D flip-flop counter has been presented by 196 cells which has good delay and cost. A counter in [11], has employed D flip-flop and has 174 cells, area of 0.194 $\mu m^2$ and delay of 3 clock cycles. This design has improved cells number and area, but is not optimal in terms of delay and cost. In [12], a counter with 140 cells has been presented by T flip-flop and each T flip-flop contains one XOR logic gate. A counter with 110 cells has been proposed in [13] that is the best design in terms of delay, area and cost compared to the priors. As shown in Fig. 1, the main advantage of the circuit in [13] is the crossing wires at two different clock phases. So, the wires cross each other with the minimum area and delay.

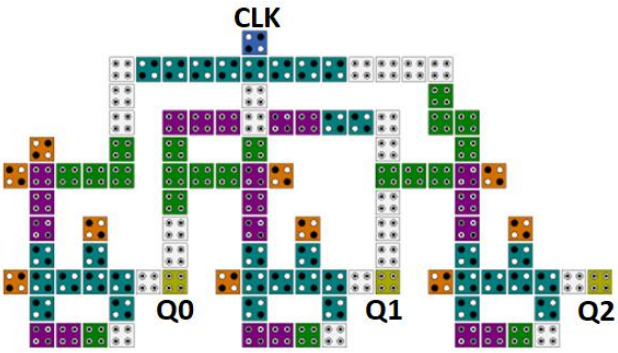



Fig. 1: Structure of three-bits counter with 110 cells [13].

*Main contributions:* We design a new 3-bits counter in this paper and follow these contributions:

1- It has been tried to design a circuit with the minimum number of cells.
2- Since the counter delay is related to the delay of T flip-flops, the implemented T flip-flops structures have been redesigned to improve the circuit delay. This will qualify the circuit for high-speed applications.
3- The total energy dissipation of the circuit has been improved.
4- It has been tried to preserve the circuit stability and the circuit fault tolerance in normal situation.

In continuous of the paper, the background of the QCA is discussed in section 2. In Section 3, the circuit design method is introduced and the proposed multi-layer 3-bits counter is explained. Simulation results and comparisons, the circuit energy analysis, and reliability are represented in section 4 and finally, the conclusion is given in section 5.

## QCA Background

The QCA is a nano-electronics computing architecture and is implemented to build circuits in nano-dimensions [14]. The basic unit in the QCA is its cell. As shown in Fig. 2, the QCA cell shape is square and consists of four quantum dots [15]-[16].

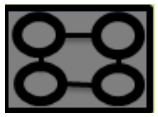
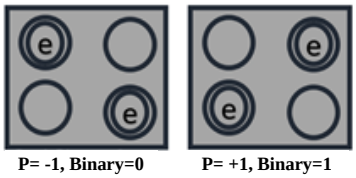
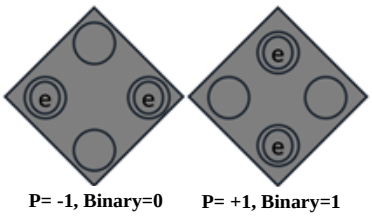


Fig. 2: Structure of a QCA cell.

The cell with four quantum dots, positioned at the corners of a square, contains two free electrons. An electron can be quantum-mechanically confined in a quantum dot. Due to the Coulombic interaction, electrons occupy the farthest possible positions from each other [17]. Therefore, the two stable states are the corners of the QCA cell and consequently, the possible polarizations are P = "-1" and P = "+1", which are translated as logics '0' and '1', respectively. The logics of the QCA cell are shown in Fig. 3(a) and 3(b). The standard distance between two adjacent cells is 2 nm and the cell standard dimensions are 18 x 18 $nm^2$, as shown in Fig. 4 [10].




(a)




(b)

Fig. 3: (a) The angle of electron is 90. (b) The angle of electron is 45.

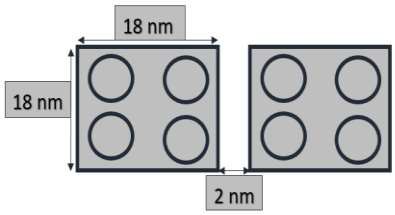
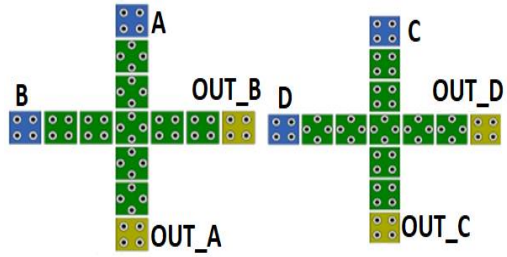


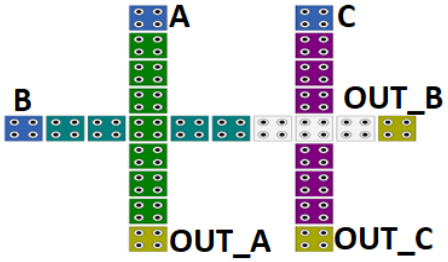

Fig. 4: Quantum dot cell dimensions.

The Coulombic interaction effects the adjacent cells and transfers the logic of one cell to the other cells. Therefore, the consecutive cells can create a QCA wire [18]. Since there is no current and output capacitor in the circuit, the QCA has lower power consumption compared to the CMOS. The QCA has simple structures for 'AND' and 'OR' gates, and has the ability to cross the

wires over each other. In classical binary QCA, wires crossing can be implemented by two methods that are coplanar wires and multi-layer wires. In the coplanar, the cells can cross with two different orientations or with two different clock phases as shown in Fig. 5. In multiple layers, one of the wires is transferred to the second layer and then returns to the first layer. Thus, two wires cross without affecting each other. Fig. 6 shows the overview of the multi-layer wires. It is proved that the multi-layer approach is more robust than the coplanar method [19]. In coplanar crossing, the wire coupler is loose and can be affected by the random external influences. In multi-layer, intermediate layers are used to prevent any possible crosstalk. Each layer can be employed as an active layer on which a new circuit can be designed independently [20]. A multi-layer model decreases the overall area and thus potentially consumes less chip area compared to the coplanar approach.




(a)




(b)

Fig. 5: Coplanar wires (a) Two wires crossing in 45& 90-degrees. (b) Two wires crossing with 2 different clock phases.

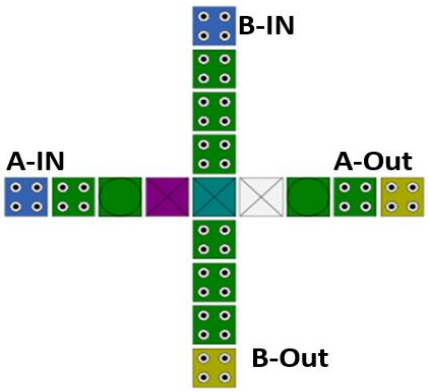
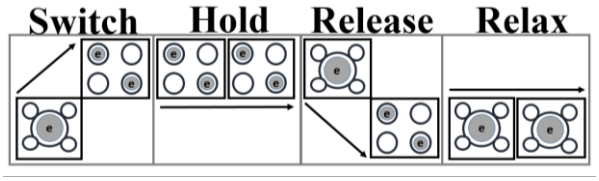
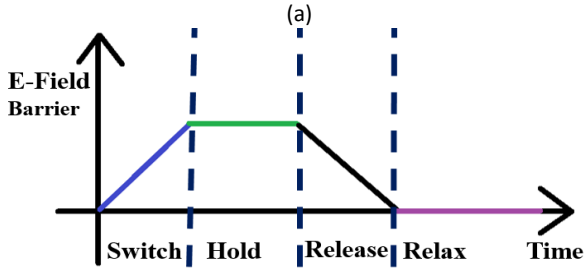



Fig. 6: Multi-layer wires crossing.

Binary logic movement in the QCA requires clocking. Timing/synchronization in the QCA is done by the cascaded clocking of four distinct and periodic phases as shown in Fig. 7.




(a)




(b)

Fig. 7: (a) Clock diagrams in QCA. (b) Clock phases in QCA.

The phases are rising (switch), falling (Release), staying at high potential (Hold) and staying at low potential (Relax). The applications of clocking are:

1- Creating an appropriate mechanism for synchronous movement of data in the circuit.

2- Determining the direction of data movement in the circuit.

3- Supplying the required power for the operation of the circuit.

A tool for the QCA circuits simulations is “QCA Designer”. In the “QCA designer” tool, the phase of the cells, along with the type of the cells (input/output), are determined by a special coloring which are shown in Fig. 8.

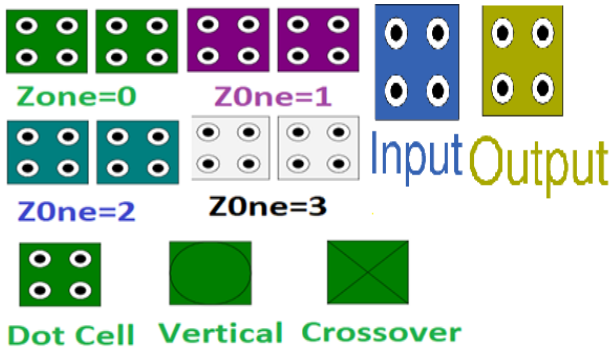



Fig. 8: The clock phases of the QCA and coloring of the cells.

As mentioned, by arranging the QCA cells in a line, the polarity of the first cell is transferred to the last cell and acts like a wire. In general, two wiring methods are utilized in the QCA. The first method is standard wiring and is accomplished as shown in Fig. 9(a). The second

method in Fig. 9(b) is called complementary chain, which cells are rotated 45 degrees with "+1" and "-1" polarization. The advantage of this type of wiring is its ability to transfer both the input signal and the reverse of the input signal in odd and even cells, respectively.

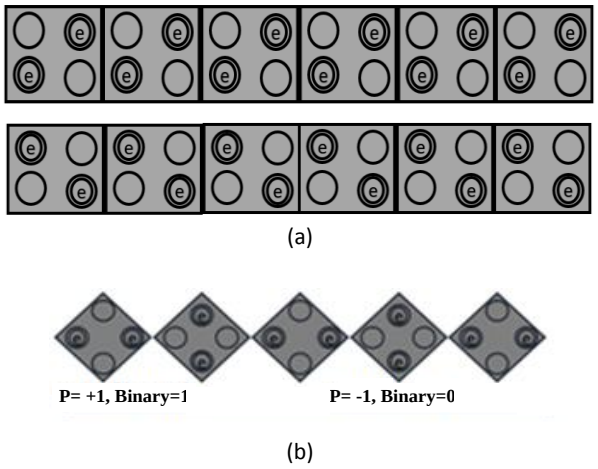



Fig. 9: (a) standard wiring. (b) complimentary chain wiring.

## Proposed Circuit

The interference minimization between wires and clock synchronization can be implemented in multi-layer designs [21]-[22]. Also, the multi-layer method reduces the overall area of the chip compared to the coplanar designs [23]. Therefore, to design the circuit with minimum area, the proposed circuit has been implemented with 3-layers. It has three output bits and contains 96 cells.

### *A. Design Methodology*

To propose a new circuit, we have employed the circuit in [13] as the base circuit and follow this algorithm to improve it:

1- Try to optimize the elements of the circuit. This will help you to optimize the whole circuit parameters.

2- Try to minimize the circuit dimensions. If the circuit dimensions are reduced, you have the opportunity to reduce the circuit delay.

3- If at least one of the previous steps has been performed successfully, simulate the circuit to see whether the circuit parameters are improved or not. If the parameters are improved, go to the next step, otherwise the circuit is not a good candidate as the new circuit.

4- Check the stability of the circuit. If it is stable, the new circuit has been designed correctly, otherwise the proposed circuit must be redesigned again in the first or second steps.

The flowchart of the circuit design methodology is depicted in Fig. 10.

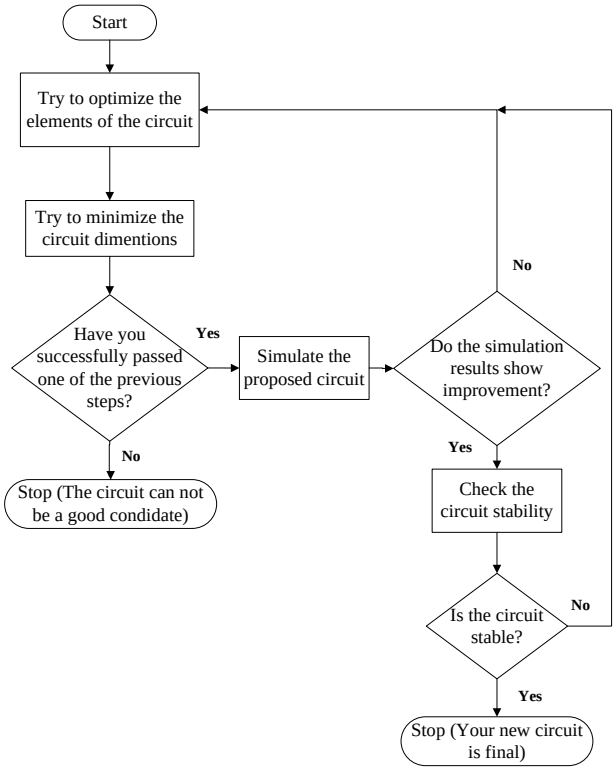



Fig. 10: The flowchart of the design methodology.

### *B. T Flip-Flop Structure*

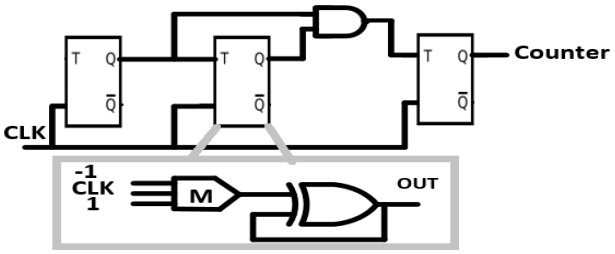
A counter is constructed by the flip-flops. According to the flowchart, we try to improve the flip-flops of the circuit in this section. The block diagram of the circuit in Fig. 11(a) shows three consecutive T flip-flops. The structure of each T flip-flop includes one 'XOR' gate and one 'AND' gate. The 'AND' gate is constructed by a three inputs majority gate which its inputs are "+1" and "-1" constant polarizations and the CLK signal. Totally, six majority gates have been utilized to design 'AND' and 'XOR' gates. Fig. 11(b) shows the internal structures of 'AND' and 'XOR' gates.

The block diagram of the T flip-flop is similar to [13]. However, as shown in Fig.12, its structure has the following differences:

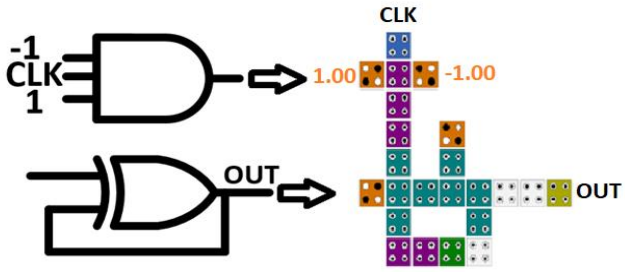
1- To reduce the number of cells in the 'XOR' majority gates of the first and third T flip-flops, normal cells employ phase 1 and fixed cells employ phase 2 of the clock. This will synchronize the data current and controls the electrons movement in the cells.

2- The input clock is applied directly to each T flip-flop which improves the circuit delay.

These simple modifications lead to the first aim of our research and decrease the delay of the T flip-flops. Consequently, by modification of the T flip flops, the total circuit delay is reduced and causes the circuit to be a candidate for high speed applications.

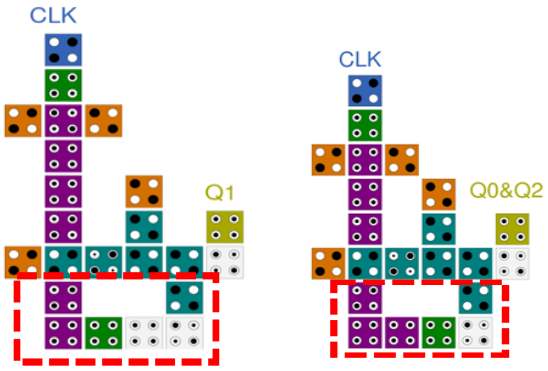



(a)




(b)

Fig. 11: (a) Block diagram of three bits counter. (b) Structure of 'AND' and 'XOR' gates.




(a) (b)

Fig. 12: (a) the structure of second flip-flop. (b) the structure of first and third flip-flop.

*C. Circuit Design*

The second step in the flowchart is the minimization of the circuit dimensions. To achieve this goal, the following modifications have been performed: 1- the wires routings have been changed. 2- three layers are selected for the circuit. 3- the vertical wire of the first and third T flip-flops has been diminished by one cell. The schematic of the circuit is illustrated in Fig. 13. As shown, one of the wires is taken to another layer and then returns to the original layer. Thus, two wires cross without affecting each other. In brief, the proposed circuit has the following modifications compared to the circuit in [13]:

1- We have replaced the crossover in prior work with the multi-layer crossover.

2- The circuit of the T flip-flop is redesigned and optimized as described in Fig. 12.

3- The wires routings have been changed to decrease the number of vertical and horizontal cells of the counter.

4- The outputs of 'AND' gates are connected directly to the 'XOR' gates which reduce one cell in each XOR gate.

These modifications lead to the area reduction aim of our research, so that the circuit cells number is reduced to 96 cells. Also, by the modifications in the T flip-flop circuit, the delay is reduced to one clock cycle.

## Simulation Results and Discussion

We have implemented "QCA Designer" tool to design the proposed counter. This tool has two simulation engines, which are "Coherence Vector" and "Bistable Approximation". In this research, the Coherence Vector engine is utilized and its parameters are depicted in Fig. 14.

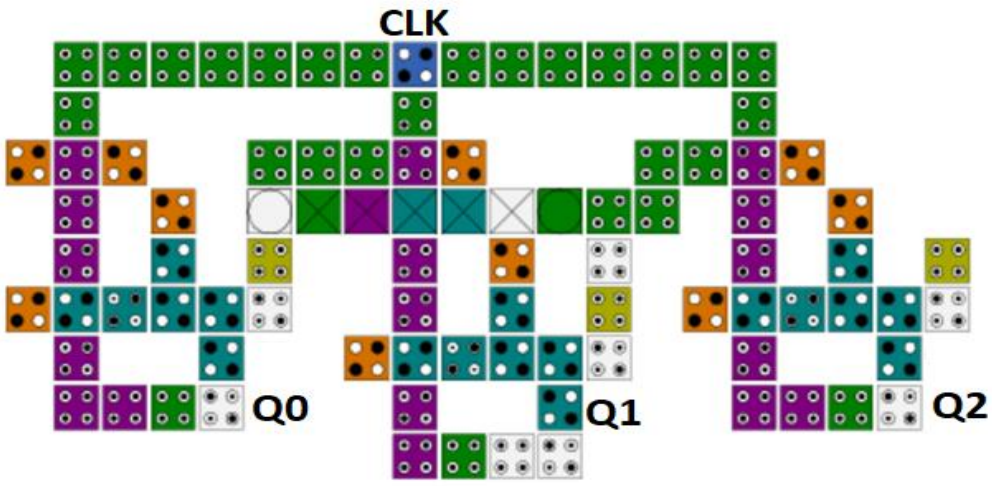



Fig. 13: The structure of proposed multilayer 3-bits counter.

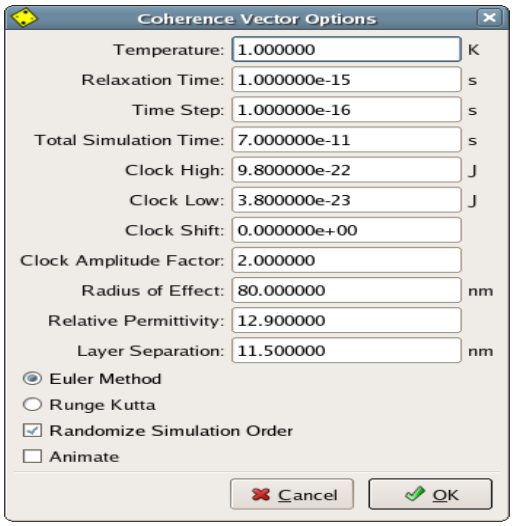



Fig. 14: The simulation parameters of coherence vector engine in QCA Designer tool.

The simulation waveforms of the proposed counter are represented in Fig. 15.

As seen, the numbers are counted properly and the circuit works correctly.

Fig. 16 shows the cells number of the proposed design in comparison with the previous designs. As depicted, the circuit contains 96 cells which is lowest among the others. The area of our circuit and the prior circuits are drawn in Fig. 17.

The occupied area of the proposed design is 0.08 $\mu m^2$, which is the least occupied area.

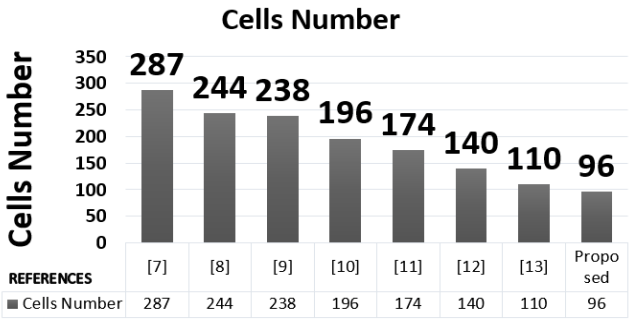



Fig. 16: The comparison of the cells number.

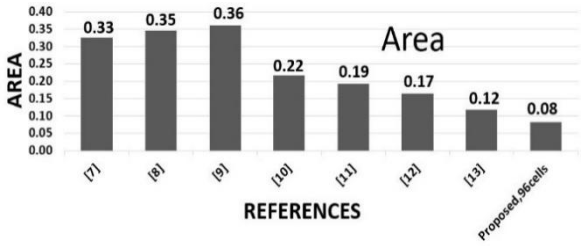



Fig. 17: Area occupied of the proposed design and previous studies.

The circuit delay is calculated by the number of clock cycles that the input signal takes time to reach to its output. The delay of our circuit is depicted in Fig. 18. As seen by the colors of the cells, the path from 'CLK' signal to the 'Q2' has experienced four consecutive phases of the clock which is equal to one clock cycle. As expected, the simulation of the proposed circuit shows that the delay is 1 clock cycle. The curve in Fig. 19 represents the delays of various designs.

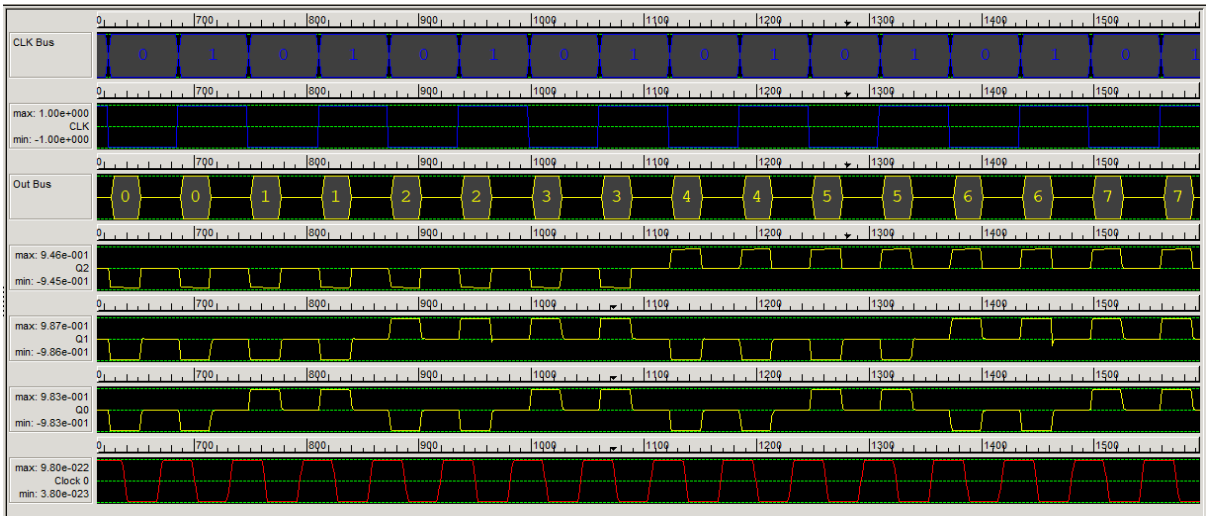



Fig. 15: Simulation results of 3-bit multilayer counter with 96 cells.

Table 1: Simulation results and comparison with the priors

| parameters | [7] | [8] | [9] | [10] | [11] | [12] | [13] | Proposed 96 Cells | our circuit improvement compare to [13] |
|---|---|---|---|---|---|---|---|---|---|
| Cell Count | 287 | 244 | 238 | 196 | 174 | 140 | 110 | 96 | 12.72% |
| Cell/Bit | 95.67 | 81.33 | 79.33 | 65.33 | 58 | 46.67 | 36 | 32 | 11.11% |
| layers number | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 3 | ---- |
| Length Covered | 778 | 958 | 858 | 638 | 438 | 458 | 458 | 418 | 8.73% |
| Width Covered | 418 | 358 | 418 | 338 | 438 | 358 | 238 | 198 | 16.81% |
| Net Area | 92988 | 79056 | 77112 | 63504 | 56376 | 45360 | 35640 | 31104 | 12.73% |
| Total Area | 325204 | 342946 | 358644 | 215644 | 191844 | 165600 | 109004 | 82764 | 24.07% |
| Area | 0.33 | 0.35 | 0.36 | 0.22 | 0.19 | 0.17 | 0.11 | 0.08 | 27.27% |
| Area/Bit | 0.11 | 0.12 | 0.12 | 0.07 | 0.06 | 0.06 | 0.04 | 0.03 | 25% |
| Wasted Area | 819 | 816 | 903 | 544 | 484 | 414 | 276 | 210 | 23.91% |
| Latency or delay | 2 | 4.25 | 2.25 | 2 | 3 | 2 | 1.5 | 1 | 33.33% |
| Cost | 348 | 885 | 855 | 688 | 324 | 196 | 81 | 37 | 54.32% |

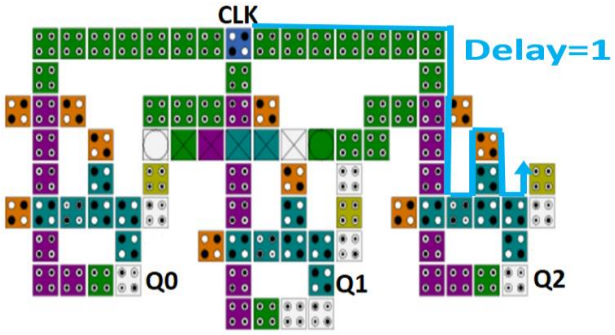



Fig. 18: The path from 'CLK' to the output 'Q2'.

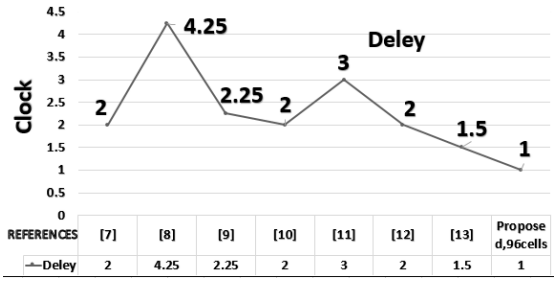



Fig. 19: The comparison of delay.

Table 1 shows all the parameters of the proposed design and the previous studies. The work in [13] has better parameters compared to the others, and therefore, our circuit has been compared to it. As seen, the delay has improved by 33.33%. The cells number decrement is 12.72% and the area reduction is 27.27%. A QCA specific cost function estimation is proposed in [24] that takes into account the number of logic gates and crossings wires in cost evaluation.

Since our circuit is multi-layer, we implement this function for the evaluation of cost metric:

$$Cost = (M^2 + I + C^2) \times T^2 \quad (1)$$

where ($T$) shows the circuit delay, ($M$) represent the number of majority gates, ($I$) is the number of inverters and ($C$) is the number if crossovers. As the number of layers and consequently, the number of crossovers increases, we expect the cost to be incremented. However, as there is only one crossover in the circuit and the delay is decreased to one clock cycle, the circuit cost has been reduced by 54.32%.

The circuit Net area is calculated by multiplication of the cells number and the area of one cell. The Net area is decreased by 12.73%.

Net area = cells number × area of one cell (2)

The circuit total area is calculated as represented in (3). It is seen that the total area is reduced by 24.07%.

Total Area = Width Covered×Length Covered (3)

Width Covered=(Vertical cells number×20nm)–2 (4)

Length Covered=(horizontal cells number×20nm)–2 (5)

To calculate the energy consumption of the circuit, "QCA Designer-E" tool is employed. This tool analyses "average energy dissipation" and "total energy dissipation" and represents the results in an output log text. The energies comparison of the proposed circuit and the priors are illustrated in Table 2. As seen, both the total energy dissipation and the average energy dissipation per clock cycle have been improved by 13%.

Table 2: The results of the energy dissipation in the proposed circuit

| Reference | Total energy dissipation | Average energy dissipation | our circuit improvement |
|---|---|---|---|
| [7] | 8.66E-02 | 7.87E-03 | 68% |
| [8] | 7.53E-02 | 6.84E-03 | 63% |
| [9] | 6.63E-02 | 6.03E-03 | 58% |
| [10] | 5.87E-02 | 5.34E-03 | 53% |
| [11] | 3.39E-02 | 3.08E-03 | 18% |
| [12] | 3.73E-02 | 3.39E-03 | 26% |
| [13] | 3.18E-02 | 2.89E-03 | 13% |
| **Proposed circuit** | 2.75E-02 | 2.50E-03 | ---------- |

### *A. Circuit Stability and Reliability*

Temperature Stability Factor (TSF) is a parameter that calculates the reliability and accuracy of the circuit. The TSF indicates the temperature range in which the circuit operates correctly. The temperature variations can disrupt the circuit operation and make it unstable. The TSF is determined by the minimum and maximum polarizations in the circuit simulation [25], [26]. The TSF simulation is performed by changing "Temperature option (k)" parameter of the coherence vector engine in the "QCA Designer" tool. Table 3 illustrates the TSF analysis of the proposed circuit. As seen, it is stable from k=1 to k=6 which is similar to the TSF of [13]. The TSF of [12] is from k=1 to k=4 which is lower than our design. Fig. 20 represents the TSF(Min) and TSF(Max) of the proposed circuit. It shows that after k=6, all curves are diverged from each other and the circuit operates incorrectly.

### *B. Fault Tolerance Analysis*

Displacement faults are usual in the QCA cell production. Therefore, it needs to be attended in the QCA circuit design [27], [28]. The Defects can occur in the individual cells production or by the movement of cells to a surface [29]-[30]. To evaluate the fault tolerance, each cell should move separately in 5 directions which are vertical (up and down), horizontal (right and left) and 45-degrees rotation. Also, the cell missing is considered in the simulation. The segmented design of the counter is illustrated in Fig. 21. Tables 4 & 5 show the fault tolerance simulation for all cells of the circuit. Some cells such as C13R4 and C15R3 are critical and their movement to horizontal right direction make the circuit unstable. Also, there are a number of cells such as C6R6 that their movement range in all directions are wide.

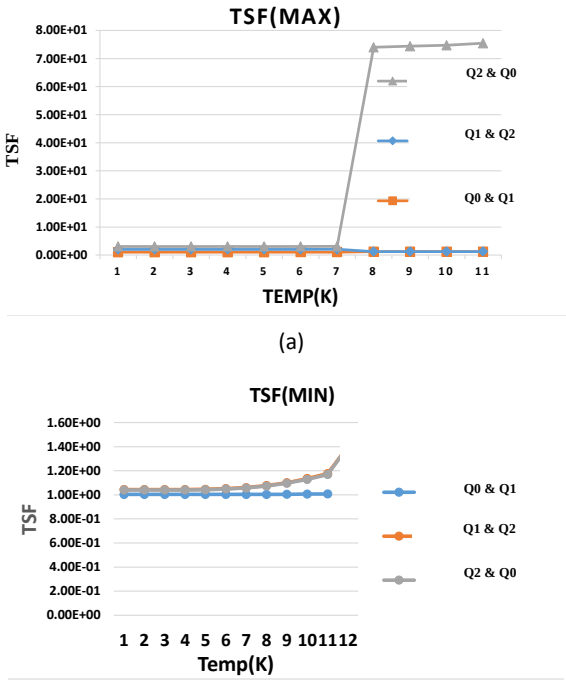



Fig. 20: Temperature Stability Factor (a) TSF(Max) (b) TSF(Min).

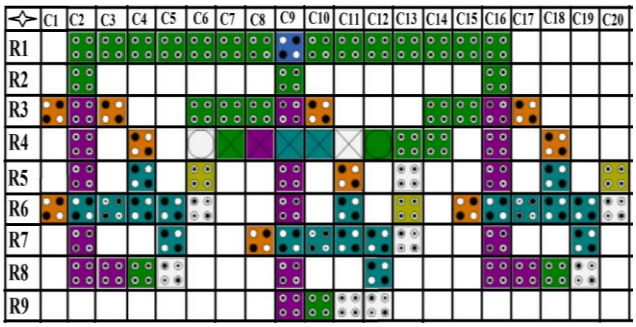



Fig. 21: Segmented design of the three bits counter.

Table 3: Temperature stability factor for output of the counter

| Temp (k) | TEMPERATURE STABILITY (MIN & MAX) FOR-three-bits counter with 96 cells | | | | | | state |
|---|---|---|---|---|---|---|---|
| | Q0&Q1 | | Q1&Q2 | | Q2&Q0 | | |
| | TSF (MAX) | TSF (MIN) | TSF (MAX) | TSF (MIN) | TSF (MAX) | TSF (MIN) | |
| **1** | 1.00 | 1.00 | 1.04 | 1.04 | 1.04 | 1.04 | **stable** |
| **2** | 1.00 | 1.00 | 1.04 | 1.04 | 1.04 | 1.04 | **stable** |
| **3** | 1.00 | 1.00 | 1.04 | 1.04 | 1.04 | 1.04 | **stable** |
| **4** | 1.00 | 1.00 | 1.04 | 1.04 | 1.04 | 1.04 | **stable** |
| **5** | 1.00 | 1.00 | 1.05 | 1.05 | 1.04 | 1.04 | **stable** |
| **6** | 1.00 | 1.00 | 1.05 | 1.05 | 1.05 | 1.05 | **stable** |
| **7** | 1.00 | 1.00 | 1.06 | 1.06 | 1.05 | 1.06 | **unstable** |
| **8** | 0.0169 | 1.00 | 1.23 | 1.08 | 72.7 | 1.07 | **unstable** |
| **9** | 0.0168 | 1.00 | 1.23 | 1.10 | 73.1 | 1.10 | **unstable** |
| **10** | 0.0168 | 1.01 | 1.23 | 1.14 | 73.5 | 1.13 | **unstable** |

For the majority of cells, the rotation by 45 degree and cell missing make the circuit unstable. The exceptions are for a few numbers of cells such as C1R3, C3R3 and etc. Generally, we can not conclude exactly that the output is fluctuation free, because a few numbers of cells are critical and their movement can make the circuit unstable.

On the opposite side, there are several cells that can be displaced more than 1.5nm. So, it depends deeply to the fabrication process accuracy and its fault percentage. However, from the calculated values in Tables 4 & 5, we can summarize that about 70% of the cells are allowed to be displaced by 1.5nm or more.

Table 4: Fault tolerance analysis (C1 to C9)

| Name of Cells | Horiz. Left (nm) | Horiz. Right (nm) | Vertic. Up (nm) | Vertic. Down (nm) | Rotate (45 DEG) | Missing Cell |
|---|---|---|---|---|---|---|
| C1R3 | stable | 2.5 | 7.8 | 5.4 | stable | stable |
| C1R6 | 0.5 | 2.2 | 2.2 | 2.2 | unstable | unstable |
| C2R1 | 5.7 | 2.5 | 5.5 | 3.6 | unstable | unstable |
| C2R2 | 5.1 | 4.3 | 3.6 | 4.7 | unstable | unstable |
| C2R3 | 1.7 | 1.4 | 4.8 | 6.8 | unstable | unstable |
| C2R4 | 4.6 | 4.1 | 2.8 | 5.1 | unstable | unstable |
| C2R5 | 4.2 | 1.5 | 1.6 | 0.6 | unstable | unstable |
| C2R6 | 0.3 | 0.6 | 0.2 | 0.4 | unstable | unstable |
| C2R7 | 3.8 | 1 | 0.6 | 0.9 | unstable | unstable |
| C2R8 | 2.6 | 3.5 | 3.8 | 1.1 | unstable | unstable |
| C3R1 | 2.5 | 3.4 | stable | 5.6 | stable | stable |
| C3R3 | 2.3 | 34 | 7.7 | 7.2 | stable | stable |
| C3R6 | 3 | 0.7 | 1 | 0.4 | unstable | unstable |
| C3R8 | 2.8 | 5.1 | 3.6 | 3.9 | unstable | unstable |
| C4R1 | 2.5 | 5.6 | stable | stable | unstable | unstable |
| C4R4 | 3.8 | 3.8 | 1.6 | 0.4 | unstable | unstable |
| C4R5 | 2.3 | 1.7 | 1.2 | 0.2 | unstable | unstable |
| C4R6 | 0.8 | 0.1 | 0.1 | 0.5 | unstable | unstable |
| C4R8 | 1.1 | 5.8 | 2.7 | 2.8 | unstable | unstable |
| C5R1 | 5.5 | 6.6 | 5.6 | 5.5 | unstable | unstable |
| C5R6 | 0.6 | 3.8 | 1.9 | 1.5 | unstable | unstable |
| C5R7 | 3.7 | 2.5 | 2.8 | 4.1 | unstable | unstable |
| C5R8 | 6.2 | 0.9 | 3.9 | 1.2 | unstable | unstable |
| C6R1 | 6 | 6.8 | 5.4 | 5.6 | unstable | unstable |
| C6R3 | 1.6 | 6.1 | 1.7 | 4.4 | unstable | unstable |
| C6R4-L1 | 3.8 | 2.7 | 4.4 | 2.2 | unstable | unstable |
| C6R4-L2 | 6.8 | 6.7 | 6.6 | 5.1 | unstable | unstable |
| C6R4-L3 | stable | 3.9 | stable | stable | stable | stable |
| C6R5 | 1.8 | 4.1 | 1.6 | 6.6 | unstable | unstable |
| C6R6 | 5 | stable | 5.8 | stable | unstable | unstable |
| C7R1 | 6.7 | 7.2 | 6.2 | 6.3 | unstable | unstable |
| C7R3 | 6.6 | 1.3 | 5.8 | 3.7 | unstable | unstable |
| C7R4-L3 | 3 | 6.1 | 3.5 | 4.4 | unstable | unstable |
| C8R1 | 6.8 | 14.6 | 6.9 | 6.3 | unstable | unstable |
| C8R3 | 3.6 | 2.8 | 5.4 | 3.3 | unstable | unstable |
| C8R4-L3 | 5.8 | 6.7 | 3 | 2.8 | unstable | unstable |
| C8R7 | 0.6 | 2.2 | 2.4 | 2.4 | unstable | unstable |
| C9R1 | 5.1 | 5.1 | 3.4 | 5.8 | unstable | unstable |
| C9R2 | 3.7 | 3.8 | 8.4 | 1.9 | unstable | unstable |
| C9R3 | 1.7 | 1.3 | 1 | 5.6 | unstable | unstable |
| C9R4-L1 | 3.5 | 5.2 | 7 | 2.2 | unstable | unstable |
| C9R4-L3 | 7.1 | 6.8 | 4.4 | 4.5 | unstable | unstable |
| C9R5 | 4.5 | 4.6 | 2.7 | 2.2 | unstable | unstable |
| C9R6 | 4.2 | 1.2 | 1.2 | 0.9 | unstable | unstable |
| C9R7 | 0.4 | 0.6 | 0.2 | 0.3 | unstable | unstable |
| C9R8 | 4 | 1.1 | 0.5 | 1 | unstable | unstable |
| C9R9 | 1.5 | 4 | 3.9 | 1 | unstable | unstable |

Table 5: Fault tolerance analysis (C10 to C20)

| Name of Cells | Horiz. Left (nm) | Horiz. Right (nm) | Vertic. Up (nm) | Vertic. Down (nm) | Rotate (45 DEG) | Missing Cell |
|---|---|---|---|---|---|---|
| C10R1 | 9.5 | 6.8 | 4.8 | 4.5 | unstable | unstable |
| C10R3 | 2.2 | 3.5 | 5.3 | 3.3 | unstable | unstable |
| C10R4-L3 | 6.7 | 6.1 | 3.5 | 3.4 | unstable | unstable |
| C10R7 | 3.4 | 0.7 | 0.7 | 0.5 | unstable | unstable |
| C10R9 | 6.8 | 5 | 2.7 | 2.6 | unstable | unstable |
| C11R1 | 6.2 | 6.7 | 3.5 | 3.5 | unstable | unstable |
| C11R4-L3 | 0.4 | 6.8 | 1.9 | 1.6 | unstable | unstable |
| C11R5 | 3.8 | 0.8 | 1.1 | 0.5 | unstable | unstable |
| C11R6 | 2.2 | 1.7 | 1.1 | 0.2 | unstable | unstable |
| C11R7 | 0.9 | 0.2 | 0.1 | 0.5 | unstable | unstable |
| C11R9 | 5.3 | 6.5 | 3.8 | 3.8 | unstable | unstable |
| C12R1 | 6.8 | 6.6 | 2.1 | 4.1 | unstable | unstable |
| C12R4-L1 | 1.5 | 0.1 | 3.6 | 2.8 | unstable | unstable |
| C12R4-L2 | 1 | 2.5 | 1.8 | 2.6 | unstable | unstable |
| C12R4-L3 | 6.2 | 0.2 | 1.4 | 0.9 | unstable | unstable |
| C12R7 | 0.7 | 3.4 | 3.5 | 3.1 | unstable | unstable |
| C12R8 | 6.9 | 5.7 | 2.2 | 4.4 | stable | stable |
| C12R9 | 6.3 | 6 | 4.1 | 5.9 | unstable | unstable |
| C13R1 | 6 | 0.6 | 1.1 | 4.4 | unstable | unstable |
| C13R4 | 0.1 | 0 | 0.2 | 0 | unstable | unstable |
| C13R5 | 0.1 | 0.8 | 1.6 | 3.7 | unstable | unstable |
| C13R6 | 3.7 | 1.5 | 2.5 | 1.3 | unstable | unstable |
| C13R7 | 4.8 | 2.9 | 5.9 | 2.4 | unstable | unstable |
| C14R1 | 6.6 | 1 | 4.4 | 0.6 | unstable | unstable |
| C14R3 | 0.05 | 0.1 | 0.1 | 0 | unstable | unstable |
| C14R4 | 0 | 0.1 | 0 | 0 | unstable | unstable |
| C15R1 | 0.3 | 1.9 | 4.7 | 0.7 | unstable | unstable |
| C15R3 | 0.2 | 0 | 0.5 | 0.2 | unstable | unstable |
| C15R6 | 0.5 | 2.2 | 2.2 | 2.2 | unstable | unstable |
| C16R1 | 2.3 | 0.4 | 0.1 | 0.9 | unstable | unstable |
| C16R2 | 1.5 | 0.1 | 1.3 | 0.1 | unstable | unstable |
| C16R3 | 1 | 0.3 | 0.1 | 1.8 | unstable | unstable |
| C16R4 | 1.6 | 2.4 | 3 | 2.7 | unstable | unstable |
| C16R5 | 4.1 | 1.4 | 1.6 | 0.8 | unstable | unstable |
| C16R6 | 0.3 | 0.6 | 0.2 | 0.4 | unstable | unstable |
| C16R7 | 3.8 | 1 | 0.5 | 0.9 | unstable | unstable |
| C16R8 | 2.6 | 3.5 | 3.8 | 1.1 | unstable | unstable |
| C17R3 | 0.3 | 0 | 1.1 | 0.4 | unstable | unstable |
| C17R6 | 2.9 | 0.7 | 0.9 | 0.4 | unstable | unstable |
| C17R8 | 6.8 | 5 | 3.6 | 3.8 | unstable | unstable |
| C18R4 | 5.2 | 5.4 | 3.8 | 0.4 | stable | unstable |
| C18R5 | 4 | 4 | 4 | 0.2 | unstable | unstable |
| C18R6 | 0.8 | 0.1 | 0.1 | 0.5 | unstable | unstable |
| C18R8 | 1.2 | 5.8 | 2.7 | 2.8 | unstable | unstable |
| C19R6 | 0.6 | 3.8 | 4 | 1.3 | unstable | unstable |
| C19R7 | 3.8 | 2.6 | 2.9 | 4 | unstable | unstable |
| C19R8 | 6.2 | 0.9 | 3.9 | 1.3 | unstable | unstable |
| C20R5 | 4.3 | 5.7 | 4.5 | 6.6 | unstable | unstable |
| C20R6 | 5.1 | 4.7 | 6 | 3.1 | unstable | unstable |

## Conclusion

A three-bits QCA counter utilizing T flip-flop with 96 cells was introduced in this research. The circuit designed in three layers and its outputs are three bits. The design methodology was introduced and our design flowchart was explained. The counter components were drawn in a block diagram and each component explained with details. The whole circuit along with its routing and clocking methods were illustrated and the modifications were defined. The modifications contain two parts which were T flip-flops improvement and circuit dimensions reduction. These modifications were performed to minimize the circuit delay and to make the circuit as a high-speed counter. The simulation waveforms of the circuit proved the design accuracy. The simulation results depicted that the proposed circuit has been improved in delay, area and energy dissipations compared to the previous designs. So that the terms of cells number, area and delay were improved by 12.72%, 27.27%, and 33.33%, respectively compared to [13]. Also, the total energy dissipation and the average energy dissipation showed 13% improvement. The circuit temperature stability and fault tolerance of the circuit was analyzed. The temperature analysis illustrated that the circuit temperature stability was similar to the previous circuit and it was not decreased. The fault tolerance simulation represented that about 70% of the cells can be displaced by 1.5 nm or more. We can say somehow that the fault tolerance is dependent to the fabrication process and it is a weakness for the proposed circuit.

## Author Contributions

G. Asadi-Ghiasvand designed the experiments. G. Asadi-Ghiasvand, M. Zare and M. Mahdavi collected and carried out the data analysis. G.Asadi-Ghiasvand and M. Zare interpreted the results and wrote the manuscript.

## Acknowledgment

The author would like to thank the Shahr-e-Qods Branch, Islamic Azad University, that sponsored this research.

## Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the ethical issues including plagiarism, informed consent, misconduct, data fabrication and, or falsification, double publication and, or submission, and redundancy have been completely witnessed by the authors.

## Abbreviations

| | |
|---|---|
| *CMOS* | Complementary Metal Oxide Semiconductor |
| *QCA* | Quantum-dot Cellular Automata |
| *P* | Polarization |
| *CLK* | Clock |
| *T* | Circuit delay |
| *M* | Number of majority gates |
| *I* | Number of inverters |
| *C* | Number if crossovers |
| *TSF* | Temperature Stability Factor |
| *k* | Temperature parameter in QCA-Designer |

## References

[1] K. Jeong, A. B. Kahng, “A power-constrained MPU roadmap for the International Technology Roadmap for Semiconductors (ITRS),” in Proc. 2009 international SoC Design Conference (ISOCC), 2009.

[2] R. Chakrabarty, D. Kumar Mahato, A. Banerjee, S. Choudhuri, M. Dey, N. K. Mandal, "A novel design of flip-flop circuits using quantum dot cellular automata (QCA)," in Proc. 2018 IEEE 8th Annual Computing and Communication Workshop and Conference (CCWC): 408-414, 2018.

[3] H. Cho, E. E. Swartzlander, “Adder and multiplier design in quantum-dot cellular automata,” IEEE Trans. Comput., 58(6): 721-727, 2009.

[4] M. A. Dehkordi, A. S. Shamsabadi, B. S. Ghahfarokhi, A. Vafaei, “Novel RAM cell designs based on inherent capabilities of quantum-dot cellular automata,” Microelectron. J., 42(5): 701-708, 2011.

[5] M. N. Asfestani, S. R. Heikalabad, “A novel multiplexer-based structure for random access memory cell in quantum-dot cellular automata,” Phys. B: Condens. Matter, 521: 162-167, 2017.

[6] C. S. Lent, P. D. Tougaw, W. Porod, G. H. Bernstein, “Quantum cellular automata,” Nanotechnology, 4(1): 49-57, 1993.

[7] S. Angizi, S. Sayedsalehi, A. Roohi, N. Bagherzadeh, K. Navi, "Design and verification of new n-bit quantum-dot synchronous counters using majority function-based JK flip-flops," J. Circuits Syst. Comput., 24(10): 1550153, 2015.

[8] K. S. Bhavani, V. Alinvinisha, "Utilization of QCA based T flip flop to design Counters," in Proc. 2015 International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS): 1-6, 2015.

[9] S. Angizi, M. H. Moaiyeri, S. Farrokhi, K. Navi, N. Bagherzadeh, "Designing quantum-dot cellular automata counters with energy consumption analysis," Microprocess. Microsyst., 39(7): 512-520, 2015.

[10] M. Abutaleb, “Robust and efficient quantum-dot cellular automata synchronous counters,” Microelectron. J., 61: 6-14, March. 2017.

[11] Z. Amirzadeh, M. Gholami, “Counters designs with minimum number of cells and area in the quantum-dot cellular automata technology,” Int. J. Theor. Phys., 58: 1758-1775, 2019.

[12] A. H. Majeed, E. Alkaldy, M. S. bin Zainal, D. Bin MD Nor, “Synchronous counter design using novel level sensitive T-FF in QCA technology,” J. Low Power Electron. Appl., 9(3): 27, 2019.

[13] J. Mohammadi, M. Zare, M. Molaei, M. Maadani, "Low-cost three-bit counter design in quantum-dot cellular automata technology," IETE J. Res., 2022.

[14] C. S. Lent, P. D. Tougaw, “Lines of interacting quantum-dot cells: A binary wire,” J. Appl. Phys., 74(10): 6227-6233, 1993.

[15] F. Lombardi, J. Huang, "Design and test of digital circuits by quantum-dot cellular automata," Artech House, Inc., Electronic ISBN:9781596932685, 2007.

[16] P. D. Tougaw, C. S. Lent, "Logical devices implemented using quantum cellular automata," J. Appl. Phys., 75(3): 1818-1825, 1994.

[17] C. S. Lent, P. D. Tougaw, "A device architecture for computing with quantum dots," Proc. IEEE, 85(4): 541-557, 1997.

[18] B. Sen, M. Dalui, B. K. Sikdar, "Introducing universal qca logic gate for synthesizing symmetric functions with minimum wire crossings," in Proc. ICWET: 828–833, 2010.

[19] G. Schulhof, Konrad, G. A. Jullien, "Simulation of random cell displacements in qca," J. Emerg. Technol. Comput. Syst., 3(1), 2007.

[20] K. Walus, G. Schulhof, G. A. Jullien, "High level exploration of Quantum-Dot Cellular Automata (QCA)," in Proc. 38th Asilomar Conference on Signals, Systems and Computers: 30–33, 2004.

[21] A. Gin, P. D. Tougaw, S. Williams, "An alternative geometry for quantum-dot cellular automata," J. Appl. Phys., 85(12): 8281–8286, 1999.

[22] I. L. Bajec, P. Pecar, "Two-layer synchronized ternary quantum-dot cellular automata wire crossings," Nanotechnol., 7: 368–376, 2012.

[23] B. Sen, A. Nag, A. De, B. K. Sikdar, "Multilayer Design of QCA Multiplexercellular," in Proc. 2013 Annual IEEE India Conference (INDICON), 2013.

[24] W. Liu, L. Liang, M. O'Neill, E. Swartzlander, "A first step towards cost functions for quantum-dot cellular automata designs," IEEE Trans. Nanotechnol., 13(3): 476-487, 2014.

[25] S. S. Roy, "Fault tolerance and temperature stability: the dynamic error estimation in quantum-dot cellular automata," in proc. 2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS): 84-89, 2017.

[26] D. Bhowmik, J. Pal, M. Chandra, A. K. Saha, N. Kumar, "QCA based design of cost-efficient code converter with temperature stability and energy efficiency analysis," Mater. Today Proc., 49(8): 3585-3594 , 2022.

[27] B. Sen, A. Nag, A. De, B. K. Sikdar, "Towards the hierarchical design of multilayer QCA logic circuit," J. Comput. Sci., 11: 233-244, 2005.

[28] J. Pal, S. Bhattacharjee, A. K. Saha, P. Dutta , " Study on temperature stability and fault tolerance of adder in quantum-dot cellular automata," in Proc. 5th IEEE International Conference on Signal Processing, Computing and Control (ISPCC 2k19), 2019.

[29] M. Momenzadeh, H. Jing, M. B. Tahoori, F. Lombardi, "Characterization, test, and logic synthesis of and-or-inverter (AOI) gate design for QCA implementation," IEEE Trans. Comput. Aided Des. Integr. Circuits Syst., 24 (2005): 1881-1893, 2005.

[30] A. Roohi, R. F. DeMara, N. Khoshavi, "Design and evaluation of an ultra-area-efficient fault-tolerant QCA full adder," Microelectron. J., 46(6): 531-542, 2015.

## Biographies

**Ghodratollah Asadi Ghiasvand** received his B.Sc. in Telecommunication Engineering, transmission trend from Ghiaseddin Jamshid Kashani university, Abyek, Iran in 2011 and his M.Sc. in Telecommunication systems trend from Islamic Azad university، Department of Electrical Engineering, Shahr-e-Qods Branch, Tehran, Iran, 2022. He has been working in the radio department of Infrastructure Communications Company since 2012, He is currently an expert in the data department of Infrastructure Communications Company and interests in digital circuit design and telecommunication system design.


- Email: telecom.engineer.asadi@gmail.com
- ORCID: 0009-0003-7959-4496
- Web of Science Researcher ID: JLM-1309-2023
- Scopus Author ID: NA
- Homepage: NA


**Mahdi Zare** received his B.Sc. and M.Sc. degrees in Electrical Engineering from South Tehran Branch, Islamic Azad University, Tehran, Iran, in 2001 and 2004, respectively. He received his Ph.D. degree in Electronic Engineering at the Tehran Science and Research Branch, Islamic Azad University. He worked as senior hardware engineer in Rayaphone Co. since 2004. He is currently the faculty member of Shahr-e-Qods branch, Islamic Azad University. His research interests include performance and area optimization in latency-insensitive systems, multi-core synchronization, and Mixed signals circuit design. He has published several scientific papers and has acted as a reviewer in several international journals and conferences.


- Email: zare@qodsiau.ac.ir, d.mehdi.zare@gmail.com
- ORCID: 0000-0002-9797-0083
- Web of Science Researcher ID: AAO-1254-2021
- Scopus Author ID: 57129066700
- Homepage: NA


**Mojdeh Mahdavi** received the Ph.D. degree in Electronics from Islamic Azad University, Science and Research Branch, Tehran, Iran, in 2010. In 2006, she joined the Electrical Engineering Department as an Assistant Professor at Islamic Azad University, Shahr-e-Qods Branch, Tehran, Iran. Her current research interests include digital system design and implementation, nanotechnology and fault tolerant design.


- Email: mahdavi.qodsiau@gmail.com
- ORCID: 0000-0001-8774-2426
- Web of Science Researcher ID: NA
- Scopus Author ID: AAO-1261-2021
- Homepage: NA


**How to cite this paper:**
G. Asadi Ghiasvand, M. Zare, M. Mahdavi, "A new high-speed multi-layer three-bits counter design in quantum-dot cellular automata technology" J. Electr. Comput. Eng. Innovations, 12(1): 235-246, 2024.

**DOI:** 10.22061/jecei.2023.9955.667

**URL:** https://jecei.sru.ac.ir/article_1999.html