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Research paper

A Fast and Accurate Yield Optimization Method for Designing Operational Amplifier Using Multi-Objective Evolutionary Algorithm Based on Decomposition

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Abstract

Background and Objectives: In recent years, the electronics industry has experienced rapid expansion, leading to increased concerns surrounding the expenses associated with designing and sizing integrated circuits. The reliability of these circuits has emerged as a critical factor influencing the success of production. Consequently, the necessity for optimization algorithms to enhance circuit yield has become increasingly important. This article introduces an enhanced approach for optimizing analog circuits through the utilization of a Multi-Objective Evolutionary Algorithm based on Decomposition (MOEA/D) and includes a thorough evaluation. The main goal of this methodology is to improve both the speed and precision of yield calculations.
Methods: The proposed approach includes generating initial designs with desired characteristics in the critical analysis phase. Following this, designs that exceed a predefined yield threshold are replaced with the initial population that has lower yield values, generated using the classical MOEA/D algorithm. This replacement process results in notable improvements in yield efficiency and computational speed compared to alternative Monte Carlo-based methods.
Results: To validate the effectiveness of the presented approach, some circuit simulations were conducted on a two-stage class-AB Op-Amp in 180 nm CMOS technology. With a high yield value of 99.72%, the approach demonstrates its ability to provide a high-speed and high-accuracy computational solution using only one evolutionary algorithm. Additionally, the observation that modifying the initial population can improve the convergence speed and yield value further enhances the efficiency of the technique. These findings, backed by the simulation results, validate the efficiency and effectiveness of the proposed approach in optimizing the performance of the Op-Amp circuit.
Conclusion: This paper presents an enhanced approach for analog circuit optimization using MOEA/D. By incorporating critical analysis, it generates initial designs with desired characteristics, improving yield calculation efficiency. Designs exceeding a preset yield threshold are replaced with lower yield ones from the initial population, resulting in enhanced computational speed and accuracy compared to other Monte Carlo-based methods. Simulation results for a two-stage class-AB Op-Amp in 180 nm CMOS technology show a yield of 99.72%, highlighting the method's effectiveness in achieving high speed and accuracy with a single evolutionary algorithm.

Introduction

With the continuous development of the electronics industry in recent decades, there has been a growing concern regarding the cost associated with designing and sizing integrated circuits. Consequently, the yield value of these circuits has garnered significant attention. Yield is defined as the proportion of products that satisfy all

design constraints to the total number produced [1]-[3], and plays a crucial role in determining the overall success of circuit production. Therefore, the development of optimization algorithms that effectively enhance the yield value has become of utmost importance. The process of yield optimization typically encompasses several key steps, as shown in Fig. 1 [4]. These steps involve specifying design variables while considering desired constraints, generating initial designs using dedicated design tools based on the defined specifications, evaluating the yield value of the designs through simulation tools, iterating if the desired yield value is not achieved, and considering the optimization process complete once the desired yield value is attained.

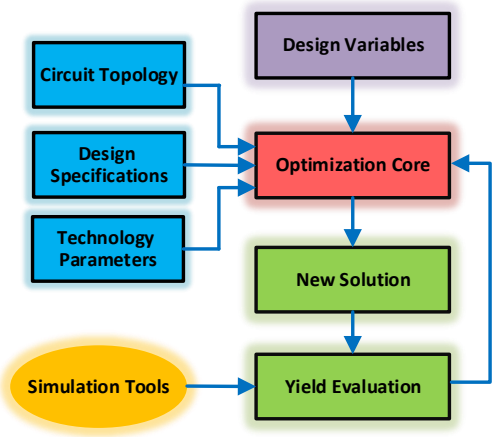


Fig. 1: General flowchart for yield optimization.

In general, yield optimization methods can be broadly categorized into two main categories [5]: statistical methods, such as Monte Carlo (MC) based methods and response-surface-based (RSB) methods, and non-statistical methods, including corner-based methods and performance-specific worst-case design (PSWCD) methods. Non-statistical methods offer advantages such as a lower number of simulations, simplicity, and faster sensitivity analysis. However, they have weaknesses such as design overhead at corner points and lower accuracy in estimation [5]. On the other hand, statistical methods provide good accuracy in calculating yield value and perform better at corner points compared to non-statistical methods. However, their main weakness lies in the large number of simulations required, which can be time-consuming [5].

Typically, yield optimization methods aim to maximize the yield value while minimizing computational time. Recent efforts have been made to optimize yield using evolutionary algorithms, which have shown promising results in increasing yield [6]-[9]. Additionally, some new methods have been proposed for yield estimation using machine learning instead of SPICE simulations including the work presented in [10]. However, it is important to note that this technique may not apply to all types of circuits, as in this method, numerous designs are generated from a circuit, and then a machine learning algorithm is trained using these designs. Therefore, when faced with other circuits that have not been trained by the algorithm, this method may not provide suitable responses.

The MC method is widely acknowledged as the most precise and commonly used approach for simulations. However, it does have a significant drawback, which is the extensive number of simulation iterations required, resulting in longer optimization process times. To address this challenge, various methods have been proposed to improve the efficiency of MC-based techniques. Examples of such methods include Latin Hypercube Sampling (LHS) [11] and Quasi MC simulation (QMC) [12]. The primary objective of speeding up MC simulations is to reduce the computational budget while maintaining yield accuracy. Therefore, yield optimization algorithms need to fulfill the following conditions: reducing the number of simulations, minimizing computational steps, and improving overall efficiency.

In this work, a combination of critical analysis and a Multi-Objective Evolutionary Algorithm [6], [13] based on Decomposition (MOEA/D) [14]-[15] is introduced. Indeed, to improve the efficiency of the optimization process, the conventional MOEA/D framework has been adapted by integrating critical analysis. This integration of critical analysis into the MOEA/D framework results in reduced simulation time and increased efficiency. The use of critical analysis helps to identify critical solutions that have a significant impact on yield improvement, while non-critical solutions are separated. To refine the simulation process further, this paper additionally utilizes the integration of optimal computing budget allocation (OCBA) [6] alongside critical analysis. This strategy controls the number of simulations needed for each design, thereby minimizing the simulation budget. As a result, the entire optimization process is accelerated. Pole-Zero analysis is also conducted to assess the stability of the circuit. Furthermore, this study considers a broader range of design characteristics compared to existing methods. In summary, the contributions of this work can be summarized as follows: enhancement of the classical MOEA/D method through the combination of critical analysis and MOEA/D, improvement of the yield value by replacing designs generated in both critical analysis and classical MOEA/D, acceleration of the yield calculation by reducing computational steps, and inclusion of circuit stability analysis and consideration of additional design characteristics.

The remainder of this paper is structured as follows. Initially, the background knowledge pertinent to this

study will be discussed in detail. Next, the specifics of the proposed method will be explored. This will be followed by an examination of the simulation results derived from the experiments. To wrap up, the key findings of the research presented will be summarized.

Background Knowledge of the Presented Technique

Since the proposed approach for yield optimization in this work is established based on OCBA, Multi-Objective Optimization (MOO), and MC simulation, these techniques are briefly reviewed in the following sub-sections. It should be noted that in the process of yield optimization, the goal is to identify a point that maximizes the yield value [5]. Therefore, the formula for calculating the yield can be expressed as follows:

$$d^* = \arg_{d \in D} \max\{Y(d)\} \quad (1)$$

where d is the design parameters such as transistor's dimensions, resistor and capacitor values, bias voltages, and current values. For each design parameter, an acceptable range of variations (upper and lower bands) is selected. The selection of this range of acceptable values is dependent on design knowledge, technological processes, or user preferences. In (1), the design space denoted by D. d^* represents the optimal point within the design space D that leads to maximizing the yield value. It is important to note that maximizing the yield is not always the goal; in some cases, the opposite is pursued, and the objective is to minimize the yield value (e.g., chip area in the case of yield-aware sizing). Accordingly:

$$Y(d) = E\{YS(d, s, \theta) \mid pdf(s)\} \quad (2)$$

where E is the expected value, θ indicates the environmental variables, and s represents the space of statistical parameters. In the case where all specifications are satisfied, $\mathrm{YS(d, s, \theta)}$ is set to 1, but if not, $\mathrm{YS(d, s, \theta)}$ is set to 0.

Optimal Computing Budget Allocation

The OCBA is one of the popular methods for ranking and selection in optimization methods [16]. In this method, the necessary number of iterations for each design is intelligently allocated based on the calculated mean value and variance for the designs. This enables a substantial reduction in the simulation budget by judiciously assigning simulation iterations to each design. With OCBA, the subsequent simulation step aims to identify the best solution by maximizing the likelihood of its discovery.

Multi-Objective Optimization

In the MOO technique, unlike single-objective optimization, multiple objective functions are employed to attain more accurate optimal solutions [17]. Consequently, in MOO, a set of solutions is obtained based on predefined objective functions. The optimization of multi-objective analog circuits is grounded in the use of multi-objective evolutionary algorithms (MOEAs). The MOO equation is given by:

$$\begin{aligned} &\text{Min/max } f_1(x), f_2(x), \ldots, f_n(x) \\ &\text{Subject to: } x \in U \end{aligned} \quad (3)$$

where the number of objective functions indicated by n , U is a set of feasible solutions, in this case, and $f_n(x)$ represents nth objective function. There are two types of object operations: min/max and x represents the solution. The proposed approach uses the MOEA/D multi-objective algorithm, which is discussed later.

Monte-Carlo Simulation

MC simulation delineates the process of translating uncertainties from a model's input to uncertainties in its output [6]-[9]. By employing statistical sampling, the MC method offers approximations for quantitative problems, facilitating an explicit and quantitative simulation of uncertainty. In MC simulation, inputs are designated as probability distributions, allowing for a clear representation of uncertainty. The predictability of system performance becomes uncertain when the inputs describing a system are uncertain. The outcome of any analysis involving inputs represented by probability distributions is likewise presented as a probability distribution. Typically, more than 1000 simulations are executed in the MC method, with each run referred to as a realization. Each realization involves sampling the distribution of each uncertain parameter, and selecting a random value for each parameter. Subsequently, specific input parameters are employed to simulate the system over time. This simulation yields performance metrics for the system. Ultimately, the system will traverse a potential path, and outputs are presented in the form of probability distributions.

Presented Method

After brief introduction of MC simulation, OCBA, and MOO technique, the presented method is described in this section. Fig. 2 shows the flowchart of the proposed method, which uses improved MOEA/D for yield optimization. Referred to Fig. 2, the combination of MOEA/D and critical analysis is employed to improve the classical MOEA/D and each is described separately here.

Critical Analysis

As previously mentioned, the MC method stands out as one of the most widely used techniques for calculating yield. Nevertheless, a significant challenge associated with this method is the extensive number of simulations, which can lead to system slowdown.

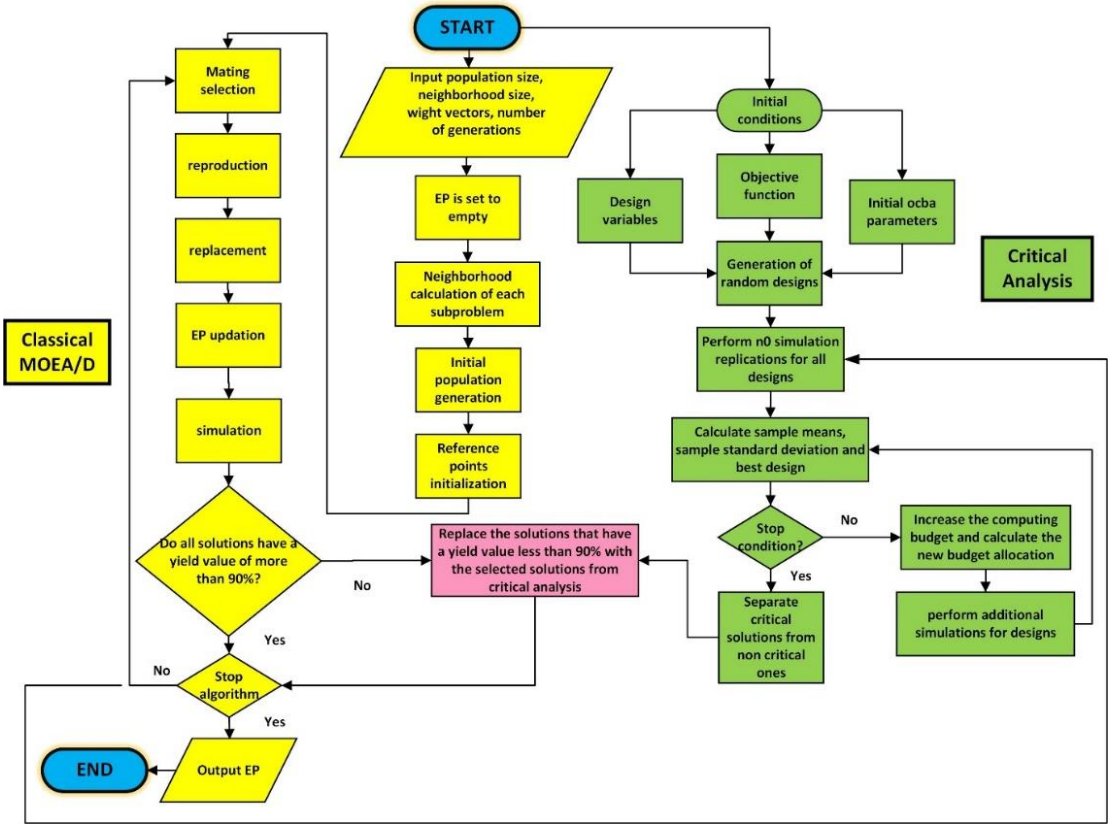


Fig. 2: Flowchart of the proposed approach for yield optimization.

A proposed solution to expedite the MC method involves reducing or eliminating simulation iterations assigned to non-critical solutions [6]. Critical solutions refer to designs that have a substantial impact on increasing the yield value, while non-critical solutions have a lesser effect on this calculation. Accordingly, the OCBA technique is employed to identify critical and non-critical solutions, intelligently allocating an appropriate number of simulation iterations to each [18], [19]. Consequently, this method of budget allocation between solutions leads to a reduction in computational time. The utilization of OCBA also contributes to a decrease in the yield estimator's variance. As a result, more simulation iterations are directed toward critical solutions, minimizing the time spent on non-critical ones. The details of this approach are outlined in Algorithm 1 [6].

Based on algorithm 1, T , K and b are the total budget of simulations, the number of competing designs and the best design, respectively. The variance and mean of the k solutions indicated by σ_i^2 , J_i . Every candidate solution runs n_0 simulations initially. N_i and N_j are the number of simulation replications allocated to design i , j respectively and $\delta_{b,i} = J_b - J_i$.

Multi-Objective Evolutionary Algorithm based on Decomposition

The MOEA/D [20], [21], developed by Jang in 2007, decomposes a multi-objective problem into multiple subproblems and optimizes them concurrently. This method combines the objective functions using a weight vector defined for each subproblem. Each individual in the population represents a solution obtained through an aggregation vector, with the population size matching the number of problems, so each solution corresponds to a member of the population. By the end of the search, each problem yields a Pareto-front answer, which is the best solution discovered for the respective subproblem constituting the population in each generation. The proximity between aggregation vectors establishes neighbor relations among sub-problems. During the search, a neighborhood member plays a role in contributing to the solution of the problem, marking this stage as the collaboration stage. For each subproblem following the current one in the neighborhood, a weighted aggregation vector is provided. If the solutions to the neighbors' problems surpass the original answers, these should replace the initial answers, constituting the competition stage. The processes of cooperation and competition are applied to all sub-problems, ensuring a continuous exchange of information between neighbors.

The subproblems within its neighborhood are leveraged to optimize each subproblem in the algorithm. The general framework of the MOEA/D can be considered as follows:

Algorithm 1. Critical Analysis

Initializing design variables and specifying a reasonable range for each of the design specifications.

Initializing $K, \mathrm{T}, \mathrm{n}_0, \Delta$ and let $l \leftarrow 0$. Then performing n_0 simulation replications for all designs.

$$N_1^l = N_2^l = \ldots = N_k^l = n_0$$

Calculate sample means and standard deviation, then finding the best design according to $b = \arg\min_i (J_i)$.

Construct solution set by critical solutions.

If the termination condition is satisfied, then, end the algorithm. Otherwise, increase the computing budget by Δ and calculate the new budget allocation.

$N_1^{l+1}, N_2^{1+1}, \ldots, N_k^{l+1}$

$$\frac{N_i}{N_j} = \left(\frac{\sigma_i / \delta_{b,i}}{\sigma_j / \delta_{b,j}} \right)^2$$

$$N_b = \sigma_b \sqrt{\sum_{i=1, i \neq b}^{k} \frac{N_i^2}{\sigma_i^2}}$$

$i, j \in \{1, 2, \ldots, k\}$ *and* $i \neq j \neq b$

Perform additional $\max(N_i^{l+1} - N_i^l, 0)$ simulations for the design i, $i = 1, 2, \ldots, k; l \leftarrow l + 1$

Go to step 3

$$\begin{aligned} &\text{Minimize}\,(f_1(x), f_2(x), \ldots, f_m(x)) \\ &\text{Subject to}\, g(x) \geq 0, X_L < x < X_H \end{aligned} \tag{4}$$

A given objective function is called fi(x), i = 1...m, m is the number of objectives, and x is the design variable. There are X_L and X_H for the lower and upper bounds, respectively. The vector g(x) ≥ 0 represents the design constraints.

Each non-dominated solution to the multi-objective optimization problem aligns with an optimal single-objective solution when utilizing a specific weight vector. Within MOEA/D, distinct weight vectors guide diverse searches across various regions of the objective space, forming a comprehensive set of weight vectors. In the context of a multi-objective optimization problem, the Tchebycheff method allows for the definition of N subproblems. In this method, the objective function of the jth (j=1, 2, ..., N) sub-problem is as follows:

$$g^{te}(x \mid \lambda^j, z^*) = \max_{1 \leq i \leq m} \left\{ \lambda_i^j \mid f_i(x) - z_i^* \mid \right\} \tag{5}$$

where $\lambda^j = \left(\lambda_1^j, \ldots, \lambda_m^j \right)^T$ demonstrates a weight vector, $z^* = (z_1^*, \ldots, z_m^*)^T$ represents the vector of reference points. For each Pareto optimal point x* there exists a weight vector so that x* is the optimal solution of (5). There are related references such as the work presented in [15] that describe methods for determining the weight vector. There are Pareto optimal solutions to the problem of (4) for each solution of (5). Some methods [14], [20] have pointed to the weakness of the MOEA/D when facing more complex circuits and a higher number of objectives in comparison with the NSGA-II. However, others [12], [21] have emphasized the capability of the MOEA/D in multi-objective optimization problems. Given this, the main goal of the proposed method in this article is to enhance the convergence speed of the algorithm while upholding a high level of accuracy. This goal is achieved through an effective integration of the critical analysis method and the MOEA/D algorithm. The comparison of the yield histogram between the proposed method and the classic MOEA/D, serves as evidence of the method's efficacy. Furthermore, in contrast to the CSNM [6] employing the NSGA-III, the proposed method, by integrating solution responses, demonstrates both remarkable speed and accuracy, as will be expounded upon in the upcoming simulation results section. It is essential to note that alternative methods, such as epsilon constraint methods or lexicographical methods, can also be considered valuable techniques for objective weighting.

The critical analysis section begins by generating a set of designs aiming to optimize the desired specifications, which serve as the objectives. These objectives include DC voltage gain, unity-gain bandwidth (UGBW), phase margin, common-mode rejection ratio (CMRR), total harmonic distortion (THD), output voltage swing, slew rate (SR), and power dissipation. Additionally, the stability of each solution is assessed through pole-zero analysis. The design variables governing the solutions encompass capacitor capacitance, transistor dimensions, the number of parallel transistors, and bias voltages. The designer selects the initial population size, the number of subproblems, the maximum iteration limit to conclude the algorithm, and values associated with critical analysis

parameters. In the multi-objective optimization algorithm, the goals involve the simultaneous minimization of THD and power consumption, while maximizing other specified objectives. It should be noted that as illustrated in Fig. 3, design parameters often trade off against each other, turning the design process into a multi-dimensional optimization. Successfully navigating these challenges requires a combination of intuition and experience to reach an acceptable compromise [22]. It seems that having too many objectives in an optimization problem hinders a multi-objective algorithm's ability to improve them simultaneously, especially if they all are correlated. Therefore, it may be beneficial to remove objectives that are of lesser importance in amplifier design. However, to achieve a highly effective design that excels in all aspects, it is crucial to consider all important objectives. In this particular design, parameters such as input resistance, output resistance, and noise were not included in the optimization problem to address the aforementioned issue.

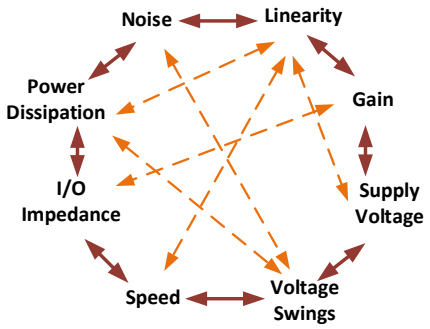


Fig. 3: Analog design octagon [22].

In this work, the optimization procedure begins by using critical analysis and OCBA to identify designs that meet the desired specifications. Concurrently, a decomposition-based optimization algorithm generates the initial population. A comparative analysis is then conducted to evaluate the production yield of the population generated by MOEA/D against that found through critical analysis. Solutions identified through critical analysis that exhibit higher yield values than those in the MOEA/D production population are subsequently substituted. At this stage, the population formed is anticipated to contain more optimal solutions than the initial production population. This iterative substitution process continues until the algorithm's stopping criteria are met. Specifically, the stopping criterion for the critical analysis phase is achieved when the cumulative number of simulations assigned to the designs meets or exceeds the total computational budget. Meanwhile, the termination criterion for the MOEA/D algorithm is reached when the predefined maximum number of iterations, set at the algorithm's inception, is attained.

It is important to note that if designs with yield values below the designer's desired threshold are replaced and the stop conditions are not met, these solutions will be redirected to the critical analysis section for reassessment of simulations. Through these iterations, the process helps generate a more optimal set of solutions in this phase. Conversely, if the designs produced in the MOEA/D section have yield values exceeding the desired threshold, there is no need for replacement, and the critical analysis step can be skipped. This approach not only accelerates computational speed but also improves production efficiency by preserving solutions generated in the MOEA/D stage during previous iterations.

Simulation Results

The proposed algorithm is tested on a two-stage class-AB Operational Amplifier (Op-Amp) shown in Fig. 4 [23] in a standard 0.18µm CMOS technology with a supply voltage of 1.8V. For performing MC simulations and evaluation of circuit performance parameters, MATLAB R2020 and Synopsys HSPICE are used, respectively. It should be noted that Op-Amp proposed in [23] is a fully differential two-stage amplifier employing a positive feedback technique and split-length transistors to increase the DC voltage gain without affecting the UGBW, stability, power dissipation, and output voltage swing compared to the conventional two-stage Op-Amp. A comprehensive analysis of the Op-Amp shown in Fig. 4 is provided in [23]. In Fig. 4, the first stage is a folded-cascade and the second stage is a common-source amplifier. Transistor pairs of $M_{16\text{-}19}$ and $M_{20\text{-}23}$ are used to build split-length transistors and by applying the output signal V_{out+} to the drain terminal of M_{22} and V_{out-} to the drain terminal of M_{18}, a positive feedback loop is created.

Fig. 5 illustrates the MATLAB-HSPICE link, which is employed for implementing the algorithm presented in this work. In this process, the user defines the design variables and circuit specifications in MATLAB. MATLAB then prepares the circuit netlist parameters and initiates the simulation of the circuit using HSPICE. Following the HSPICE circuit simulation, MATLAB scans the output file generated by HSPICE and extracts various metrics of the simulated circuit, such as SR, CMRR, and output voltage swing. This step involves MATLAB analyzing the simulation results and making adjustments to the circuit parameters in the subsequent iteration if the desired values for the output parameters are not achieved.

Table 1 shows the desired specifications for the Op-Amp shown in Fig. 4. The compensation capacitance, bias voltages, transistor dimensions, as well as parallel transistor count are the design variables in this work. According to the utilized technology file, the transistor's width ranges from 0.54µm to 100µm and their length can range from 0.18µm to 20µm. Moreover, the compensation capacitance which is utilized for stability concerns is set to be from 0.1pF to 10pF.

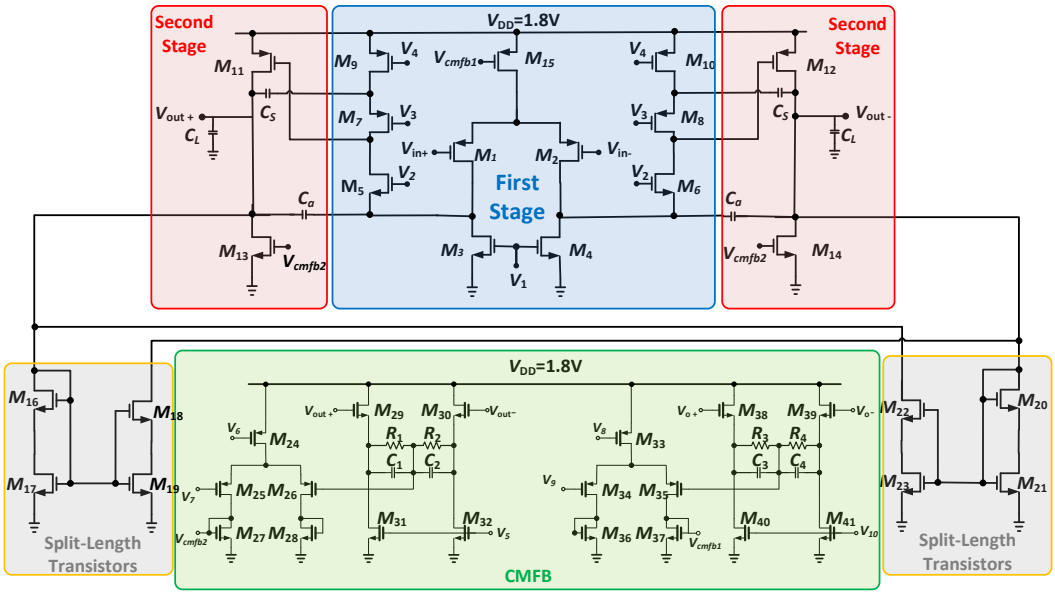


Fig. 4: Circuit schematic of the utilized two-stage class AB-OP-Amp [23].

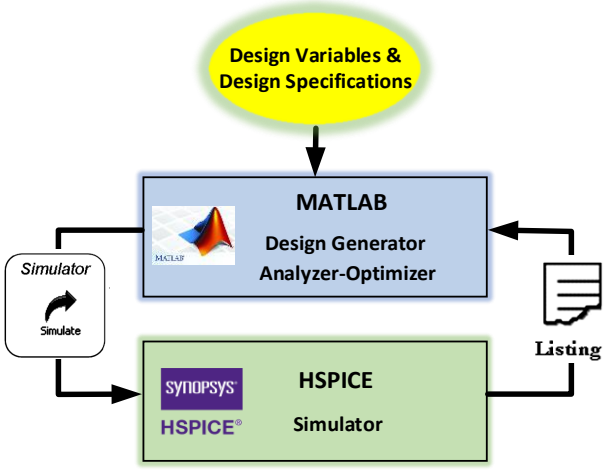


Fig. 5: Utilized MATLAB-HSPICE link.

Table 1: Desired specifications of the two-stage class AB-OP-Amp

Specifications	Desired value
DC Voltage Gain (dB)	80≥
Phase Margin (deg)	60°≤ PM≤ 80°
Power Dissipation (mW)	≤ 10
Slew Rate (V/µs)	600≥
Unity-Gain Bandwidth (MHz)	300≥
Common Mode Rejection Ratio (dB)	90≥
Power Supply Rejection Ratio (dB)	60≥
Output Voltage Swing (V)	2.5≥
Bandwidth (KHz)	1≥
Total Harmonic Distortion (dB)	≤ -30
Pole-Zero Analyze	Pole: Z=a+bj, Re(Z) < 0

In the presented work, critical analysis should be initiated by creating some random designs, based on the design specifications and design variables mentioned above. Next, critical analysis is used to select designs that comply with the design constraints. All the settings related to the critical analysis method are done exactly as the [24], [25], where n_0 is set to be 5 and $\Delta = 5$. Moreover, T is determined by:

$$T = M_1 \times sim_{ave} \tag{6}$$

where sim_{ave} represents the average budget for each candidate and M_1 denotes the number of critical solutions, which are set to be 50 and 100, respectively.

In the next step, random solutions are generated by the MOEA/D algorithm. Then, the necessary simulations are performed to evaluate the desired goals. The number of MOEA/D population is equal to 100 and also the maximum number of iterations to reach appropriate goals is equal to 100. Alternative critical analysis solutions with a yield value higher than 90% are substituted for solutions with yield values less than 90% in the set of the current MOEA/D population. If the set of solutions generated in the critical analysis section does not have a sufficient number of solutions with a yield value greater than the designer's desired value, solutions with a yield value greater than the solutions generated by the MOEA/D algorithm are replaced. At the end, the stop condition is checked and if the stop condition is not satisfied, the cycle of production and replacement of solutions will continue.

As mentioned above, after the replacement of the design produced in the MOEA/D section with a yield value of less than 90%, if the stop conditions are not met, this set of solutions will be sent to the critical analysis section

to reassign simulations to these designs. It is obvious that if the solutions created in the MOEA/D section have a yield value greater than the desired yield value by the designer, there is no need to replace the solutions. At this condition, the critical analysis step is removed at the next iteration. By replacing the selected solutions between two steps, the calculation speed and the yield value calculation accuracy will be increased.

Obtained from a presented algorithm, the values of the passive components, bias voltages, and transistors dimensions used in the two-stage class-AB Op-Amp can be found in Table 2.

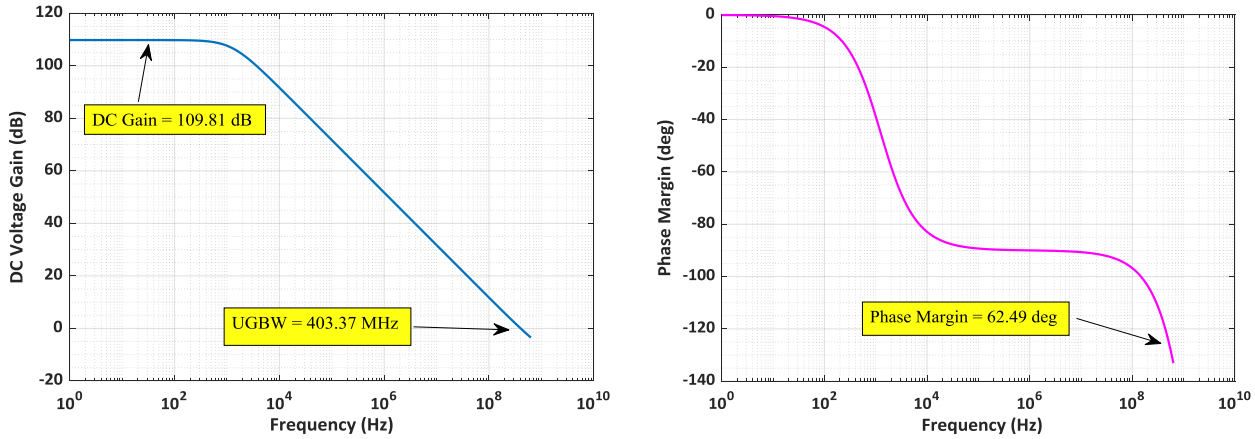
Moreover, Table 3 provides the simulation results for the DC gain, UGBW, phase margin, power dissipation, output voltage swing, CMRR, Power Supply Rejection Ratio (PSRR), amplifier Bandwidth (BW), THD, and SR of the designed two-stage class-AB Op-Amp in different process and temperature corners. As stated in Table 3, the simulation results for the two-stage class-AB Op-Amp indicate the following values: DC gain of 109.81dB, UGBW of 403.37MHz, phase margin of 62.49°, power dissipation of 7.94mW, output voltage swing of 3.4V, CMRR of 148.56dB, PSRR of 61.41dB, BW of 1.26 kHz, THD of -42.14dB, and SR of 667.93 V/µs. Fig. 6 illustrates the open-loop frequency responses of the two-stage class AB Op-Amp that has been designed using the values specified in Table 2. It's crucial to emphasize that the simulation results illustrated in Table 3 align with the expected outcomes. Additionally, Fig. 7, Fig. 8, and Fig. 9 show the plots for CMRR, PSRR, and output voltage swing of the designed Op-Amp, respectively. According to Fig. 10(a), the designed two-stage class-AB Op-Amp is utilized as a unity gain capacitor buffer to measure its slew rate [23], [26]. In this configuration, a square wave with 1Vpp amplitude and a frequency of 5 MHz was applied to the circuit, and the result is given in Fig. 10(b). The measured slew rate value of the two-stage class-AB Op-Amp is 667.93 V/µs.

Table 2: One solution of a two-stage class-AB Op-Amp (Fig. 4) based on transistor dimensions and passive components

Parameter	Value	Parameter	Value
$(W/L)_{1,2}$	$2\times 22.92\,\mu m/0.18\mu m$	$(W/L)_{38,39}$	$1\times 20.25\mu m/0.18\mu m$
$(W/L)_{3,4}$	$3\times 25.17\,\mu m/0.18\mu m$	$(W/L)_{40,41}$	$1\times 20.88\mu m/0.18\mu m$
$(W/L)_{5,6}$	$1\times 35.68\,\mu m/0.18\mu m$	C_s	$1.05pF$
$(W/L)_{7,8}$	$4\times 44.44\,\mu m/0.18\mu m$	C_L	$1pF$
$(W/L)_{9,10}$	$2\times 90.5\,\mu m/0.18\mu m$	C_a	$1pF$
$(W/L)_{11,12}$	$4\times 43.51\,\mu m/0.36\mu m$	$C_{1,2,3,4}$	$1.5\,pF$
$(W/L)_{13,14}$	$1\times 59.01\,\mu m/0.36\mu m$	$R_{1,2,3,4}$	$20K\Omega$
$(W/L)_{15}$	$5\times 29.4\,\mu m/0.18\mu m$	V_1	$0.6V$
$(W/L)_{16,17,20,21}$	$1\times 2\mu m/0.18\mu m$	V_2	$1V$
$(W/L)_{18,19,22,23}$	$1\times 2.58\mu m/0.18\mu m$	V_3	$0.77V$
$(W/L)_{24}$	$1\times 40.5\mu m/0.18\mu m$	V_4	$1.2V$
$(W/L)_{25,26}$	$1\times 22.03\mu m/0.18\mu m$	V_5	$0.685V$
$(W/L)_{27,28}$	$1\times 38.11\mu m/0.18\mu m$	V_6	$1.14V$
$(W/L)_{29,30}$	$2\times 10.43\mu m/0.18\mu m$	V_7	$0.276V$
$(W/L)_{31,32}$	$1\times 19.6\mu m/0.18\mu m$	V_8	$1.2V$
$(W/L)_{33}$	$1\times 44.2\mu m/0.18\mu m$	V_9	$0.5V$
$(W/L)_{34,35}$	$1\times 19.7\mu m/0.18\mu m$	V_{10}	$0.59V$
$(W/L)_{36,37}$	$1\times 4.37\mu m/0.18\mu m$		

Table 3: Specifications of the two-stage class-AB Op-Amp

Specifications	temperature corners		
	TT (27°C)	FF (-40°C)	SS (90°C)
DC-Gain (dB)	109.81	87	96.4
Phase Margin (°)	62.49	61.14	62.11
Power Dissipation (mW)	7.94	9.1	7.34
Slew Rate (V/µs)	667.93	843.87	575.1
UGBW (MHz)	403.37	511.6	321.65
CMRR (dB)	148.56	127.1	136.89
Output Swing (V)	3.4	3.4	3.4
THD (dB)	-42.14	-40.5	-41.9
PSRR (dB)	61.41	59.7	60
BW (KHz)	1.26	1.07	1.19



(a) (b)

Fig. 6: Frequency response of the two-stage class-AB Op-Amp: a) magnitude, b) phase.

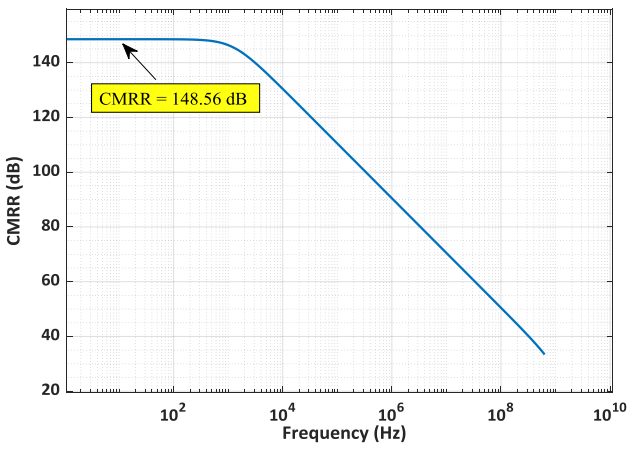


Fig. 7: CMRR behavior of the simulated two-stage class-AB Op-Amp.

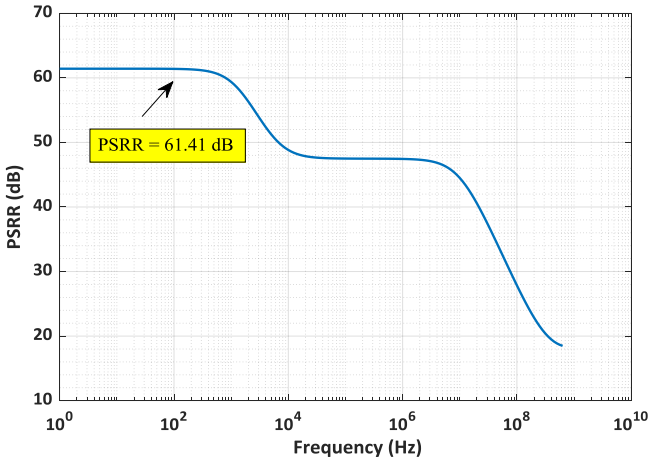


Fig. 8: PSRR behavior of the simulated two-stage class-AB Op-Amp.

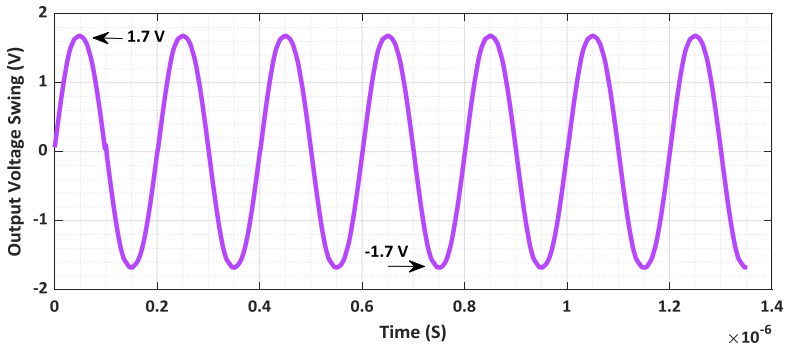
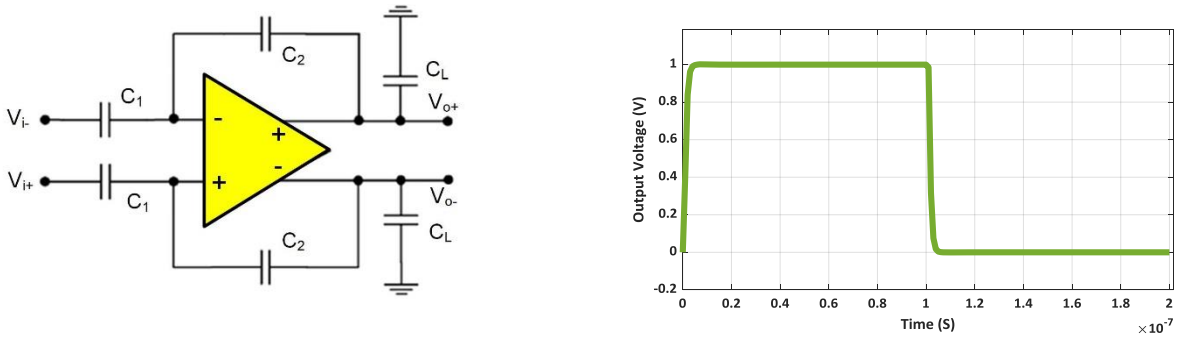
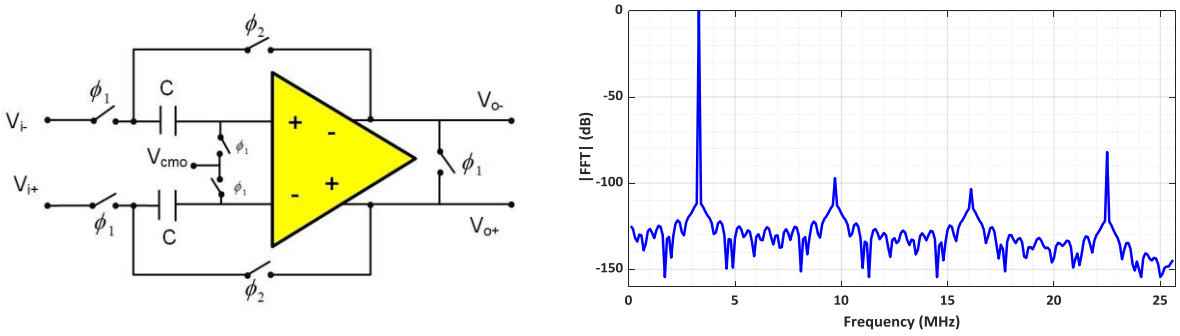


Fig. 9: Output Swing of the two-stage class-AB Op-Amp.



(a) (b)

Fig. 10: (a) Circuit schematic of a unity gain capacitive buffer [23], [26], (b) Op-amps large signal step responses.



(a) (b)

Fig. 11: (a) Circuit schematic of designed flip-around sample-and-hold [27], [28], (b) FFT plot of the output of the designed sample-and-hold.

Moreover, the designed two-stage class-AB Op-Amp in this work is used in a switched-capacitor flip-around sample-and-hold (SH) circuit shown in Fig. 11(a) [27], [28] to study its linearity in a closed-loop configuration. Fig. 11(b) depicts the circuit-level simulation outcome of the output voltage spectrum, showcasing the large signal transient response of the circuit to a 1Vpp input step voltage with two non-overlapping clocks at a frequency of 3.125MHz. According to the performed simulations, the output spectrum of the SHA shows a THD of -42.14dB.

The stability of the designed two-stage class-AB Op-Amp is thoroughly examined and verified through the implementation of Pole-Zero analysis, a powerful technique used to assess the system's stability characteristics. By analyzing the Pole-Zero plot, which is visually depicted in Fig. 12, valuable insight into the location and behavior of the poles and zeros of the Op-Amp's transfer function has been gained. This comprehensive analysis ensures that the Op-Amp operates within stable and desirable parameters, guaranteeing reliable and accurate performance in various applications.

To attain a more precise yield simulation, this study conducted the MC simulation with 2000 replications, as indicated by the values presented in Table 2. Fig. 13(a) shows a histogram of yields. According to Fig. 13(a), the

mean value for yield is 99.72%, with a standard deviation of 0.03%. In Fig. 13(b), a histogram of yields for the classic MOEA/D algorithm is depicted. According to Fig. 13(b), the mean value for yield is 89.95%, with a standard deviation of 0.03%. By comparing the two Figs, it is evident that in the proposed method, which combines critical analysis and MOEA/D, not only higher accuracy is achieved but also the issue of objective aggregation present in classic MOEA/D [14], [20] has been addressed.

To assess the effectiveness of the proposed method, the CSNM [6], Freeze-Thaw Bayesian optimization [30], and Mirzaei [7] algorithms were evaluated on the circuit shown in Fig. 4. To have a more accurate comparison between the methods examined, all of these methods have been implemented by the authors and the simulations performed on a workstation equipped with a CPU: Intel Core i7-4790K @4GHz, 16GB RAM, and a 64-bit operating system with an x64-based processor. The improved MOEA/D algorithm used in the proposed approach demonstrated faster performance compared to the other three algorithms, as shown in Table 4. Additionally, the proposed approach required fewer computational steps compared to the other three methods.

Based on these findings, it can be concluded that when combined with critical analysis, the proposed method can decrease the number of simulations needed for solutions with minimal effects on yield. Furthermore, replacing critical analysis with MOEA/D solutions can significantly enhance efficiency and reduce simulation time. However, it is worth noting that the CSNM, which utilizes OCBA, critical analysis, and two evolutionary algorithms, achieved a higher yield value compared to the proposed approach. So, the proposed approach, compared to three other existing methods, demonstrates lower complexity, fewer steps, and reduced computational time.

In Fig. 14, two diagrams related to the Pareto-front evaluation of the generated solutions (phase margin versus voltage gain, and UGBW versus voltage gain) are reported. As shown in Fig. 14(a) and according to Table 1, a voltage gain value greater than 80 dB and a phase margin range between 60 to 80 degrees are obtained. Also, the simulation results for the plot of UGBW versus voltage gain also comply with the conditions stated in Table 1. It should be noted that based on what is observable in Fig. 14, the simulation results show more scattering in regions with a voltage gain of around 110 dB, a phase margin of 63 degrees, and an UGBW of 400 MHz.

Table 4: Yield simulation results and the run time for different techniques applying to the two-stage class-AB Op-Amp of Fig. 4

Technique	Best	Worst	Mean	Run time (h)	Computer
Freeze–Thaw Bayesian [30]	99.24	99.13	99.23	19	CPU Intel Core i7-4790K @4GHz with 16GB RAM
CSNM [6]	99.97	98.77	99.87	20	
Mirzaei method [7]	99.11	98.91	99.01	22	
Proposed Method	99.82	99.62	99.72	16	

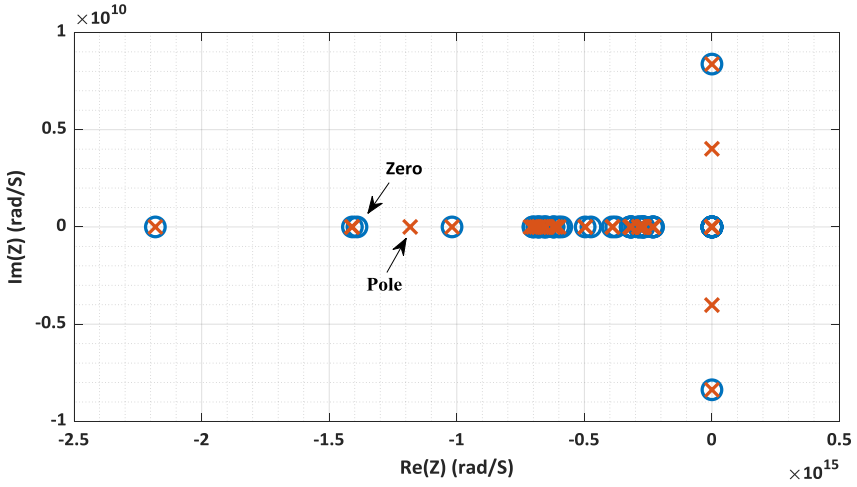
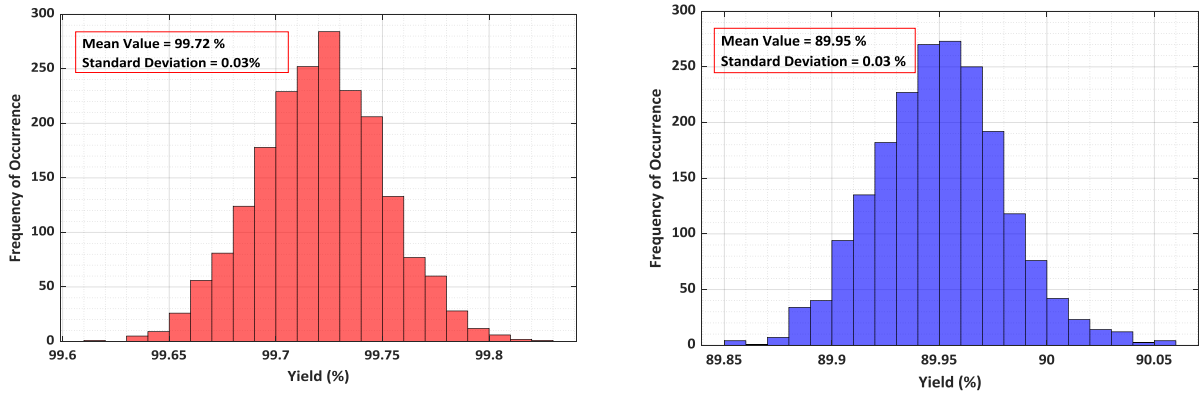
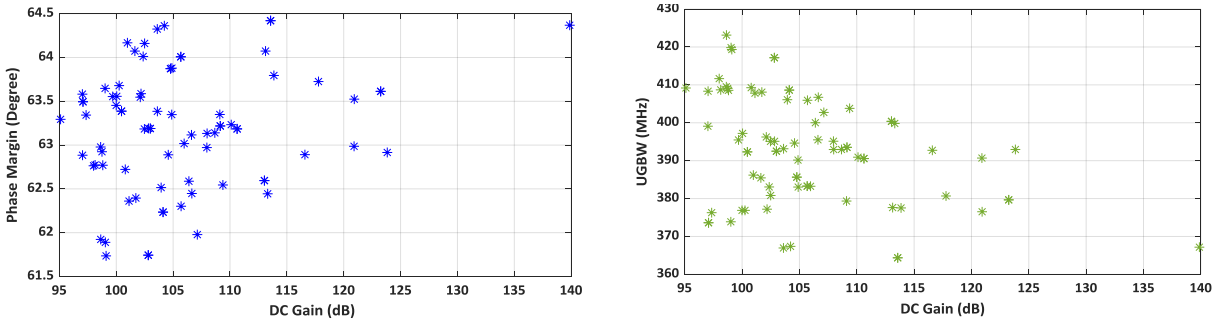


Fig. 12: Pole-Zero plot of the designed Op-Amp.



(a) (b)

Fig. 13: The yield histogram for the MC simulation with 2000 iterations of the utilized Op-Amp, (a) Propose approach, (b) Classic MOEA/D.



(a) (b)

Fig. 14: Pareto front of the generated solutions, (a) DC gain versus Phase Margin, (b) DC gain versus UGBS.

Conclusion

In this paper, an enhanced approach for MOEA/D based on Decomposition, utilizing critical analysis is presented to enhance the computational speed and accuracy of yield calculation in analog circuit optimization. The critical analysis generates initial designs with desired characteristics. Subsequently, designs surpassing a predefined yield threshold are replaced with the initial population having lower yield values, which is generated using the classical MOEA/D. This approach significantly improves yield efficiency and computational speed compared to other MC-based methods. The simulation results for a two-stage class-AB Op-Amp in 180 nm CMOS technology demonstrate a yield value of 99.72%. This computational approach stands out as a high-speed and high-accuracy technique, employing only one evolutionary algorithm. Furthermore, by modifying the initial population, improvements in both the convergence speed and yield value of the evolutionary algorithm have been observed. The efficiency of the proposed technique is validated through extensive simulation results.

Author Contributions

Conceptualization and design, A. Yaseri; formal analysis, A. Yaseri; software, A. Yaseri; investigation, M. H. Maghami.; writing—original draft preparation, A. Yaseri; writing—review and editing, M. H. Maghami. supervision, M. H. Maghami, and M. Radmehr.

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Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the ethical issues including plagiarism, informed consent, misconduct, data fabrication and, or falsification, double publication and, or submission, and redundancy have been completely witnessed by the authors.

Abbreviations

MC	Monte Carlo
RSB	response-surface-based
PSWCD	performance-specific worst-case design
LHS	Latin hypercube sampling
QMC	Gaussian Monte Carlo simulation

MOEA/D	Multi-Objective Evolutionary Algorithm based on Decomposition
OCBA	optimal computing budget allocation
MOO	Multi-Objective Optimization
MOEA	multi-objective evolutionary algorithm
CA	Critical Analysis
UGBW	unity-gain bandwidth
CMRR	common-mode rejection ratio
THD	total harmonic distortion
SR	slew rate
PSRR	Power Supply Rejection Ratio
BW	Bandwidth

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