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Multistep Model Predictive Control of Diode-Clamped Multilevel Inverter

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Abstract

Background and Objectives: To overcome the disadvantages of the traditional two-level inverters, especially in electric drive applications, multi-level inverters (MLIs) are the widely accepted solution. Diode-Clamped Inverters (DCIs) are a well-known structure of multi-level inverters. In DCIs, the voltage balance of the DC-link capacitors and the Common Mode (CM) voltage reduction are two important criteria that should be considered.
Methods: This paper concentrates on the current control of 3-phase 4-level DCI with finite control set model predictive control (MPC) strategy. Current tracking performance, DC-link capacitor voltage balance, switching frequency minimization, and CM voltage control have been considered in the objective function of the MPC. Moreover, the multistep prediction method has been applied to improve the performance of the DCI.
Results: The effectiveness of the proposed multistep prediction control for the 4-level DCI has been evaluated with different horizon lengths. Moreover, the effect of several values of weighting factors has been studied on the system behavior.
Conclusion: Results validate the accuracy of current tracking and voltage balancing in the suggested multistep MPC for the 4-level DCI. In addition, CM voltage control and switching frequency reduction can be included in the predictive control. Decreasing the CM voltage and switching frequency will oppositely affect the dynamic behavior and voltage balancing of the DCI. Therefore, selection of weighting factors depends on the system needs and requirements.

Introduction

Nowadays, multilevel converters (MLCs) are widely utilized in medium- and high-voltage applications for generating high-quality voltage and current [1], [2]. In comparison with the conventional two-level converter, MLCs can operate at higher voltage ratings for the same switching frequency and with lower dv/dt.

Therefore, MLCs are used in high-power drives [3], active filters [4], electric transportation systems [5]-[7], and other industrial applications such as fans, blowers, and pumps.

Three well-known topologies of multi-level inverters (MLIs) are the diode-clamped inverter (DCI), flying capacitor inverter [8], and cascaded H-bridge inverter [9]-[11]. Diode-clamped inverters offer high efficiency, low number of capacitors, and low stress on power electronic switches. Therefore, they are popular in various industrial applications. This paper concentrates on the 4-level diode-clamped inverter.

Traditional control approaches for producing the switching pulses of the DCI are the linear control [12] and the space vector modulation [13], [14]. Also, modulation techniques have also been presented in low frequency applications for reducing the common mode (CM) voltage, decreasing the output THD of the inverter and

harmonics elimination, and reducing the switching frequency of the inverter [15]-[17].

In recent years, new control approaches have been studied to control the power and current of inverters. Among them is the Model Predictive Control (MPC) [18]-[20]. The MPC offers desirable advantages such as fast response dynamics and compatibility with the system nonlinearity and various restrictions [21]-[28]. The MPC uses the mathematical model of the system to predict the system's behavior in future horizons. A cost function is defined according to the desired behavior of the system. In fact, the MPC is an optimization method that obtains the optimal switching state of the inverter by minimizing the cost function. Finally, the best switching state is applied to the inverter.

Since all calculations are repeated in each sampling period, for a large number of switching states, the computation burden is high. In the practical applications of the MPC for the MLIs, it is important to reduce the number of switching states. Recently, different strategies have been proposed for moderating the computation burden in MLIs with MPC [29]-[37]. Sometimes, this issue is solved by using the offline method. For this purpose, all possible states of the system are calculated offline. Accordingly, a look-up table is prepared and given as input to the system so that they can be used in each interval instead of many calculations [38], [39].

The MPC of DCI has been investigated in the literature for different applications [40]-[47]. However, the research in this field has not yet been completed. In [41], the MPC of 4-level DCI has been investigated for wind turbine systems. Different criteria have been included in the objective function of MPC such as switching states and CM voltage. In this work, the prediction has been only carried out with a horizon of N=2. Moreover, the effect of different weighting factors has not been studied in this work. The MPC for grid-connected 4-level DCI has been evaluated in [44]. Active and reactive power, capacitor voltage balancing, and switching frequency have been considered in the objective function. The delay-compensation method has been applied. But the CM voltage has not been minimized. Furthermore, multi-step prediction has not been utilized in the control scheme. In [44], the MPC of 4-level DCI has been investigated for wind energy systems. The capacitor voltage balancing and the number of switching states have been included in the objective function of MPC. However, the CM voltage has not been considered. In addition, the MPC of a 4-level DCI has been performed with a prediction horizon of N=1. In [47], a simplified MPC has been proposed for 4-level DCIs. The suggested method yields lower computational burden and total harmonic distortion (THD) in compare to the traditional MPC. However, only the current tracking and capacitor voltage balancing have been included in the objective function of the proposed MPC. In addition, the prediction has been only carried out with a horizon of N=1. This paper proposes a multistep MPC strategy for the current control of the 3-phase 4-level DCI, considering different cost functions. Current control, DC-link capacitor voltage balance, switching frequency minimization, and CM voltage control have been considered in the prediction method. The delay compensation with the multistep prediction method has been applied to improve the performance of DCI. The main contributions of this paper are as follows:

- Presenting a multistep predictive current control for the 3-phase 4-level DCI
- Evaluating several horizon lengths in multistep prediction control of the 4-level DCI
- Including various objectives in the predictive controller such as current tracking, DC-link voltage balance, reduction of the CM voltage, and decreasing the switching frequency
- Evaluating the effect of different values of weighting factors on the system performance

Mathematical Model of 4-Level DCI

Fig. 1 illustrates the topology of the three-phase 4-level DCI. Eighteen IGBT switches with anti-parallel diodes, eighteen clamping diodes, and three capacitors are used to generate four voltage levels. The switches are placed in up and down groups and receive complementary firing pulses. A 4-level DCI has 4^3=64 switching states. Table 1 shows all feasible switching conditions of the single-phase 4-level DCI and the related voltage level.

According to Table 1, the DCI voltages can be written as [43], [44]:

$$\begin{aligned} v_{aO} &= v_{C1}.S_{a1} + v_{C2}.S_{a2} + v_{C3}.S_{a3} \\ v_{bO} &= v_{C1}.S_{b1} + v_{C2}.S_{b2} + v_{C3}.S_{b3} \\ v_{cO} &= v_{C1}.S_{c1} + v_{C2}.S_{c2} + v_{C3}.S_{c3} \end{aligned} \quad (1)$$

where v_{cj} is the voltage of j-th capacitor ($j \in \{1,2,3\}$). S_{xy} is the switching state of the y-th IGBT ($y \in \{1,2,3\}$) in phase x ($x \in \{a,b,c\}$) of the DCI (as shown in Fig. 1). In the 4-level DCI, the CM voltage can be calculated as [41]:

$$v_{nO} = v_{CM} = \frac{v_{aO} + v_{bO} + v_{cO}}{3} \quad (2)$$

where O is the negative DC-Link and n is the neutral point of the load.

The phase voltage with respect to the load neutral can be written as [41]:

$$\begin{aligned} v_{an} &= v_{aO} - v_{nO} \\ v_{bn} &= v_{bO} - v_{nO} \\ v_{cn} &= v_{cO} - v_{nO} \end{aligned} \quad (3)$$

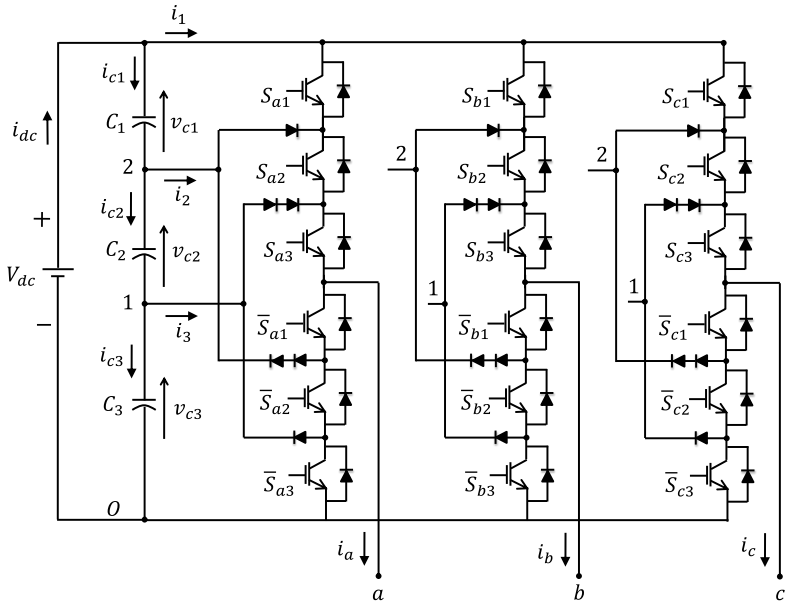

Fig. 1: Structure of 3-phase 4-level DCI [49].

Table 1: Switching states of the 4-level DCI [40]

S_x	Output Voltage Level	Switching Pulse		
		S_{x1}	S_{x2}	S_{x3}
0	0	0	0	0
1	v_{c3}	0	0	1
2	$v_{c2}+v_{c3}$	0	1	1
3	$v_{c1}+v_{c2}+v_{c3}$	1	1	1

The discrete-time model of the capacitor voltages can be written as [48]:

$$v_{c1}(k+1) = v_{c1}(k) + \frac{T_s}{C_1} i_{c1}(k) \tag{4}$$

$$v_{c2}(k+1) = v_{c2}(k) + \frac{T_s}{C_2} i_{c2}(k) \tag{5}$$

$$v_{c3}(k+1) = v_{c3}(k) + \frac{T_s}{C_3} i_{c3}(k) \tag{6}$$

in which $v_{c1}(k)$, $v_{c2}(k)$, and $v_{c1}(k)$ are the capacitor voltages. $i_{c1}(k)$, $i_{c2}(k)$, and $i_{c1}(k)$ are the capacitor currents and can be computed as [49]:

$$\begin{aligned} i_{C1}(k) &= -i_1(k) \\ i_{C2}(k) &= -i_1(k) - i_2(k) \\ i_{C3}(k) &= -i_1(k) - i_2(k) - i_3(k) \end{aligned} \tag{7}$$

where

$$\begin{aligned} i_1(k) &= K_{a1} i_a(k) + K_{b1} i_b(k) + K_{c1} i_c(k) \\ i_2(k) &= K_{a2} i_a(k) + K_{b2} i_b(k) + K_{c2} i_c(k) \\ i_3(k) &= K_{a3} i_a(k) + K_{b3} i_b(k) + K_{c3} i_c(k) \end{aligned} \tag{8}$$

where K_{xy} $(x \in \{a,b,c\}, y \in \{1,2,3\})$ can be defined as [49]:

$$\begin{aligned} K_{x1} &= S_{x1}\, S_{x2}\, S_{x3} \\ K_{x2} &= \bar{S}_{x1}\, S_{x2}\, S_{x3} \\ K_{x3} &= \bar{S}_{x1}\, \bar{S}_{x2}\, S_{x3} \end{aligned} \tag{9}$$

in which S_x is defined in Table 1.

For the resistive-inductive load, the discrete-time model of the DCI load current can be written as [48]:

$$i_a(k+1) = \left(1 - \frac{RT_s}{L}\right) i_a(k) + \frac{T_s}{L} v_{an}(k) \tag{10a}$$

$$i_b(k+1) = \left(1 - \frac{RT_s}{L}\right) i_b(k) + \frac{T_s}{L} v_{bn}(k) \tag{10b}$$

$$i_c(k+1) = \left(1 - \frac{RT_s}{L}\right) i_c(k) + \frac{T_s}{L} v_{cn}(k) \tag{10c}$$

in which k is the sampling instant and T_s represents the sampling time. R and L are the load resistance and inductance, respectively. $v_{an}(k)$, $v_{bn}(k)$, and $v_{cn}(k)$ are the phase voltages and can be obtained from (1)-(3) using the measured capacitor voltages and optimal switching states.

Single-Step Model Predictive Control of the 4-Level DCI

Fig. 2 represents the block diagram of the MPC strategy for a 4-level three-phase DCI. The main aim is to predict the load current and capacitor voltages in the next sampling instant. Accordingly, all 64 switching states of the 4-level DCI are searched to find the optimal switching state that minimizes the objective function. In the single-step MPC method and without the delay compensation, the predictions were made in the (k+1)-th sampling instant.

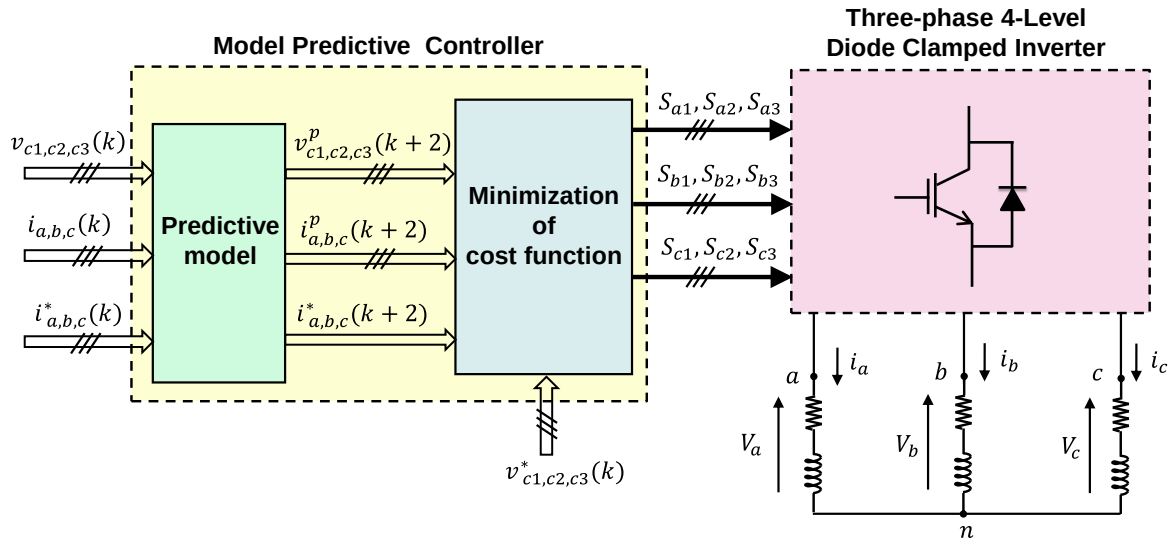

Fig. 2: MPC of the 4-level three-phase DCI with delay compensation method [40].

In practice, the computational delay due to the microprocessor's operation affects the accuracy of the prediction. Therefore, the delay compensation strategy is proposed to compensate the perdition error. In the delay compensation strategy, the predictions are made for the (*k*+2)-th sampling instant.

The prediction of load currents in the (*k*+2)-th sampling instant gives [49]:

$$i_x(k+2) = \left(1 - \frac{RT_s}{L}\right) i_x(k+1) + \frac{T_s}{L} v_{xn}(k+1) \tag{11}$$

where $x \in \{a, b, c\}$.

Furthermore, the capacitor voltages are predicted for the (*k*+2)-th sampling instant [49]:

$$\begin{aligned} v_{c1}(k+2) &= v_{c1}(k+1) + \frac{T_s}{C_1} i_{c1}(k+1) \\ v_{c2}(k+2) &= v_{c2}(k+1) + \frac{T_s}{C_2} i_{c2}(k+1) \\ v_{c3}(k+2) &= v_{c3}(k+1) + \frac{T_s}{C_3} i_{c3}(k+1) \end{aligned} \tag{12}$$

The overall objective function can be defined as:

$$g(k+2) = g_i(k+2) + \lambda_V\, g_{v_c}(k+2) + \lambda_S\, g_{sw}(k+2) + \lambda_{CM}\, g_{CM}(k+2) \tag{13}$$

where g_i, g_{v_c}, g_{sw}, and g_{CM} are the terms of the objective function to control current tracking, capacitor voltage balance, CM voltage, and switching frequency, respectively. λ_V, λ_S, and λ_{cm} are the weighting factors that adjust the capacitor voltages, CM voltage, and switching frequency, respectively.

g_i and g_{v_c} can be written as [44]:

$$g_i(k+2) = \sum_{x=a,b,c} \left(i^*_x(k+2) - i_x(k+2)\right)^2 \tag{14}$$

$$g_{v_c}(k+2) = \sum_{j=1,2,3} \left(v^*_{cj} - v_{cj}(k+2)\right)^2 \tag{15}$$

Moreover, v^*_{c1}, v^*_{c2}, and v^*_{c3} are the final capacitor voltages:

$$v^*_{c1} = v^*_{c2} = v^*_{c3} = \frac{V_{dc}}{3} \tag{16}$$

i^*_a, i^*_b, and i^*_c are the current references. The future current references of the (*k*+2)-th sampling instant can be computed using extrapolation [48]:

$$i^*_x(k+2) = 6\, i^*_x(k) - 8\, i^*_x(k-1) + 3\, i^*_x(k-2) \tag{17}$$

where $x \in \{a, b, c\}$.

Moreover, g_{sw} can be calculated as [44]:

$$g_{sw}(k+2) = \sum_{x=a,b,c} \sum_{j=1}^{3} \left|S_{xj}(k+2) - S_{xj}(k+1)\right| \tag{18}$$

Note that g_{sw} is related to the number of switching commutations that directly affect the average switching frequency of the DCI.

g_{CM} can be extracted using (2):

$$g_{CM}(k+2) = v_{CM}(k+2) \tag{19}$$

Fig. 3 illustrates the flowchart of the MPC strategy for a 4-level DCI with the prediction horizon of N=1 and delay compensation.

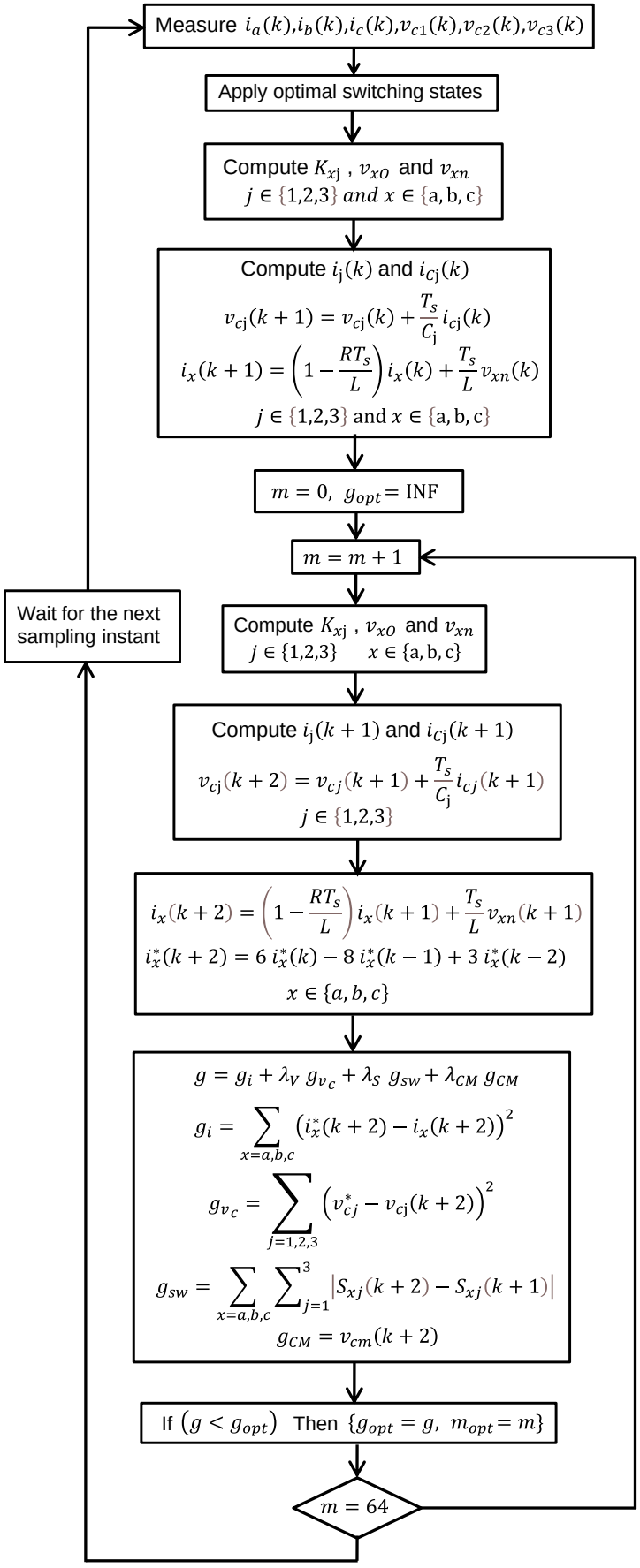

Fig. 3: Flowchart of the MPC of a 4-level DCI with a prediction horizon of N=1.

Multistep MPC in 4-Level DCI

The main aim of the multistep MPC is to predict the system behavior in more than one sampling instant. In the multistep prediction strategy, the total objective function in the horizon of N can be defined as:

$$g_{total} = \sum_{l=2}^{N+1} g(k+l) \tag{20}$$

where N is the horizon of prediction. With the prediction horizon of N=1, the prediction index is (k+2), and the objective function becomes the same as in (13).

By substituting (13)-(19) in (20), the total objective function in the horizon of N can be written as in (21). Fig. 4 represents the main part of the multistep MPC algorithm with a prediction horizon of N=3, which has the task of minimizing the objective function. All 64^3 switching possibilities will be searched.

$$g_{total} = \sum_{l=2}^{N+1} \Big(\sum_{x=a,b,c} \big(i_x^*(k+l) - i_x(k+l)\big)^2 + \lambda_V \sum_{j=1,2,3} \Big(v_{cj}^* - v_{cj}(k+l)\Big)^2 + \lambda_{sw} \sum_{x=a,b,c} \sum_{j=1}^{3} \big|S_{xj}(k+l) - S_{xj}(k+l-1)\big| + \lambda_{cm} v_{cm}(k+l) \Big) \tag{21}$$

In a specific switching condition, if the objective function g_{total} becomes lower than the optimal value g_{opt}, the switching condition will be saved as m_{opt}. The optimum switching condition m_{opt} will be applied to the DCI in the next sampling instant.

The future current references of the (k+3), (k+4), and (k+5)-th sampling instant can be calculated as [48]:

$$i_x^*(k+3) = 10\, i_x^*(k) - 15\, i_x^*(k-1) + 6\, i_x^*(k-2) \tag{22}$$

$$i_x^*(k+4) = 15\, i_x^*(k) - 24\, i_x^*(k-1) + 10\, i_x^*(k-2) \tag{23}$$

$$i_x^*(k+5) = 21\, i_x^*(k) - 35\, i_x^*(k-1) + 15\, i_x^*(k-2) \tag{24}$$

where $x \in \{a, b, c\}$.

```
for m=1:64
Compute g(k+2) = g_i(k+2) + λ_V g_vc(k+2) + λ_S g_sw(k+2) + λ_CM g_CM(k+2)
    for n=1:64
    Compute g(k+3) = g_i(k+3) + λ_V g_vc(k+3) + λ_S g_sw(k+3) + λ_CM g_CM(k+3)
        for i=1:64
        Compute g(k+4) = g_i(k+4) + λ_V g_vc(k+4) + λ_S g_sw(k+4) + λ_CM g_CM(k+4)
        g_total = g(k+2) + g(k+3) + g(k+4)
            if ( g_total < g_opt )  then (g_opt = g_total, m_opt = m)
            end if
        end for
    end for
end for
```

Fig. 4: Main part of the multistep MPC algorithm for the 4-level DCI with a prediction horizon of N=3.

Results and Discussion

The effectiveness of the suggested multistep MPC method is verified by simulating a 4-level DCI with Matlab/Simulink. The total DC-link voltage is 520 V. The DC-link capacitors are C_1=C_2=C_3=2.2 mF. The load resistance and inductance are R= 10 Ω and L= 10 mH, respectively.

Fig. 5 illustrates the simulation results in the 4-level DCI with multistep MPC for prediction horizon of N=2. The weighting factor λ_V is set to 0.5. The weighting factors λ_S and λ_{CM} are set to zero. The sampling time T_s is 50 µsec. A 50 µsec delay time has been applied to the controller for modeling the computational delay in the practical conditions. To validate the tracking performance of the multistep MPC strategy, the reference currents are changed from 10 A to 5 A at t=0.06 sec. Fig. 5(a) shows the current tracking performance in the 4-level DCI with multistep MPC. It is visible that the currents follow their references properly. Fig. 5(b) presents the line-to-line

voltage (V_{ab}) in the 4-level DCI with multistep MPC. The voltage amplitude corresponds to the step change in the load current. Fig. 5(c) shows the capacitor voltages (v_{C1}, v_{C2}, v_{C3}) in the 4-level DCI. The distortion in the voltage balance of the capacitors is low and is not affected by the step change in the reference currents. Fig. 5(d) illustrates the CM voltage (v_{cm}) in the 4-level DCI with multistep MPC for prediction horizon of N=2. The CM voltage and the switching frequency are high since they are not included in the objective function.

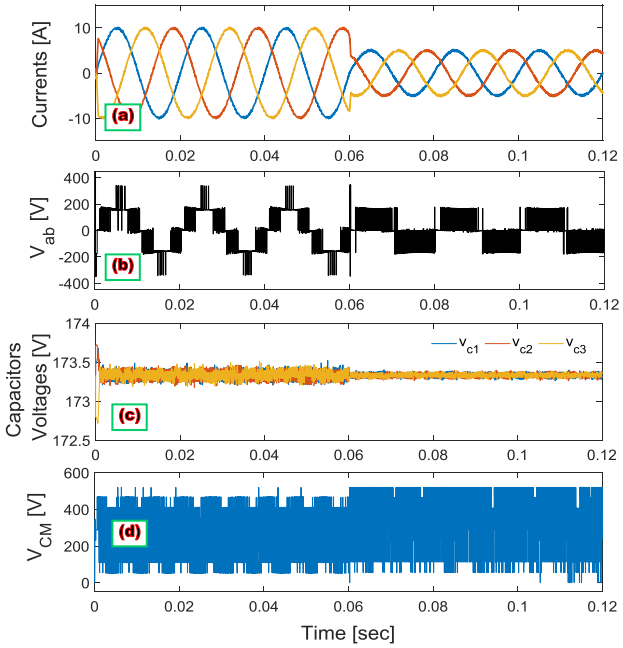

Fig. 5: Simulation results of the 4-level DCI with multistep MPC for N=2: (a) current; (b) line voltage; (c) capacitor voltages; (d) CM voltage.

Fig. 6 compares the load current, phase voltage (V_{an}), and line-to-line voltage (V_{ab}) of the MPC strategy in 2-level VSI with 4-level DCI. Simulation parameters are the same as in Fig. 5. It is obvious that the harmonic distortion is much lower in 4-level DCI than in 2-level VSI. The current THD is reduced from 15.47% in 2-level VSI to 1.82% in 4-level DCI.

Figs. 7(a)-(d) show the load current in the 4-level DCI with traditional MPC without delay compensation, single-step MPC with a horizon of N=1, and multistep MPC with a horizon of N=2 and N=3, respectively. In multistep MPC methods, the future prediction of reference currents can be obtained from (22)-(24). Simulation parameters are the same as in Fig. 5. The sampling time T_s is 100 µsec. A 100 µsec delay time has been applied to the controller. It is evident that the lowest current distortion belongs to the multistep MPC with a horizon of N=3 (as shown in Fig. 7(d)) and the highest current distortion refers to the traditional MPC without delay compensation (as shown in Fig. 7(a)).

Figs. 8(a)-(d) present the capacitor voltages in the 4-level DCI with traditional MPC without delay compensation, single-step MPC with a horizon of N=1, and multistep MPC with a horizon of N=2 and N=3, respectively. It is visible that the capacitor voltage balance is higher in the multistep MPC (as shown in Fig. 8(d)) than in the traditional MPC without delay compensation (as shown in Fig. 8(a)). The voltage balance with a horizon of N=2 (according to Fig. 8(c)) is almost similar with the horizon of N=3 (according to Fig. 8(d)). Further increase in the prediction horizon will increase the computational burden and the simulation time, while the DCI performance does not improve significantly. Thus, it is not preferable.

In the next part, the effect of different weighting factors on the system performance is investigated. The multistep MPC with a horizon of N=2 has been applied to control the 4-level DCI. The sampling time T_s is 100 µsec and a 100 µsec delay time has been applied to the controller.

Fig. 9 shows the effect of two different values of λ_V on the performance of 4-level DCI. The weighting factors λ_S and λ_{CM} are set to zero. λ_V is changed from zero to 0.5 at t=0.06 sec. Figs. 9(a)-(b) show the currents and line voltage in the 4-level DCI with multistep MPC with a horizon of N=2. The tracking performance is not affected in the steady-state condition. Fig. 9(c) presents the capacitor voltages (v_{C1}, v_{C2}, v_{C3}) in the 4-level DCI. As can be seen, increasing λ_V balances the DC link capacitor voltages. Figs. 9(d)-(e) illustrate the CM voltage and gate pulse S_{a1} in the 4-level DCI with multistep MPC. The CM voltage and the switching frequency increase significantly in higher values of the weighting factor λ_V.

Fig. 10 presents the comparative results of the system behavior with three different values of λ_S. The value of λ_S is changed from zero to 0.1 at t=0.04 sec and from 0.1 to 0.3 at t=0.08 sec. Moreover, λ_V=0.5 is selected, and λ_{CM} is set to zero. Figs. 10(a)-(b) show the currents and line voltage in the 4-level DCI with multistep MPC with a horizon of N=2. The tracking performance is not affected in different values of λ_S. Fig. 10(c) presents the capacitor voltages (v_{C1}, v_{C2}, v_{C3}) in the 4-level DCI. As can be seen, increasing λ_S results in a higher voltage unbalance. Figs. 10(d)-(e) illustrate the CM voltage and gate pulse S_{a1} in the 4-level DCI. It is visible that increasing λ_S reduces the switching frequency; however, the CM voltage is high since it is not included in the objective function.

Fig. 11 illustrates the effect of three different values of λ_{CM} on the system performance. λ_{CM} is changed from zero to 0.05 at t=0.04 sec and from 0.05 to 0.1 at t=0.08 sec. λ_V=0.5 is selected, and λ_S is set to zero. Figs. 11(a)-(b) show the currents and line voltage in the 4-level DCI with multistep MPC with a horizon of N=2. As can be seen, increasing λ_S reveals a higher harmonic distortion in the current and voltage waveforms. Fig. 11(c) presents the

capacitor voltages (v_{C1}, v_{C2}, v_{C3}) in the 4-level DCI. Reducing the CM voltage leads to a significant decrease of the voltage balance. Figs. 11(d)-(e) illustrate the CM voltage and gate pulse S_{a1} in the 4-level DCI. It is obvious from the results that increasing λ_{CM} reduces of CM voltage.

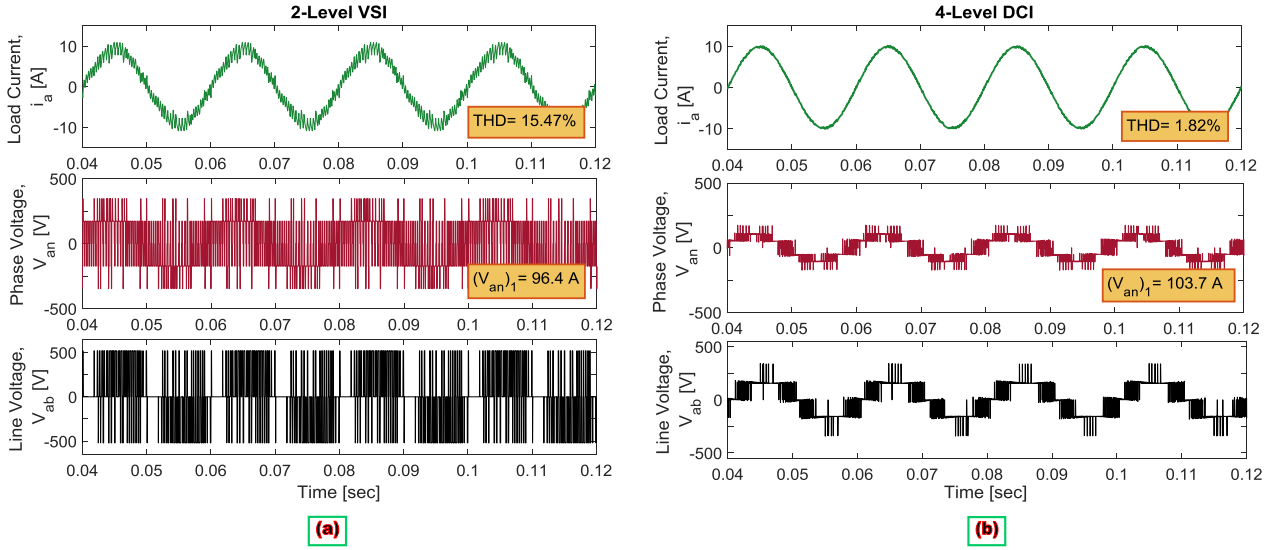

Fig. 6: Load current, phase voltage, and line voltage with MPC strategy in: (a) 2-level VSI; (b) 4-level DCI.

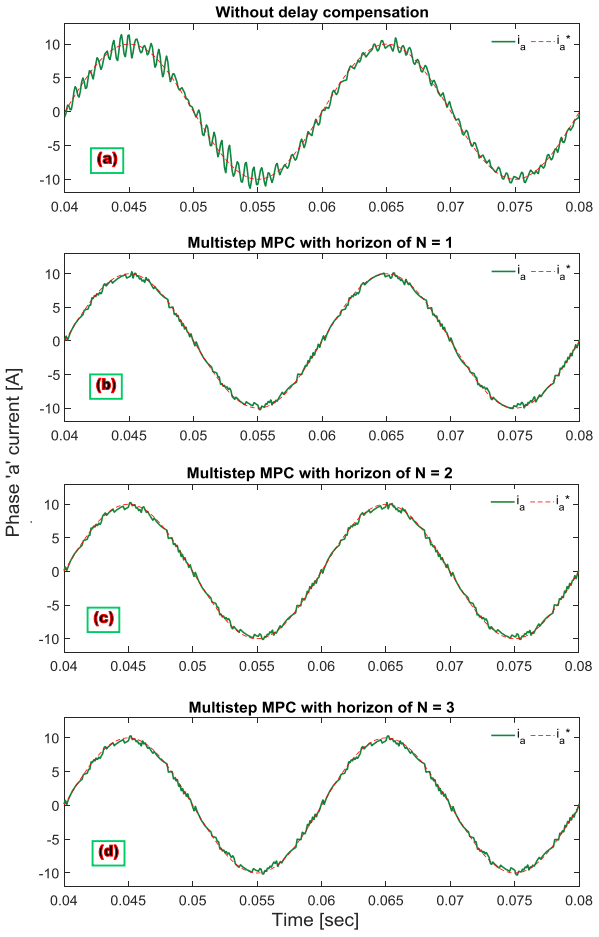

Fig. 7: Phase 'a' current in the 4-level DCI: (a) MPC without delay compensation; (b) single-step MPC with a horizon of N=1; (c) multistep MPC with a horizon of N=2; (d) multistep MPC with a horizon of N=3.

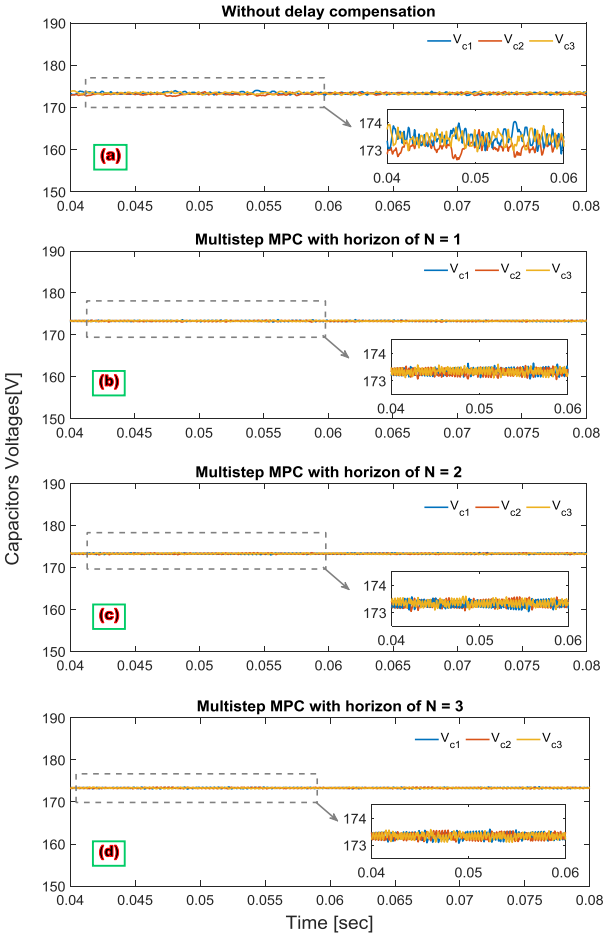

Fig. 8: Capacitor voltages in the 4-level DCI: (a) MPC without delay compensation; (b) single-step MPC with a horizon of N=1; (c) multistep MPC with a horizon of N=2; (d) multistep MPC with a horizon of N=3.

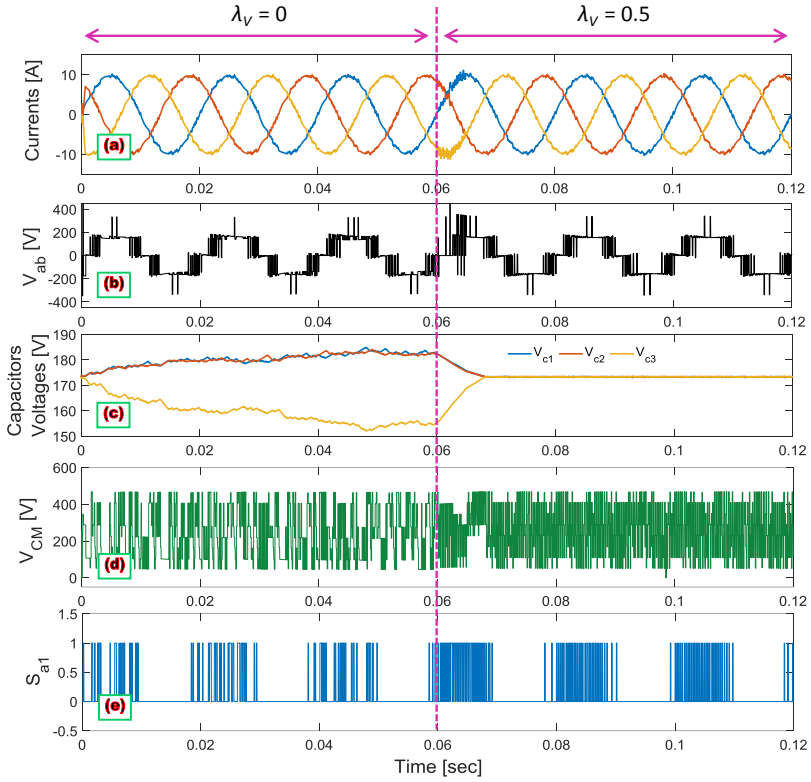

Fig. 9: Effect of weighting factor λ_V on the behavior of 4-level DCI with multistep MPC for N=2: (a) current; (b) line voltage; (c) capacitor voltages; (d) CM voltage; (e) gate pulse S_{a1}.

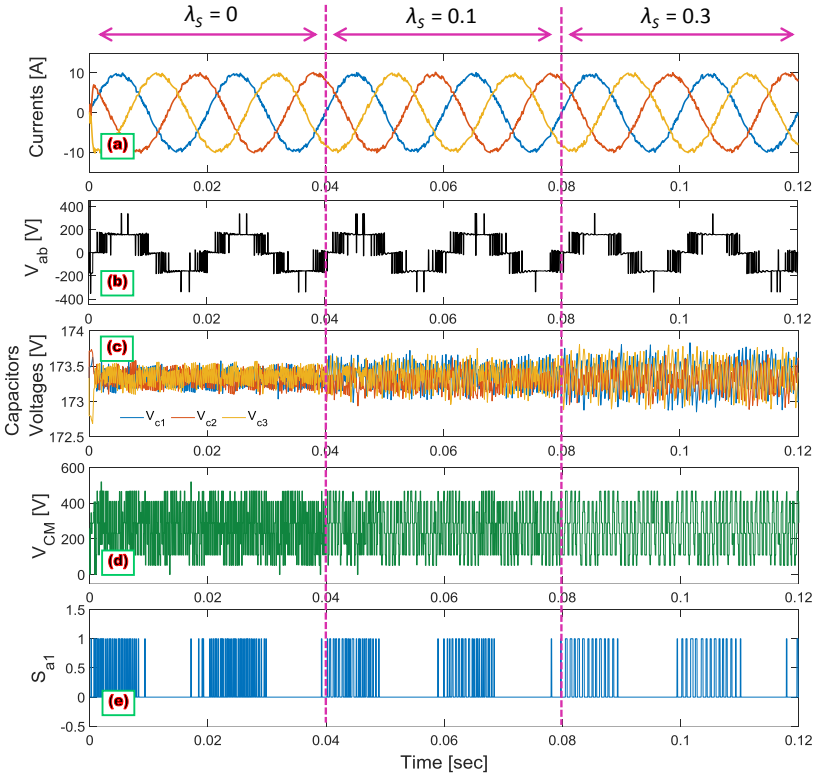

Fig. 10: Effect of weighting factor λ_S on the behavior of 4-level DCI with multistep MPC for N=2: (a) current; (b) line voltage; (c) capacitor voltages; (d) CM voltage; (e) gate pulse S_{a1}.

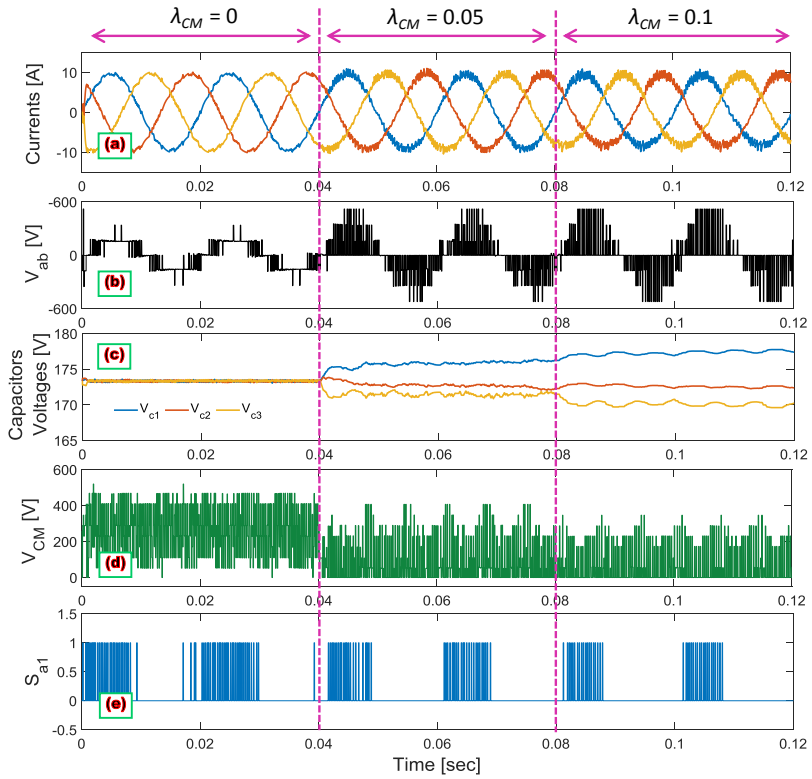

Fig. 11: Effect of weighting factor λ_{CM} on the behavior of 4-level DCI with multistep MPC for N=2: (a) current; (b) line voltage; (c) capacitor voltages; (d) CM voltage; (e) gate pulse S_{a1}.

Conclusion

This work has proposed a multistep predictive current control for the 3-phase 4-level DCI. The suggested method has succeeded in controlling the load current, while other objectives were easily included in the predictive controller. In addition to the current tracking, this paper has evaluated the DC-link voltage balance, reduction of the CM voltage, and decreasing the switching frequency in the prediction strategy. In this regard, the multistep prediction control with different horizon lengths has been applied to the 4-level DCI. Moreover, the effect of different values of weighting factors has been studied on the system performance.

Simulation results have revealed the excellent dynamic response and DC-link voltage balancing in the 4-level DCI controlled by the multistep predictive method with a horizon of N=2. However, in long prediction horizons, the simulation time and computational burden will increase. Therefore, current tracking quality and voltage balancing may not be obtained. On the other hand, decreasing the CM voltage and the switching frequency has the opposite effect on the current tracking quality and voltage balancing in the DCI. Generally, dynamic response and voltage balancing are the main requirements of the DCI. Therefore, a trade-off will be imposed when selecting the weighting factors of the objective function depending on the system requirements. The future work will focus on the multistep model predictive control of motor drives supplied with 4-level diode-clamped inverter including various objectives in the predictive controller. Furthermore, the effect of different values of weighting factors on the system performance will be investigated.

Author Contributions

P. Hamedani carried out the simulations, interpreted the results, and wrote the manuscript.

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Conflict of Interest

The author declares no potential conflict of interest regarding the publication of this work.

Abbreviations

CM	Common Mode
DCI	Diode-Clamped Inverter
MLC	Multilevel Converter
MLI	Multilevel Inverter
MPC	Model Predictive Control
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter

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