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Research paper

Modified Topologies for Single Source Switched-Capacitor Multilevel Inverters

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Abstract

Background and Objectives: Increasing environmental problems and challenges have led to increased use of renewable energy sources such as photovoltaic or PV system. One of the attractive research fields is power electronic converters as interfaces for renewable energy sources. Multilevel inverters can operate as such interfaces. This paper introduces modified topologies of switched-capacitor multilevel inverters, designed to overcome constraints of low voltage renewable energy sources such as PV.

Methods: Configuration of topologies utilize a single DC source with series or parallel connection of capacitors to produce 7-level, 9-level, and 11-level voltage in the converter load side. The paper presents the converter operation principle, elements voltage stress analysis, and capacitor sizing calculations. Also, operation analysis of suggested inverter topologies is validated using implemented set up.

Results: Comprehensive comparative analysis reveals that the proposed topologies have merits and superior performance compared to existing solutions regarding component number, voltage boost factor, and voltage stress. The experimental measurement results confirm the accuracy of multilevel output voltage waveforms and the self-balancing of capacitor voltages, as predicted by theoretical analysis.

Conclusion: The suggested switched-capacitor multilevel inverters, moreover the superiority over previously presented topologies, show great potential for application in photovoltaic systems and electric vehicle battery banks.

Introduction

In order to achieve zero carbon emissions, renewable energy sources have gained noteworthy regard due to their dependable performance, minimal ecological footprint, cost efficiency, and adaptability within systems. Increasing adoption of renewable energy sources and electric vehicles has led to a growing need for enhanced voltage boost capability. Nevertheless, most of DC sources such as solar cells and EV batteries have a restricted capacity for boosting power, indicating the need for immediate improvements in this field [1]-[3].

Commercial solutions in this field typically use two-stage power conversion, utilizing a step-up converter. In order to get the highest possible output voltage, the components utilized in these converters operate at high switching frequencies, which increase power losses and prices [4]. The impedance source inverter, which employs LC units, incurs additional system volume and expense. In addition, the converters' two-level setup results in high total harmonic distortion (THD) and power losses. The high rate of voltage variation (d*v*/d*t*) in switches increases power losses during switching, and also, increases voltage

stress and electromagnetic interference (EMI), and impaired reliability. Ultimately, this can lead to reduction in lifespan of electric vehicles or motors [5]-[8].

Industry commonly utilizes multilevel inverters, including traditional diode-clamp, flying-capacitor, and cascade H-bridge topologies. These inverters offer several benefits, such as low output voltage THD, less switching stress, and lower operating frequency. Traditional configurations of multilevel inverters cannot enhance the input voltage [5]-[8].

An innovative multilevel inverter utilizing switched capacitor (SC) approach was provided as a solution to address the abovementioned limitations [9]-[11]. SC multilevel inverters offer the following benefits:

- Capacitor voltage self-balance: This feature guarantees that the voltage across every capacitor in the inverter is similar, hence preserving the stability of the inverter [12], [13].
- The inverter does not utilize significant magnetic components and transformers, resulting in lighter and smaller sizes, enhancing its portability and compactness [12], [14], [15].
- Offer a high degree of flexibility as they can be quickly adjusted to match the individual needs of various applications [16], [17].
- SC multilevel inverters provide the ability to boost the input voltage, which distinguishes them from traditional multilevel inverters [12], [18], [19].

SC multilevel inverters have some demerits, such as employing high count of active and passive elements, and capacitor voltage balancing concerns [20]. However, they are still highly regarded for their merits and have been proposed for use in high-power photovoltaic systems [21].

A multilevel inverter including SC cells was introduced in [22]. This inverter can be constructed in symmetric or asymmetric configurations and possesses the capability to expand up to greater levels. Its main advantage is low voltage stress on its switches. Nevertheless, the primary disadvantages of this system consist in its extensive utilization of numerous switches and the inclusion of unidirectional switches. A topology capable of producing a voltage with seven distinct levels and a voltage boost factor of 3 has been suggested in [23]. This is accomplished by utilizing only four high-frequency switches, which are secured by low-voltage capacitors. Nevertheless, this configuration experience significant voltage stress on the switches and also, necessitate additional passive components. Consequently, size and weight of the converter are increased. A seven-level inverter design was suggested in [24] for use in medium-voltage scenarios, particularly for high-power applications. The configuration includes eight operational switches, two internal flying-capacitor units, and two diodes. However, this topology has two primary disadvantages: the use of two unidirectional current switches and the imposition of considerable voltage stress on the switch.

In [25], a generalized boost multilevel inverter that can be utilized in applications with low-voltage input sources.

By controlling the parallel and series connection of capacitors and DC sources, this configuration can produce high voltage levels.

The important demerit of this topology is utilizing high count of passive elements, which increases the converter cost, size, and weight. The single-phase SC MLI proposed in [26] can produce a nine-level AC voltage with a voltage gain of 4 in the output. This 9-level topology is achieved by modifying the switching algorithm of the 13-level configuration introduced in [26].

However, this topology has essential downside as it requires a large number of switches, which in turn increases the need for gate drivers, and subsequently, the cost and size of the converter. A 9-level inverter was introduced in [27], which offers the significant advantage of zero current switching for charging capacitors. However, its primary drawback is utilization of high count of switches, diodes, capacitors, and switches with very high total standing voltage (TSV). According to the configuration presented in [28], 11-level switched-capacitor multilevel inverter can produce an output voltage waveform using 14 switches, 3 capacitors, and 2 diodes. However, this topology has a major drawback of using a lot of switches and a low boost factor. A single-phase switched-capacitor based 11-level inverter topology is presented in [29].

This configuration offers increased levels, a quintuple voltage boost factor, and natural capacitors voltage-balancing as its main features. However, due to the inclusion of more passive elements and high TSV, power loss, cost, and volume are increased. The 11-level topology that uses the SC technique, described in [30], offers several benefits including capacitor voltage self-balancing and high boost efficiency. However, because of large number of power switches and high TSV, the converter experiences high power losses that consequently reduce efficiency.

The rest of the paper is organized as follows: In section 2, proposed multilevel inverter topology and operation are described. Section 3 presents extended topology of suggested converter. Capacitor sizing calculations is given in section 4, and converter power losses are computed in section 5. Section 6 presents comprehensive comparison of the introduced converter with similar topologies. Experimental test results are illustrated in section 7, and section 8 concludes the paper.

Proposed 7-Level Inverter Topology

A. Circuit Description

Circuit schematic of proposed boost multilevel inverter is illustrated in Fig. 1. Suggested 7-level topology contains a DC voltage source, V_{in}, two capacitors, C_1 and C_2 along with the voltage source with two power diodes, and eight power semiconductor switches to produce 7-level voltage in the output. Capacitors C_1 and C_2 have equal capacity and are charged in the same manner. Proposed MLI generates output voltage with levels of $\pm V_{in}$, $\pm 2V_{in}$, and $\pm 3V_{in}$ by H-bridge inverter. Different switching modes for the suggested topology to produce 7-level output voltage are shown in Table 1. All switches used in this configuration have the ability to facilitate bidirectional current so, the converter supports the inductive load with reverse current flow.

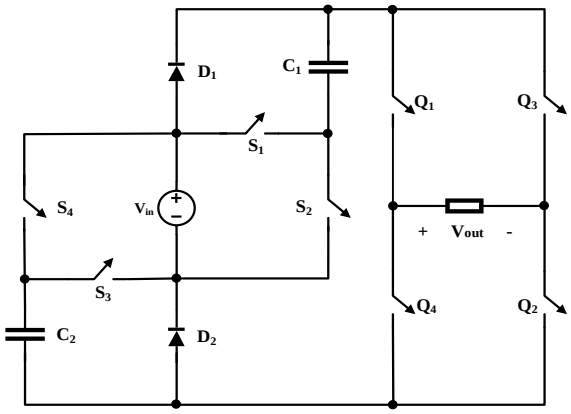


Fig. 1: Configuration of proposed 7-level switched-capacitor inverter.

Table 1: Circuit elements states for 7-level topology operation.

$\frac{V_o}{V_{in}}$	Switch and diode state										Capacitor state	
	S_1	S_2	S_3	S_4	Q_1	Q_2	Q_3	Q_4	D_1	D_2	C_1	C_2
+3	1	0	1	0	1	1	0	0	R	R	D	D
+2	1	0	0	1	1	1	0	0	R	F	D	C
+1	0	1	0	1	1	1	0	0	F	F	C	C
+0	0	1	0	1	1	0	1	0	F	F	C	C
-0	0	1	0	1	0	1	0	1	F	F	C	C
-1	0	1	0	1	0	0	1	1	F	F	C	C
-2	1	0	0	1	0	0	1	1	R	F	D	C
-3	1	0	1	0	0	0	1	1	R	R	D	D

B. Operation Principle

Operation of the introduced 7-level inverter with charge and discharge cycles of capacitors at each generated voltage level is given in Fig. 2. Switching operation of switches S_1, S_2, and switches S_3, S_4 are complementary which simple control. The switches in the flow path are marked in red colour in Fig. 2.

Mode 1: In this mode, both switches S_2 and S_4 are on, causing the capacitors to be charged equally using the source as the current flows through the diodes. The output voltage at the "*E*" terminal equals the source voltage level (Fig. 2(a)).

Mode2: Switches S_1 and S_4 are on in this mode that keeps capacitor C_2 charged. Due to the capacitor C_1 being in series with the V_{in}, voltage level of $2V_{in}$ is generated in terminal *E* (Fig. 2(b)).

Mode 3: This mode involves connecting capacitors C_1 and C_2 in series with V_{in} and discharging them to generate voltage level $3V_{in}$ in terminal by turning on switches S_1 and S_3 (Fig. 2(c)).

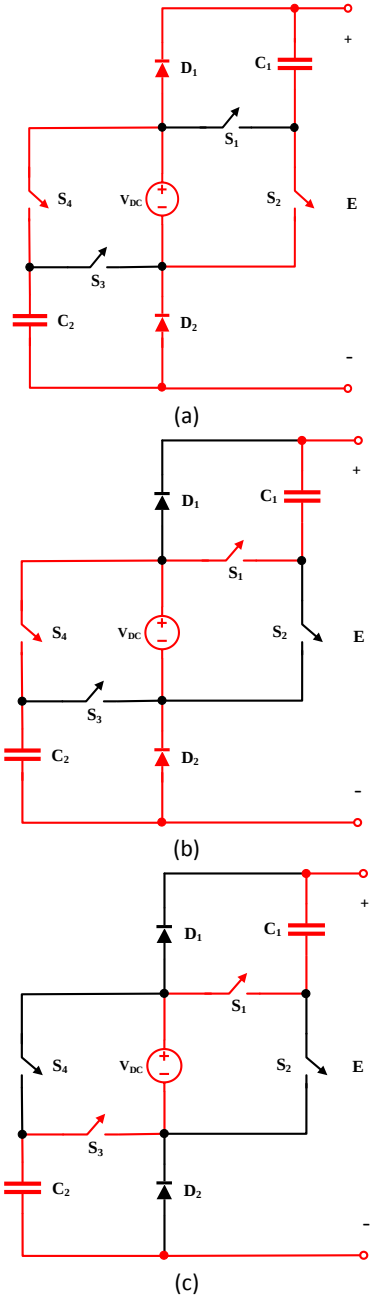


Fig. 2: Equivalent circuits of proposed inverter for each output voltage level, (a) mode 1, (b) mode 2, (c) mode 3.

C. Voltage Stress Analysis

Table 2 presents voltage stress of semiconductor elements applied in the 7-level configuration. Also, Fig. 3 illustrates TSV values of the diodes and switches. It indicates that switches S_1-S_4 have the same voltage stress, equals to V_{dc}. On the other hand, switches Q_1-Q_4, which forms the H-bridge in the output, bears varying voltage stress in each step, with the maximum voltage stress of $3V_{dc}$. TSV of the proposed 7-level configuration is obtained as given in the following:

$$TSV = 4 \times V_{dc} + 4 \times 3V_{dc} = 16V_{dc} \quad (1)$$

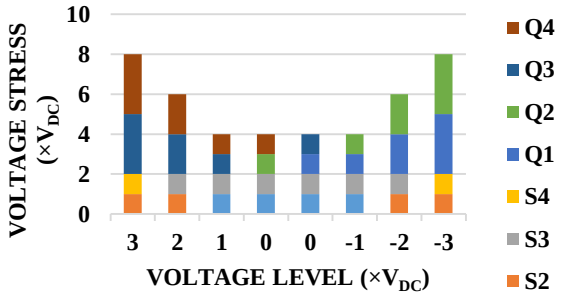


Fig. 3: Voltage stress of switches in the suggested 7-level topology.

Table 2: Circuit elements states for 9-level topology operation

$\frac{V_o}{V_{in}}$	Switch and diode state													Capacitor state		
	S_1	S_2	S_3	S_4	S_5	S_6	Q_1	Q_2	Q_3	Q_4	D_1	D_2	D_3	C_1	C_2	C_3
+4	1	0	1	0	0	1	1	1	0	0	R	R	R	D	D	D
+3	1	0	0	1	1	0	1	1	0	0	R	R	F	D	D	C
+2	1	0	0	1	0	1	1	1	0	0	R	F	F	D	C	C
+1	0	1	0	1	0	1	1	1	0	0	F	F	F	C	C	C
+0	0	1	0	1	0	1	1	0	1	0	F	F	F	C	C	C
-0	0	1	0	1	0	1	0	1	0	1	F	F	F	C	C	C
-1	0	1	0	1	0	1	0	0	1	1	F	F	F	C	C	C
-2	1	0	0	1	0	1	0	0	1	1	R	F	F	D	C	C
-3	1	0	0	1	1	0	0	0	1	1	R	R	F	D	D	C
-4	1	0	1	0	0	1	0	0	1	1	R	R	R	D	D	D

Extended Topology

A. Extended 9-Level Topology

As mentioned before, using multiple DC sources to get more levels in the output voltage is one of demerits of the multilevel inverters. However, in the extended topology of the suggested multilevel inverter, increasing the output voltage levels to 9 with only one DC sources is provided as demonstrated in Fig. 4. The introduced topology uses only one more capacitor, one more diode, and two additional switches compared to 7-Level topology, which increases the output voltage up to 4 times the input voltage. The switching modes for 9-Level topology are described in Table 2.

B. Extended 11-Level Topology

Fig. 5 illustrates 11-level topology of suggested multilevel inverter that is constructed by adding capacitor C_4, diodes D_4 and D_5, and switch S_7 compare to 9-level topology. This configuration increases the output voltage up to 5 times the input voltage with only one DC voltage source. The 11-level topology switching algorithm is listed in Table 3.

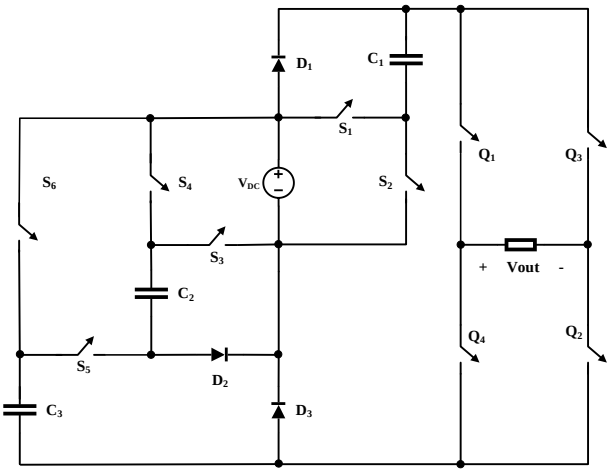


Fig. 4: Extended 9-level topology.

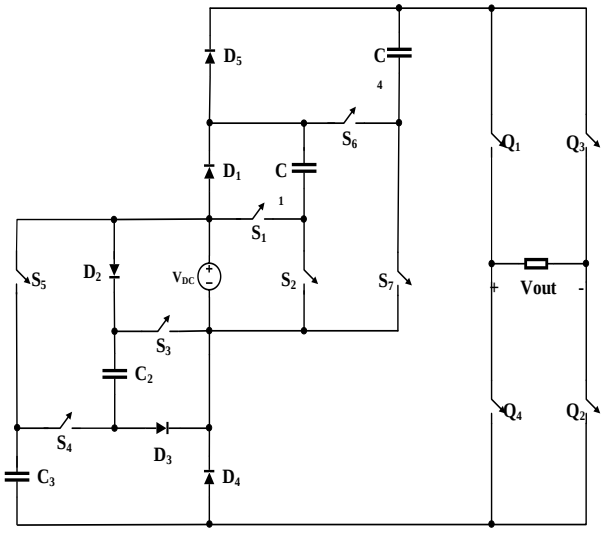


Fig. 5: Extended 11-level topology.

Capacitors Size Calculations

To determine the optimum value of capacitors, it is necessary to calculate the longest discharge period (LDP) for a given capacitor per switching cycle. During the LDP, the reserved energy within the capacitors is released and transferred to the load, resulting in generation of a specific voltage level. The LDP amounts for capacitors C_1 and C_2 are presented in Fig. 6, as indicated by the data given in Table 1.

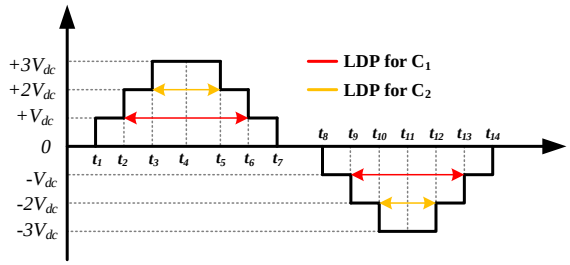


Fig. 6: LDP of capacitors.

Table 3: Circuit elements states for 11-level topology operation

$\frac{V_o}{V_{in}}$	Capacitor state																			
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	Q_1	Q_2	Q_3	Q_4	D_1	D_2	D_3	D_4	D_5	C_1	C_2	C_3	C_4
+5	1	0	1	1	0	1	0	1	1	0	0	R	R	R	R	R	D	D	D	D
+4	1	0	0	0	1	1	0	1	1	0	0	R	R	R	R	F	D	D	D	C
+3	1	0	0	1	0	1	0	1	1	0	0	R	R	R	F	F	D	D	C	C
+2	0	1	0	1	0	1	0	1	1	0	0	R	F	F	F	F	D	C	C	C
+1	0	1	0	1	0	0	1	1	1	0	0	F	F	F	F	F	C	C	C	C
+0	0	1	0	1	0	0	1	1	0	1	0	F	F	F	F	F	C	C	C	C
-0	0	1	0	1	0	0	1	0	1	0	1	F	F	F	F	F	C	C	C	C
-1	0	1	0	1	0	0	1	0	0	1	1	F	F	F	F	F	C	C	C	C
-2	0	1	0	1	0	1	0	0	0	1	1	R	F	F	F	F	D	C	C	C
-3	1	0	0	1	0	1	0	0	0	1	1	R	R	R	F	F	D	D	C	C
-4	1	0	0	0	1	1	0	0	0	1	1	R	R	R	R	F	D	D	D	C
-5	1	0	1	1	0	1	0	0	0	1	1	R	R	R	R	R	D	D	D	D

Time t_i is the transit time between two levels with different values.

According to Fig. 6, it can be concluded that LDP for capacitor C_1 is equal to (t_2-t_6) or (t_9-t_{13}), and for capacitor C_2 is equal to (t_3-t_5) or (t_{10}-t_{12}).

During LDP, the amount of charge transferred from capacitors C_1 and C_2 (Q_{C1}, Q_{C2}) is calculated as given in (2).

$$Q_{C_1} = 2 \times \int_{t_2}^{t_4} i_o(t)dt \quad ; Q_{C_2} = 2 \times \int_{t_3}^{t_4} i_o(t)dt \qquad (2)$$

where i_O is the load current or the capacitor discharge current during the LDP. Considering the specific capacitor ripple voltage (σ), the optimum capacitance for C_1 and C_2 is obtained from (3).

$$C_1 \geq \frac{Q_{C_1}}{\sigma \times V_{dc}} \quad ; C_{12} \geq \frac{Q_{C_2}}{\sigma \times V_{dc}} \qquad (3)$$

For resistive load, i_O in LDP is determined as given in the following:

$$i_o(t) = \begin{cases} 2\frac{V_{dc}}{R}; & for \ \ t_2 \leq t < t_3 \\ 3\frac{V_{dc}}{R} \ ; & for \ \ t_3 \leq t < t_4 \end{cases} \qquad (4)$$

Transit times t_2, t_3, and t_4 are obtained from (5) considering modulation with fundamental switching frequency and unit modulation index.

$$t_2 = \frac{\sin^{-1}(1/2)}{2\times\pi\times f};\ \ t_3 = \frac{\sin^{-1}(5/6)}{2\times\pi\times f};\ \ t_4 = T \quad (5)$$

where f is the switching frequency, and T represents the periodicity of the output voltage, by using (2)-(5). The optimum value of capacitance is calculated as determined in the following:

$$C_1 \geq \frac{2.67}{\pi\times f\times\sigma\times R};\ \ C_2 \geq \frac{1.76}{\pi\times f\times\sigma\times R} \quad (6)$$

Power Loss Calculations

The dominant power losses related to the introduced inverter are; a) conductive losses of switches, diodes, and capacitors; and b) voltage ripple losses of capacitors.

As mentioned before, the suggested inverter is modulated with a low switching frequency so, the switching loss is negligible. However, the conductive loss is calculated by considering on-state resistance of the switches, r_{on}, and diode, r_d, and the equivalent series resistance of capacitors, r_c. Conduction loss, $P_{cond.i}$, for the i^{th} voltage level is obtained as given in (7).

$$P_{cond.i} = r_{eq.i} \times i_{o.i}^2 \quad (7)$$

where $r_{eq.i}$ is the equivalent series resistance in the charging path of the output current and i_{oi} is the load current for the i^{th} voltage level. Because the i^{th} voltage level is repeated 4 times in each switching cycle, the average of conduction loss per cycle is calculated as given in the following:

$$P_{cond.ave.i} = \frac{4(t_{i+1}-t_i)}{T} P_{cond.i} \quad (8)$$

where (t_i+1 - t_i) is the time interval of the i^{th} voltage level. Similarly, for each voltage level, the average conduction loss of the inverter switches should be calculated.

The summation of conduction losses serves as an estimation for the overall power loss incurred by the inverter.

Ripple losses of capacitor manifest during the charge phase of the capacitor. The magnitude of the loss is contingent upon the variation between the input voltage and the instantaneous voltage across the capacitor during the charging process, as well as the capacitance value.

The equation representing the losses for the j^{th} capacitor is depicted in (9). The expression (t_j+1 - t_j) represents the duration of the charging time, while $iC_j(t)$ denotes the charging current of the j^{th} capacitor. The total ripple losses of the inverter are determined by the summation of the ripple losses of all capacitors that are utilized.

$$P_{rip.j} = \frac{1}{2T} C_j \left[\Delta V_{C_j}\right]^2 = \frac{1}{2T} C_j \left[\int_{t_j}^{t_{j+1}} i_{C_j}(t)dt\right]^2 \quad (9)$$

Therefore, total power loss of the inverter is obtained as given in the following:

$$P_{total} = P_{cond.ave} + P_{rip.j} \quad (10)$$

Comparative Analysis

This section presents a comprehensive comparative study among the proposed topologies and several recently discovered SC-based multilevel inverters. The study highlights the distinctive advantages and disadvantages of the proposed topologies, providing robust evidence to support the superiority of the suggested topologies over other competing alternatives. In Table 4, a comparison is performed by considering items such as number of voltage sources (N_{dc}), diodes (N_D), capacitors (N_C), and switches (N_{SW}), as well as the boost factor (BF) and TSV of all switches. In addition, a general comparison of the topologies introduced in [22]-[30] has been included in Fig. 7.

According to comparison results, proposed 7-level topology, despite having a boost factor equal to [22], requires fewer switches due to the reduced number of gate drivers. As a result, it costs less and is considered superior to other topologies.

In the configuration proposed in [23], there are more passive elements, and TSV on the switches is also high in compared with suggested 7-level topology. The values of N_D, N_C, and BF are the same in both proposed 7-level and [24] configurations. Additionally, the voltage stress on the switches in [24] is higher than proposed 7-level topology.

Compared to the topologies introduced in [25]-[27], the suggested 9-level topology has less voltage stress and fewer passive elements than [25]-[27] topologies.

Table 4: Comparative analysis of proposed topologies with similar SC-MLI

Top	N_L	N_{dc}	N_{SW}	N_D	N_C	BF	TSV
[22]	7	1	10	-	2	3	4.33
[23]	7	1	6	4	4	3	6
[24]	7	1	8	2	2	3	6
[25]	9	1	8	6	3	4	6
[26]	9	1	13	3	3	4	5.25
[27]	9	1	17	4	4	4	12.25
[28]	11	1	14	2	3	2.5	3
[29]	11	1	11	5	4	5	6.6
[30]	11	1	17	1	5	5	7.14
[7-Level topology]	7	1	8	2	2	3	5.33
[9-Level topology]	9	1	10	3	3	4	5.5
[11-Level topology]	11	1	11	5	4	5	5.4

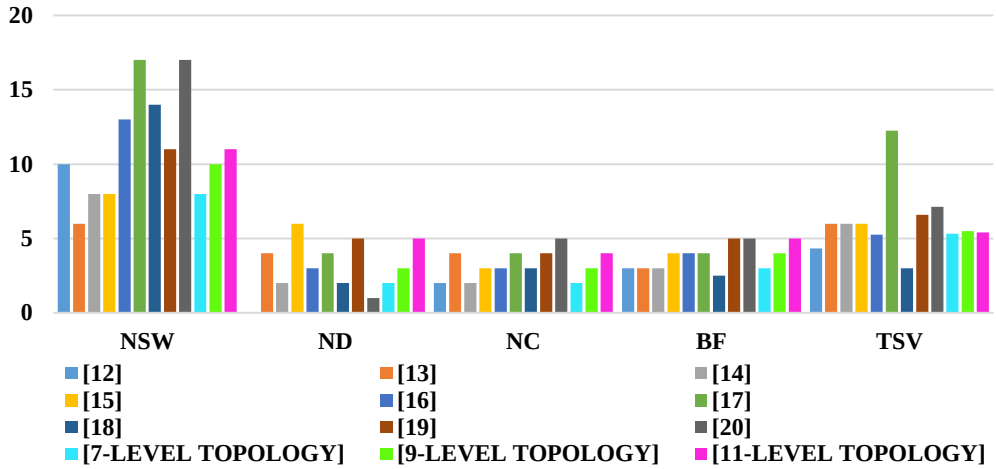


Fig. 7: Comparative analysis chart.

All these factors make proposed 9-level topology superior to the others. The topology given in [26] has lower voltage stress than proposed 9-level topology however, its demerit is applying more switches.

Although, the topology suggested in [28] has more switches than proposed 11-level topology, it has lower boost factor.

On the other hand, the topology introduced in [29] has same switches and diodes in compared to proposed 11-level topology, but it has more TSV. Despite, the combination of lower N_{SW}, N_C and TSV make the given 11-level topology superior to the topology suggested in [30].

Results and Discussion

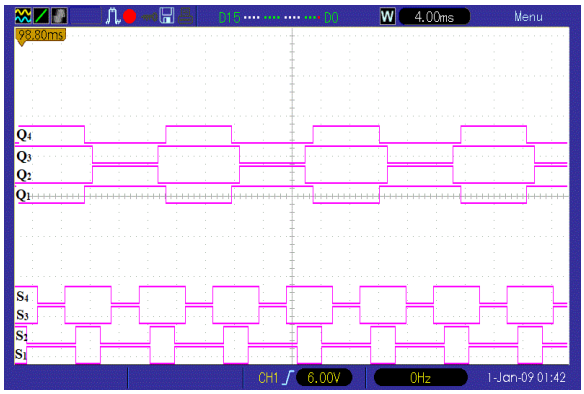
To verify practicability of the introduced topologies, a 7-level topology experimental prototype is implemented as depicted in Fig. 8. Table 5 lists the elements were employed in the laboratory prototype.

Fig. 8: Hardware setup

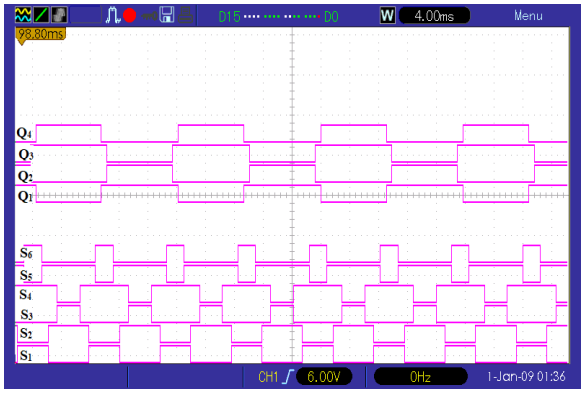
Table 5 Prototype circuit elements values

Parameter	value
Input DC sources	V_{dc}=30 V
MOSFETs type	IRFP260n
Output frequency	f_o=50 Hz
Opto-coupler	TLP250
Capacitances	4700µf
Load	R=100Ω, L=50mH
Microcontroller	Atmega8a

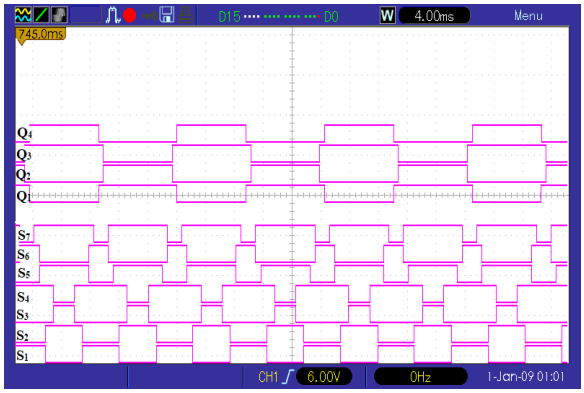
Atmega8a microcontroller is utilized to generate the gate signals of the implemented inverter switches that is shown in Fig. 9. Fig. 10(a)-(c) display the voltage and current waveforms of the resistive-inductive load (100Ω - 50 mH), respectively. The DC source has the value of 30 volts, consequently, the output voltage range is some lower than theoretical value due to losses incurred by the switches and diodes. The output current in Fig. 10 exhibits a sinusoidal waveform due to the presence of an inductive load within the circuit. Fig. 11 shows dynamic operation of the 11-level topology during load change from resistive-inductive to resistive. As shown in this figure, the suggested topology response to the load change is without performance failure. Among the proposed topologies, it is noteworthy that capacitor C_1 in 7, 9, and 11-level configurations holds the highest level of significance due to its LDP. Therefore, it is crucial to consider this aspect while deciding on the final configuration. Fig. 12 depicts the maximum voltage of capacitors C_1 in the suggested 11-level topology. The output voltage of the capacitor has a self-balancing profile, which indicates that the capacitors experience minimal ripple.



(a)



(b)



(c)

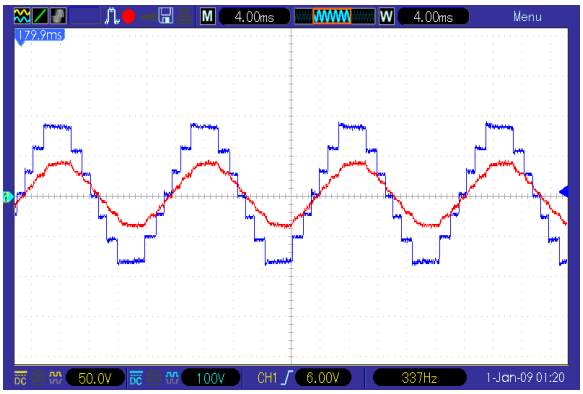
Fig. 9: Gate signals of proposed (a) 7-level, (b) 9-level, and (c) 11-level topologies.

Conclusions

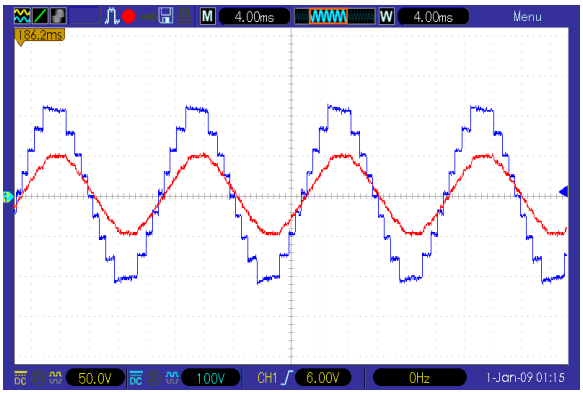
This paper has presented modified switch-capacitor multilevel inverter topologies with 7, 9, and 11 levels in output voltage. All topologies have the potential to be used in renewable energy integration and electric vehicles.

Comprehensive examinations of circuit performance, voltage stress, capacitor sizing, and power loss were presented. The comparative assessments demonstrated that the suggested configurations achieve a greater voltage boost while utilizing fewer elements in comparison to the most advanced solutions available. The experimental test results confirmed the accuracy of the theoretical statements regarding the multilevel output voltage waveforms and the ability to balance capacitor voltages.

Therefore, the suggested SC multilevel inverters show great potential as solutions for applications such as solar photovoltaic systems and electric vehicle battery banks. Subsequent research will highlight the optimization of topologies for particular power ratings and the execution of efficiency tests.



(a)



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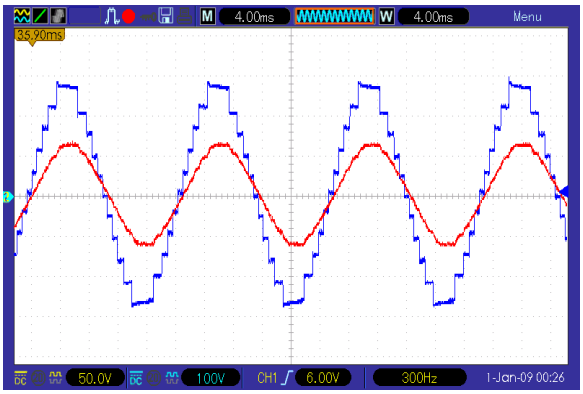


(c)

Fig. 10: Experimental test results; voltage and current waveforms of resistive-inductive load for (a) 7-Level inverter (b) 9-level inverter and (c) 11-level inverter.

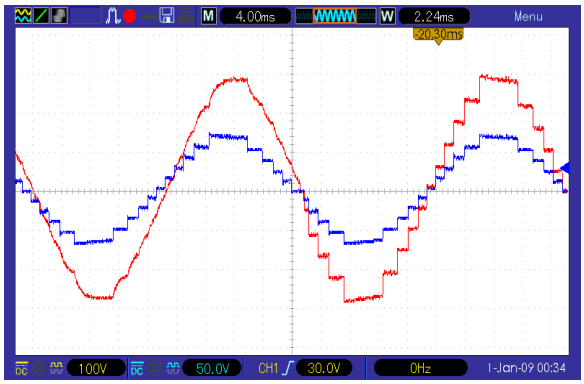
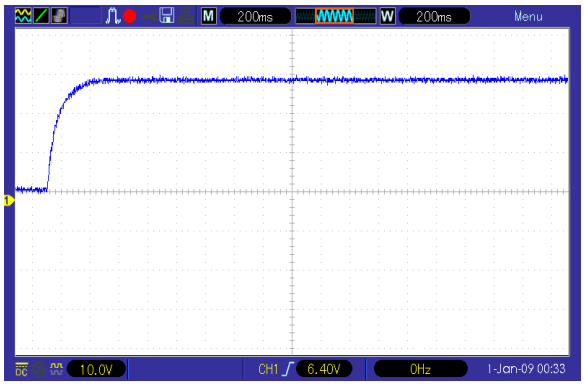
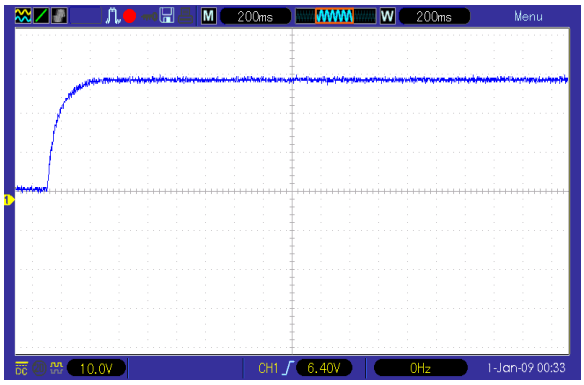


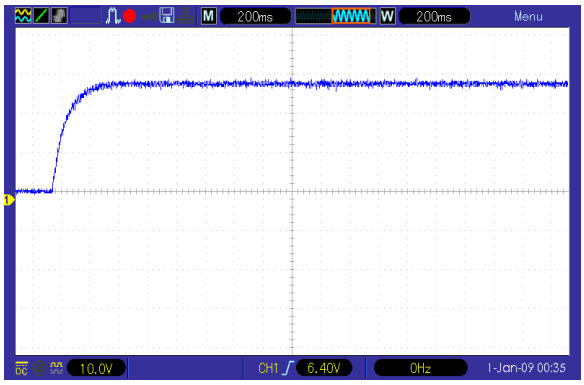
Fig. 11: Experimental test results of voltage and current waveforms for load change from resistive-inductive to resistive.



(a)



(b)



(c)

Fig. 12: Experimental test results of voltage waveforms for Capacitors C1 (a) 7-level topology, (b) 9-level topology, (c) 11-level topology.

Author Contributions

F. Sedaghati chose the field of research. S. Ebrahimzadeh and H. Dolati collected information in this field. F. Sedaghati presented the proposed topology. S. Ebrahimzadeh and H. Dolati simulated and fabricated the proposed converter converter. The authors discussed the obtained results and drew conclusions. Under the supervision of F. Sadaghti, the text of the article was prepared by S. Ebrahimzadeh and H. Dolati. F. Sedaghati submitted the manuscript.

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Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the ethical issues including plagiarism, informed consent, misconduct, data fabrication and, or falsification, double publication and, or submission, and redundancy have been completely witnessed by the authors.

Abbreviations

PV	Photovoltaic
EV	Electric Vehicle
PWM	Pulse Width Modulation
SC	Switched Capacitor
MLI	Multilevel inverter
THD	Total Harmonic Distortion
TSV	Total Standing Voltage
LDP	Longest Discharge Period
BF	Boost Factor

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