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Research paper

Design of Low-Power Flash Time-to-digital Converter Using Transmission Gate-Based D Flip-Flops and Body-Biased Delay Cells

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Abstract

Background and Objectives: A Time-to-Digital Converter (TDC) is a fundamental electronic component that converts time intervals into digital representations. It plays a critical role in high-precision applications such as particle physics experiments, time-of-flight measurements, and the processing of high-frequency signals in communication systems. This paper presents a comprehensive study on the design and simulation of two innovative low-power TDC architectures.

Methods: The approach introduces a novel low-power D Flip-Flop (D-FF) circuit using transmission gates (TG) and CMOS inverters to reduce power consumption while maintaining high performance. Specialized low-power delay cells are proposed for Flash TDC implementation. Detailed simulations were conducted using Cadence software with a 0.18 µm CMOS fabrication process at a supply voltage of 1.8 V.

Results: The results demonstrate significant improvements in power efficiency and performance metrics, indicating the potential of the proposed TDC designs for future applications requiring precise temporal measurements. The Figure of Merit (FOM) values of the two proposed structures are 0.033 and 0.020, respectively.

Conclusion: Power consumption in TDCs is a critical factor, as it directly influences the overall efficiency of electronic systems. Reducing power consumption can lead to decreased energy use, improved thermal management, and an extended lifespan for devices. Conversely, higher power consumption can generate excessive heat, which can negatively impact the system's performance and reliability. Thus, it is vital to strike an optimal balance between accuracy and power consumption in TDCs to enhance the longevity of electronic devices. This paper presents the design of delay cell circuits and a D-FF using a 0.18 µm CMOS process with a 1.8 V supply voltage. The power consumption of the proposed delay cells has been minimized through the application of the body bias technique. The performance of the delay cell has been evaluated in flash TDC circuits, and the results demonstrate the effective performance of the proposed structures.

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Introduction

In the last few decades, CMOS technology is highly regarded due to its high integration capability, simple design and low manufacturing cost. Although reducing the gate oxide thickness of the transistor causes the working voltage of the system to decrease, it becomes difficult to design the analog circuit. This is due to improper bias point operation, low input voltage swing and linearity issues [1]. To mitigate design challenges, the development of time-mode signal processing (TSMP) has been considered [2]. Understanding the relationship between TMSP and converters like voltage-to-time converter (VTC) and time-to-voltage converter (TVC) is essential for grasping their roles in modern signal processing. A VTC converts an input voltage signal into a time-domain representation (such as delay or pulse width). This process is fundamental to TMSP as it enables amplitude-based information to be processed in the time domain. After processing in the time domain, a TVC performs the reverse operation of a VTC. It converts temporal information (such as delay or pulse width) into amplitude-based signals (voltage). In a similar manner, a digital-to-time converter (DTC) transforms a digital signal into a time difference variable. Following the processing in the time domain, a time-to-digital converter (TDC) is utilized to convert the time-based signal back into a digital format. TSMP has found applications in various fields, including positron emission tomography (PET) imaging [3]. It is also utilized in digital oscilloscopes with memory and in radio frequency transceivers [4]. Some applications of TDCs are as follows:

1-Time-of-Flight (TOF): In particle physics, TOF measurements use TDCs to calculate the travel time of particles, which helps in determining their speed and position.

2- LIDAR Systems: TDCs are used in light detection and ranging systems to measure the time it takes for light to return to the sensor.

3- Radar and Ultrasonic Sensors: TDCs are also applied in radar and ultrasonic range finding systems to accurately determine distances based on the time taken for signals to travel.

A TDC can be implemented with timing comparators or the methods described below. The simple counter is the simplest TDC architecture. In this method, the time interval between the rising edges of the start and stop pulses is measured. This measurement is achieved using a counter that is controlled by a reference clock with a high frequency. Flash TDCs function similarly to flash analog-to-digital converters (ADCs) used for voltage encoding, comparing a signal edge against multiple reference edges that are time-shifted. The components responsible for comparing the input signal to the reference are typically D-type flip-flops. A TDC vernier oscillator employs two ring oscillators to produce plesiochronous square waves, enabling time interval quantization based on the slight frequency difference between the oscillators.

The fundamental TDC structure, which utilizes a delay line, consists of delay elements and flip-flops, along with start and stop signals. In this configuration, the start signal is delayed using either an inverter or a buffer element [5], [6]. Likewise, the stop signal undergoes a delay through the delay element. Sampling occurs at the rising edge of the stop signal, enabling the flip-flops to capture the state of the delay line. Ultimately, the output is generated in the form of 0 and 1 [7]. There is ongoing research focused on utilizing the adiabatic approach for designing low-power VLSI circuits [8]. Digital circuits typically exhibit significant power loss, but the adiabatic method offers an efficient solution without adding complexity to the circuit. The term adiabatic refers to the absence of heat exchange with the environment. Adiabatic circuits operate based on the principles of adiabatic charging and discharging [9]. In conventional CMOS circuits, energy is dissipated from the output capacitor to the ground. Conversely, adiabatic logic recycles energy back to the power source [10]. This approach results in greater energy savings compared to traditional logic. Adiabatic logic is also known as energy recovery logic [11], [12].

In this paper, two new low power Flash TDCs are proposed. In the proposed TDCs, two new delay cells based on bulk-driven technique are utilized. In addition, low power D Flip-Flop (D-FF) circuit based on transmission gate (TG) and CMOS inverter is suggested. The next section includes a review of existing works. In the Section 3, the proposed TDCs are explained. Next, the performance of the proposed circuits is assessed, and the comparison results are presented. Finally, to wrap up, the key findings of the research presented will be summarized.

Related Works

In [13], a two-stage TDC based on a ring oscillator is introduced. The TDC provides a total resolution of 8 bits, where 4 bits are derived from coarse conversion and the remaining 4 bits from fine conversion, utilizing time residual amplification. TDC circuit area is equal to 0.34 mm^2 in 180-nm CMOS process. The TDC circuit has demonstrated a resolution of 10.5 ps at a frequency of 50 MHz. In [14], a delay chain architecture is employed as a substitute for the delay line and sample register to minimize circuit area. However, this delay structure is sensitive to mismatches and process variations. In [15], a high-resolution two-stage ADC-based TDC is proposed, but it suffers from significant area and power consumption, as well as a limited dynamic range. A TDC

architecture utilizing cyclic interpolations is proposed in [16], offering high resolution and an extended dynamic range. However, it faces challenges such as high power consumption and low conversion speed. In [17], a low-power, compact time-to-digital converter based on a digital vernier oscillator structure is introduced. Operating with a 1.8V power supply, this TDC achieves a resolution of 100 ps and an average power consumption of 0.8 mW.

In [18], a TDC architecture designed for high-bandwidth radar systems is introduced. Its primary function is to interface RF front-ends with standard microcontrollers, eliminating the need for high-speed, high-precision analog-to-digital converters, high-performance memories, or high-speed logic. Reference [19] presents a vernier delay line TDC designed in a 180-nm CMOS process, offering excellent resolution, making it ideal for low-power, all-digital locked loops and time-mode analog-to-digital converters. In [20], a TDC is proposed in which a single interpolator is used to enhance the resolution through a triple-slope transform. This approach significantly reduces chip area and power consumption compared to the two-parallel time interpolation method, with a measured resolution of 357 ps. Reference [21] introduces a high-resolution, wide-range TDC designed for all-digital phase-locked loops. The multiphase outputs of the Digitally Controlled Oscillator are utilized to sample time differences and extend the detectable time range, while a time amplifier (TA) enhances time resolution.

In [22], an 8-bit TDC utilizing a successive approximation analog-to-digital converter (SAR ADC) architecture is presented. This design converts a time interval into a voltage, which is then input into the SAR ADC for voltage-to-time conversion. In contrast to other SAR ADC implementations, this approach is straightforward and does not necessitate a large quantity of capacitors. Reference [23] discusses various types of successive approximation TDC architectures implemented in the time domain. It also presents several feedback-based architectures optimized for propagation delay and energy efficiency. In [24], a high-speed, high-accuracy voltage-to-time difference converter is introduced. This study focuses on load regulation design to precisely adjust the delay time of the symmetrical delay cell. The circuit, fabricated in the 180-nm CMOS process, shows an 8-bit accuracy and a bandwidth of 250 MHz in simulation results. Reference [25] presents an 8-bit logarithmic analog-to-digital converter, which consists of two conversion elements. One element is a TDC with a linear transfer characteristic, and the other is a voltage-to-time converter (VTC) with a logarithmic transfer characteristic, constructed using two cross-connected inverters. Simulation results in the 130-nm CMOS process demonstrate the high efficiency of this design.

Proposed Method

Delay cells based on nonlinear current mirrors [26]-[28] and D-FF circuits are used in the structure of TDCs, and the design and analysis are presented below.

Proposed Delay Cells

The delay cell can be considered as one of the main elements in the TDC. The solution presented in this paper is to use the body bias shown in Fig. 1.

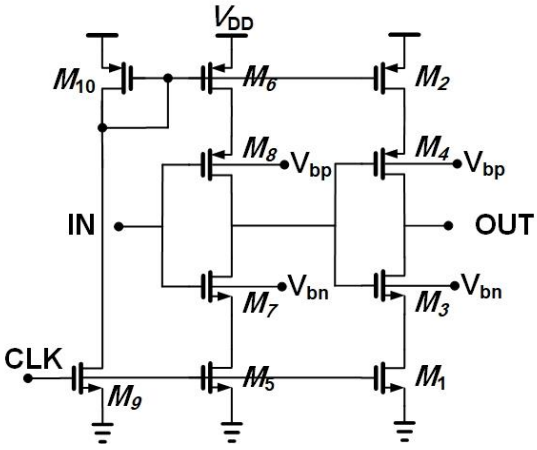


Fig. 1: Schematic of the first proposed low-power delay cell utilizing body biasing. The use of body bias significantly reduces the threshold voltage, thereby lowering the power consumption compared to conventional delay cell.

When a voltage is applied to the body (bulk) terminal of a MOSFET, it influences the threshold voltage (V_T) due to the body effect. This effect leads to a modification in the threshold voltage as a function of the voltage difference between the source and the body, V_{SB}, and is particularly important for devices operating in analog and mixed-signal circuits. The threshold voltage of a MOSFET (whether NMOS or PMOS) varies as the source-to-body voltage changes. This effect is caused by changes in the depletion region width at the semiconductor-substrate interface, which in turn affects the channel conductance. For NMOS transistors, the relationship between threshold voltage and the source-to-body voltage is given by [29], [30]:

$$V_T = V_{T0} + \gamma\left(\sqrt{2|\varphi_F| + V_{SB}} - \sqrt{2|\varphi_F|}\right) \quad (1)$$

where V_{T0} is the threshold voltage at zero bulk source voltage, φ_F is the Fermi potential, γ is the body effect coefficient. V_{SB} is the source-to-body voltage, which, in the case of NMOS, is typically negative, and for PMOS would be positive if the body is tied to the source. For PMOS transistors, the equation is similar, but the sign conventions change to accommodate the negative

threshold voltages of PMOS devices.

When a positive V_{SB} is applied to an NMOS transistor (or negative for PMOS), the depletion region at the junction between the p-type substrate and the n-type source and drain widens. This increases the channel resistance and reduces the current conduction capability, effectively increasing the threshold voltage. This means that more voltage is required to turn the transistor on, compared to the case when (V_{SB} = 0).

The body bias technique offers several advantages over adaptive biasing and sub-threshold operation. It provides more precise control over the threshold voltage of transistors, improving energy efficiency without significantly affecting performance speed. Additionally, it maintains better performance at higher frequencies, whereas other techniques may suffer from speed reduction and increased delay. Body bias also results in lower design complexity, as it can be optimized with a simpler setup compared to the more complex adaptive biasing and sub-threshold methods. Moreover, it consistently reduces power consumption without the need for continuous adjustments, unlike adaptive biasing, which requires constant tuning.

In Fig. 1, (M3 and M4) and (M7 and M8) are organized as CMOS inverters. V_{bn} and V_{bp} are applied to the body terminals of inverters to reduce the threshold voltage of the transistors. The voltages should be carefully optimized to achieve an optimal trade-off between speed and power consumption. The clock signal, with the help of (M1, M5, M9), controls the activation and deactivation of the circuit. This feature is especially important in low-power designs. The transistors (M2, M6, M10) serve as active loads. The cell delay is calculated as follows. Based on the circuit structure, the main signal path from IN to OUT consists of two cascaded inverters (M3-M4 and M7-M8) with active load and current source transistors affecting the switching speed. The propagation delay of a standard CMOS inverter can be approximated as:

$$t_p \approx 0.69 \times R_{eq} \times C_{eq} \tag{2}$$

where t_p is the propagation delay, R_{eq} is the equivalent resistance of the cell and C_{eq} is the equivalent capacitance. Thus, the total delay is:

$$t_{p-total} \approx 2 \times 0.69 \times R_{eq} \times C_{eq} \tag{3}$$

The second proposed delay cell structure is shown in Fig. 2. This structure has some differences compared to Fig. 1. In the structure of the delay cell, two flipped voltage follower consisting of a set of transistors (M5, M9, M11) and (M6, M10, M12) are used, which act as nonlinear current mirrors [26]-[28]. The nonlinearity of the current mirror leads to an arbitrary amplification of the output current.

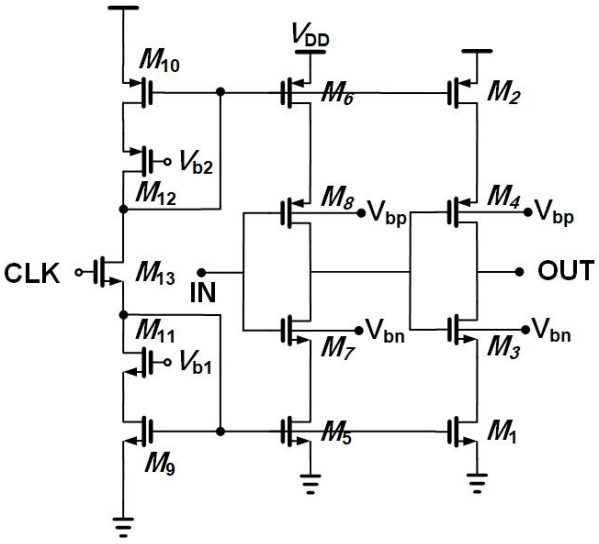


Fig. 2: Second proposed delay cell structure using flipped voltage followers as nonlinear current mirrors with body biasing technique.

Transistor M13 acts as a current reference and CLK is applied to its gate terminal. If the voltage Vb1 is chosen so that the transistor M9 is in the triode region, then the following relations can be presented:

$$I_1 = \frac{1}{2}\beta_5 V_{od5}^2 \tag{4}$$

$$I_2 = \beta_9 V_{od9} V_{DS9} \tag{5}$$

In the relations above $\beta = \mu_n C_{ox}\frac{W}{L}$, V_{od} represents the overdrive voltage. μ_n is electron mobility in the channel, C_{ox} is the capacitor per unit of gate area, W is the width of the transistor channel, and L is the length of the transistor channel. Assuming $\beta_5 = \beta_9$ and using the above relations, we have:

$$I_1 = \frac{I_2^2}{2\beta_5 V_{DS9}^2} \tag{6}$$

Considering that $V_{DS9} = V_{b1} - V_{tn} - V_{od11}$ where V_{tn} is the threshold voltage, relation (6) is expressed as follows.

$$I_1 = \frac{I_2^2}{2\beta_5 (V_{b1} - V_{tn} - \sqrt{\frac{2I_2}{\beta_{11}}})^2} \tag{7}$$

Equation (7) shows that the relationship between I1 and I2 is nonlinear. Nonlinear current sources can provide a broader output current range compared to linear sources. This is attributed to the nonlinear characteristics of the circuits, enabling the output current to attain higher values under varying operating conditions.

Proposed D-FF

The D-FF structure, as depicted in Fig. 3, utilizes two

CMOS inverters and a TG. A TG is a combination of an N-MOSFET and a P-MOSFET, and it is designed to allow signals to pass through it more effectively than a single transistor.

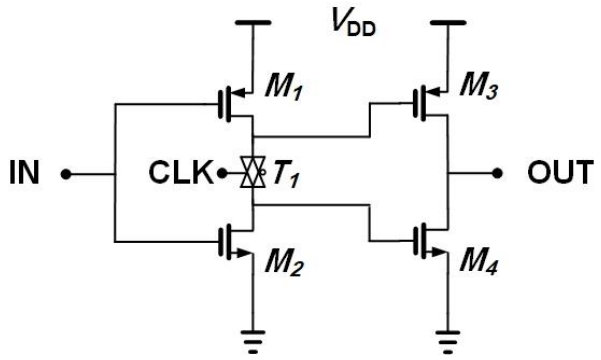


Fig. 3: The proposed D-FF.

A TG uses both P-MOS and N-MOS transistors simultaneously. When the input is logical "1", the P-MOS turns on, and when the input is logical "0", the N-MOS turns on. This dual control allows the TG to pass both logical low (0) and high (1) signals more efficiently, unlike single transistor gates that have limitations in passing specific logic levels. The TGs are particularly useful in digital circuit designs, such as multiplexers, logic reversals, and analog-to-digital converters (ADCs), where accurate signal passing (both "1" and "0") is required. This is an innovative design for a D-FF using a transmission gate (T1) and two CMOS inverters (M1, M2 and M3, M4). Here's a detailed explanation of its operation:

The transmission gate (T1) functions as a pass switch controlled by the clock signal (CLK). When the clock is active, the transmission gate allows the input signal (IN) to propagate to the output of the first inverter. M1 and M2 form a CMOS inverter that inverts the signal coming from the transmission gate. The second inverter, formed by M3 and M4, takes the inverted signal from the first inverter and inverts it again, effectively restoring the original signal at the output (OUT). This design ensures correct latching and signal propagation, following the clock's control. Its simplicity and efficiency make it suitable for high-speed and low-power applications.

The Latch state in this circuit is achieved because, when CLK changes, the input signal (IN) only propagates to the output if the transmission gate T1 is active. If the transmission gate is not active, the circuit holds its stable state, and the output (OUT) remains constant, even if the input changes. Here are some key points about the design:

1. Simplicity and Efficiency: The design uses a relatively small number of basic components (a transmission gate and inverters), which helps reduce the circuit complexity and, consequently, lowers power consumption. This is particularly beneficial in VLSI designs and digital systems that need power optimization.

2. Accurate Operation: The use of the transmission gate and CMOS inverters ensures stable and precise operation of the D-FF. The transmission gate acts as a switch, allowing the input to propagate to the output when the CLK signal is active. This design could be very useful in synchronous switching circuits and data transfer applications.

3. Power and Speed Benefits: Since CMOS is used for the inverters, the design naturally offers low power consumption and high speed. These features are highly valuable in applications where energy efficiency and performance are crucial.

The reduced power and delay characteristics of the D-FF directly enhance TDC precision. The Flash TDC benefits from faster response times and lower power consumption, making it suitable for high-speed, low-power applications such as time-of-flight sensors and high-frequency signal processing.

The proposed delay cell is used in the 8 bits flash time-to-digital converter as shown in Fig. 4 [31]. The elements in flash time-to-digital converter compare the input signal to the reference D-type flip-flops. Each buffer generates a delay equal to τ. The D-type flip-flop structure used in the converter is shown in Fig. 3.

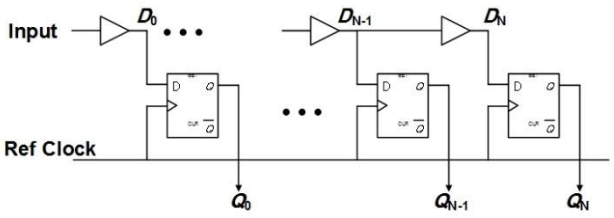


Fig. 4: Flash time-to-digital converter.

Simulation Results

A series of simulations are conducted to evaluate the performance of the proposed method. The delay cells and the D-FF design are implemented in a 0.18 µm CMOS process, operating at a supply voltage of 1.8V, and are simulated using Cadence software. The transistor dimensions are as follows: the NMOS transistor has a width of 1.5µm and a length of 0.18µm, while the PMOS transistor has a width of 3.6µm and a length of 0.18µm.

Parametric simulation in Cadence Virtuoso is used to analyze the impact of varying circuit parameters on its performance. In this simulation, parameters such as bias voltages can be altered to observe the circuit's response. This is done using the Analog Design Environment, where parameters are defined as variables, and simulations like Monte-Carlo can be performed to evaluate the effects of

parameter variations.

Fig. 5 shows the power consumption curve of the first delay cell as well as that of another circuit without using the body biasing technique.

It can be seen from the figure that the proposed structure consumes lower power compared to the conventional structure.

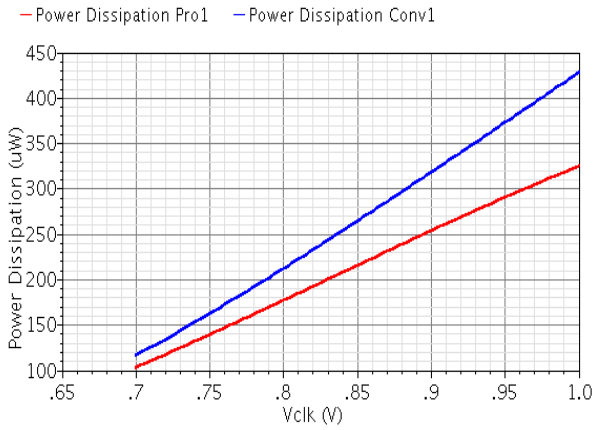


Fig. 5: Power consumption of the first delay with the application of the body biasing technique and then without it.

The power consumption of the second proposed delay cell using nonlinear current sources and the body biasing technique is illustrated in Fig. 6. The nonlinear behavior is clearly evident in this figure. Additionally, the effectiveness of the body biasing technique is also apparent.

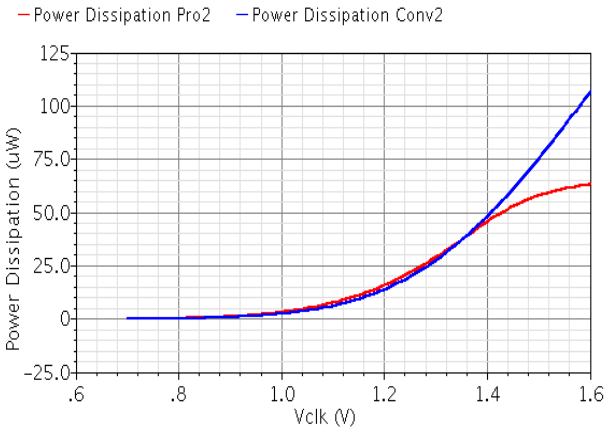


Fig. 6: Power consumption of the second delay with the application of the body biasing technique and then without it.

Monte-Carlo analysis has been performed for both proposed delay cells. The Monte-Carlo simulation of power consumption is plotted with 1000 runs. The mean power consumption of the first delay cell in the Fig. 7(a) is 104.1 µW, and the variance is 3.9 µW. The power consumption in the FF (-40°C) and SS (90°C) corners is 114.5 µW and 94.7 µW, respectively.

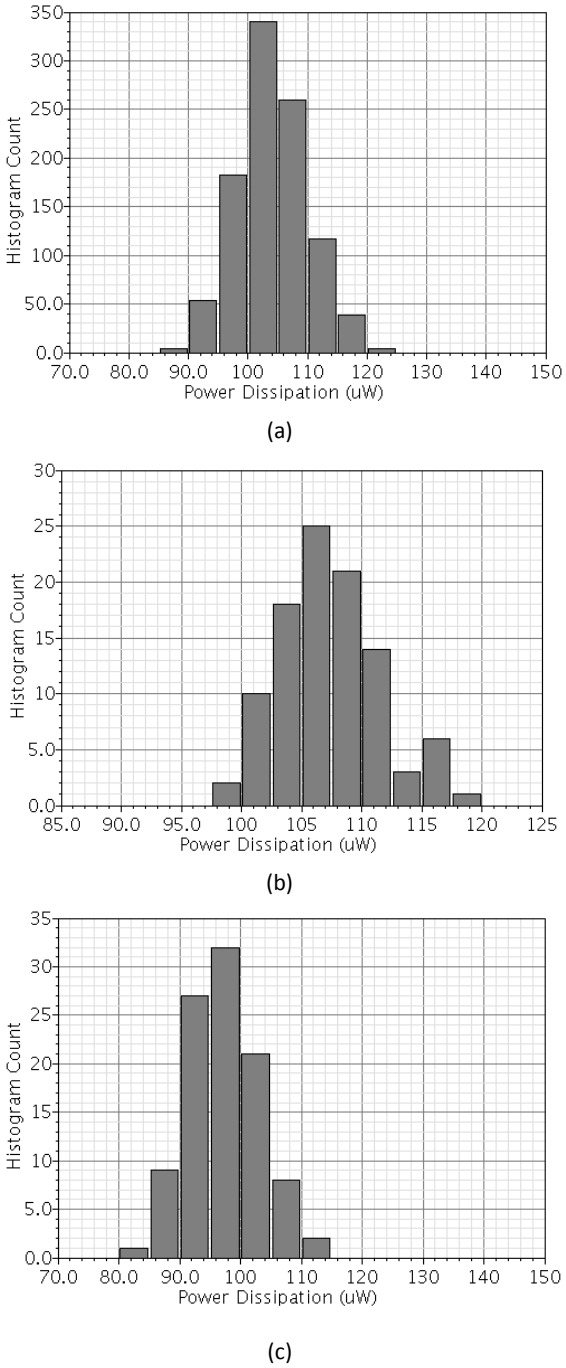


Fig. 7: Monte-Carlo Simulation Histogram Showing Power Consumption Variations in the First Delay Cell. (a) TT (27°C), (b) FF (-40°C), (c) SS (90°C).

For the second delay cell, the mean and variance are 63.3 µW and 2.9 µW, respectively which is shown in the Fig. 8(a).

At the FF corner (-40°C), the power consumption is 70.3 µW, while at the SS corner (90°C), it is 58.2 µW. The results are also summarized in Table 1. The layout of the delay cells is depicted in Fig. 9. The layout area of the first delay cell is 10µm×15µm. For the second delay cell, the layout area is 11µm×17µm.

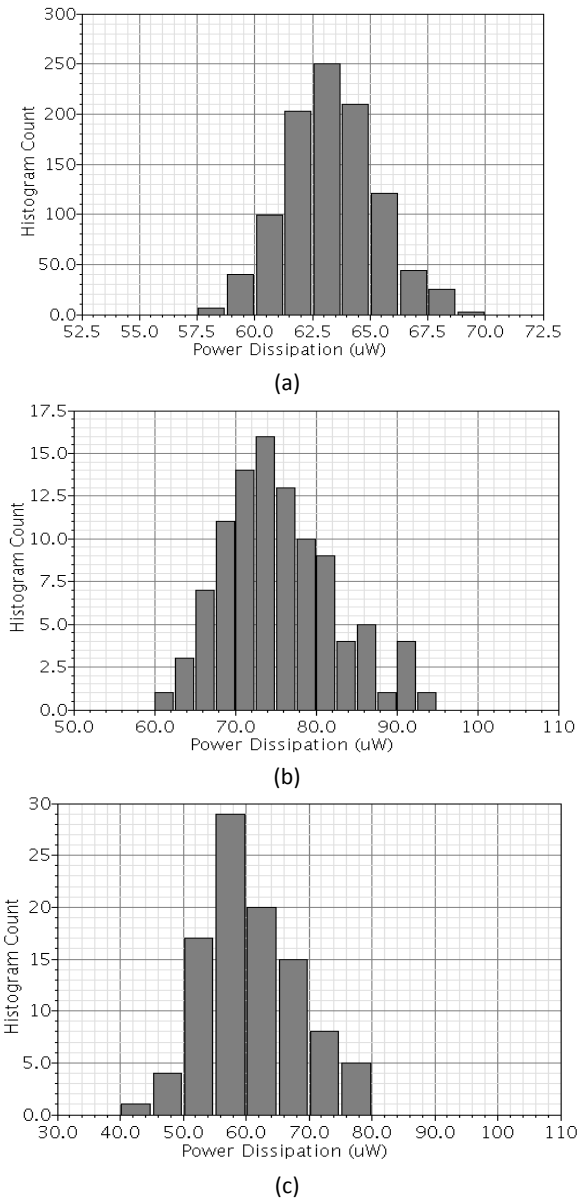


Fig. 8: Monte-Carlo Simulation Histogram Showing Power Consumption Variations in the Second Delay Cell. (a) TT (27°C), (b) FF (-40°C), (c) SS (90°C).

Table 1: Monte-Carlo analysis of power consumption for the proposed delay cells

	Mean Value (µW)	Standard Deviation (µW)
First Delay Cell at TT (27°C)	104.1	3.9
First Delay Cell at FF (-40°C)	114.5	4.1
First Delay Cell at SS (90°C)	94.7	3.8
Second Delay Cell at TT (27°C)	63.3	2.9
Second Delay Cell at FF (-40°C)	70.3	3.0
Second Delay Cell at SS (90°C)	58.2	2.8

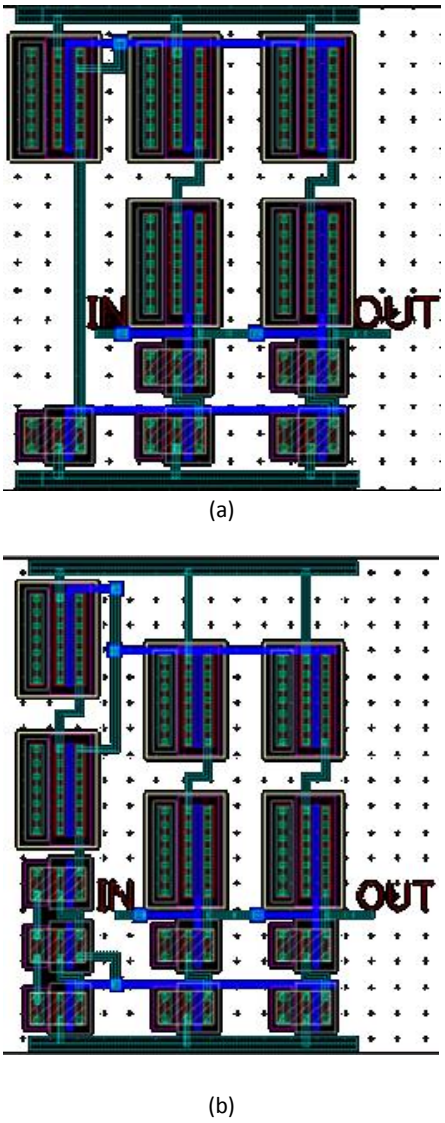
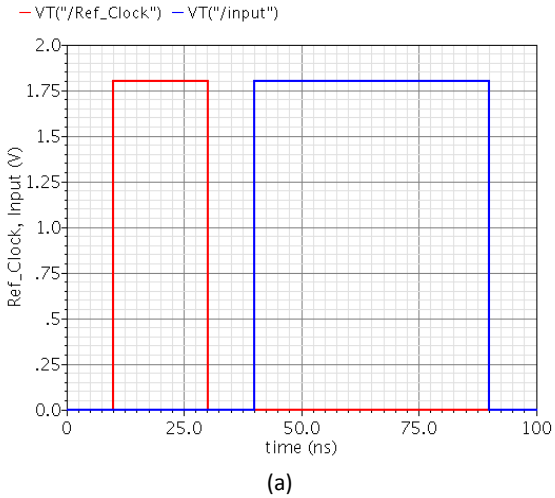
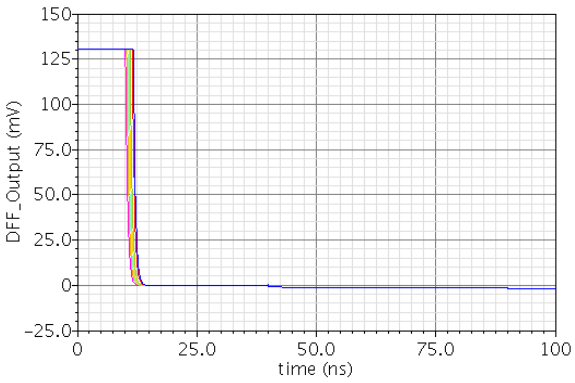


Fig. 9: Layout Design of the Delay Cells. (a) First Delay Cell, (b) Second Delay Cell.

Fig. 10 shows an example of TDC function using the first delay cell and the proposed D-FF. Since the Ref_Clock is zero on the rising edge of the input, all output values are zero.

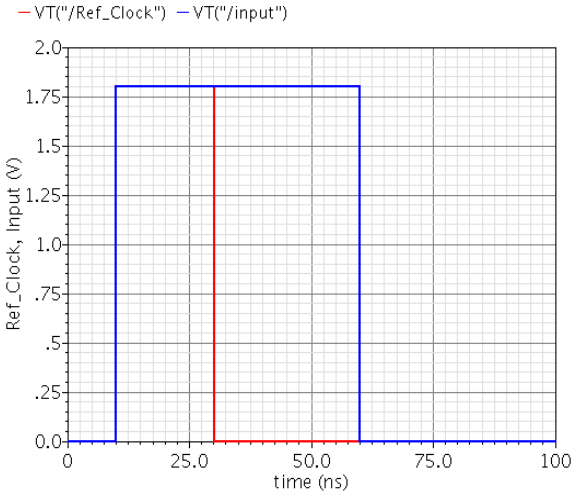




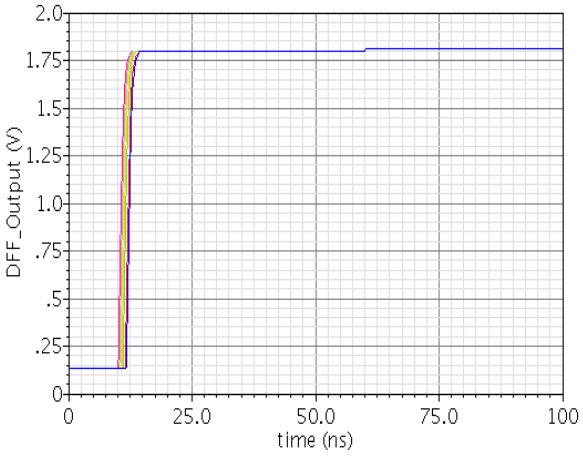
(b)

Fig. 10: (a) Ref_Clock is zero on the rising edge of the input, (b) TDC output.

However, in Fig. 11, at the rising edge of the input, the Ref_Clock is '1', and therefore all output values are '1'. Table 2 presents the post-layout comparison parameters among the proposed TDCs and other existing circuits.



(a)



(b)

Fig. 11: (a) Ref_Clock is '1' on the rising edge of the input, (b) TDC output.

Table 2: Comparison parameters of the proposed TDCs and other existing circuits

	TDC1	TDC2	[2]	[5]	[6]	[16]	[19]
Technology	0.18 µm	0.18 µm	65 nm	65 nm	65 nm	0.35 µm	0.18 µm
Supply Voltage (V)	1.8	1.8	1.2	1.2	1.2	3.3	0.6
Bits	8	8	8	9	8	13	6
Frequency (MHz)	100	100	60	150	80	0.8	50
FOM (pJ/conv)	0.033	0.020	0.85	0.108	0.328	102.3	0.166

The proposed TDCs have better Figure of Merit (FOM) compared to the other methods. The FOM is expressed as follows [5]:

$$FOM = \frac{Power}{Freq \times 2^N} \tag{8}$$

where power represents the power consumption of the TDC, *N* denotes the number of bits of the TDC, and Freq refers to the operating frequency of the TDC. A lower FOM indicates better performance, as it reflects reduced power consumption for a given frequency and bit resolution. This improvement is evident in our cells, where the FOM shows a more efficient design in terms of power consumption and frequency.

Finally, the scalability of the proposed TDCs to smaller CMOS nodes, such as 65nm and 45nm, is discussed here. As the technology node shrinks, the overall power consumption can be further reduced due to lower supply voltages and smaller transistor sizes. However, challenges such as increased process variations and noise sensitivity may arise. The body bias technique, employed in our design, can help mitigate some of these issues by providing a mechanism to adjust the threshold voltage, thus improving the robustness of the TDCs in smaller nodes.

Conclusion

The power consumption in TDCs is crucial because it directly impacts the overall efficiency of electronic systems. Lower power consumption can lead to reduced energy use, better thermal management, and extended device lifespan.

On the other hand, higher power consumption can cause excessive heat and diminish the performance and reliability of the system. Therefore, achieving an optimal balance between accuracy and power consumption in TDCs is crucial for extending the lifespan of electronic devices. In this paper, designing delay cell circuits and a D-FF in a 0.18 μm CMOS process with a 1.8 V supply voltage have been presented. The power consumption of

the proposed delay cells has been reduced using body bias technique.

The proposed delay cells have been implemented in flash TDC circuits, and the results demonstrate the proper performance of the presented structures.

Author Contributions

Conceptualization and design, M. Khoshnoud; formal analysis, M. Khoshnoud; software, M. Khoshnoud; investigation, S. M. Anisheh.; writing—original draft preparation, M. Khoshnoud; writing—review and editing, S. M. Anisheh. supervision, S. M. Anisheh, and M. Radmehr.

Conflict of Interest

The authors have disclosed that there are no potential conflicts of interest related to the publication of this work.

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Abbreviations

TDC	Time-to-Digital Converter
D-FF	D Flip-Flop
TG	Transmission Gate
FoM	Figure of Merit
TMSP	Time-Mode Signal Processing
VTC	Voltage-to-Time Converter
TVC	Time-to-Voltage Converter
DTC	Digital-to-Time Converter
PET	Positron Emission Tomography
TOF	Time-of-Flight
ADC	Analog-to-Digital Converter
TA	Time Amplifier
SAR ADC	Successive Approximation Analog-to-Digital Converter

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