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Research paper

Two Improved Topologies for Switched-Capacitor Multilevel Inverters

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Abstract

Background and Objectives: To achieve zero carbon emissions, renewable energy sources have gained noteworthy regard due to their dependable performance, cost efficiency, and adaptability within systems. Increasing adoption of renewable energy sources and electric vehicle (EV) has led to a growing need for enhanced voltage boost capability. Nevertheless, most of DC sources such as solar cells have a restricted capacity for boosting power. Multilevel inverters can operate as interfaces. In this study, two topologies of switched-capacitor multilevel inverters (SC-MLI) is suggested to overcome the mentioned constraints.

Methods:
Each stage of the introduced SC-MLI comprises a capacitor, a DC voltage supply, a diode, and two power electronic switches. A comprehensive analysis of the operational principles, and the characteristics of the presented converter, including its charging and discharging behaviors, are provided. Furthermore, the phase-disposition pulse width modulation (PD-PWM) technique is employed to generate the output voltage waveform of the introduced multilevel SC inverter.

Results: In the recommended topologies, the quantity of semiconductor power switches, isolated DC voltage supply, diodes, and so, volume and cost of the overall system are decreased in compare to similar SC-MLI topologies. The voltage across the capacitors is self-balanced accurately without using any auxiliary circuits or closed-loop systems. To validate the proposed SC-MLI's effective operation, the implemented topology's simulation and measurement results are presented. The total harmonic distortion for the 17-level inverter using the PD PWM technique at a modulation index 1 obtained 6.97%.

Conclusion: Comprehensive comparative analysis reveals that the introduced topologies have merits and superior performance compared to existing solutions regarding component number, voltage boost factor (BF), and voltage stress. Also, simulation and experimental test results verify theoretical analysis.

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Introduction

Multilevel inverters (MLIs) consist of semiconductor switches along with DC voltage sources produce staircase waveforms of voltage. In recent decades, multilevel inverters have emerged as crucial technologies in high-power medium-voltage electric power conversion systems. Consequently, they have become a significant area of interest in both industry applications and researches [1]-[5].

Significant progress has been achieved over the past two decades concerning multilevel inverters, highlighting the importance of reducing both the number of switching elements and, more critically, the number of DC sources [6]-[8]. Conventional multilevel inverters are divided into three distinct classifications: cascaded H-Bridge inverters (CHB), flying capacitor inverters (FC), and neutral point clamped inverters (NPC). Each of these inverter types presents limitations that restrict their applicability. The FC inverter requires a complex control strategy to maintain the capacitor voltage at the desired level, and this configuration also faces challenges related to balance and stability when the load type varies. The NPC inverter's applications are constrained by the switch requirements at elevated voltage generation levels. Additionally, both FC and NPC inverters can only achieve three to five levels due to the complex techniques needed for capacitor voltage balancing. In contrast, the CHB inverter outperforms the FC and NPC in terms of modularity, reliability, and superior error management; however, it necessitates multiple isolated DC voltage sources to generate a staircase output voltage [9]-[11].

Recently, various topologies are proposed to decrease the quantity of components across different applications. A decrease in semiconductor devices leads to smaller gate driver circuits, reduced size and volume, and lower overall system costs. DC sources contribute more weight, volume, and expense compared to other components in multilevel inverters [12]-[14]. Consequently, there has been considerable interest in developing multilevel inverters that minimize the use of isolated DC sources. Capacitors present a viable alternative to DC sources, giving rise to switched-capacitor (SC) multilevel inverters [15]-[19].

SC inverters are particularly suited for renewable energy applications due to their low output voltage; thus, voltage levels must be increased for high-voltage applications. Unlike traditional topologies that lack voltage boost capabilities, many of the recently proposed SC multilevel inverter configurations possess this feature. Multilevel inverters with voltage boosting capabilities have been introduced in [20]-[22]. Additionally, reference [23] presents a seven-level inverter topology with voltage boost functionality in grid-connected mode, which employs a single DC input source, two capacitors, and ten switches to elevate the input voltage. In [24], a five-level switched capacitor inverter configuration capable of doubling the input voltage is proposed, utilizing eight switches and a capacitor alongside a single DC voltage source to produce a five-level output. A drawback of this inverter is its high number of switching devices required to generate five output levels.

The various sections of the paper are introduced as given in the following: the recommended SC-MLI configuration and its operation principle are presented in section 2. Modulation technique, total standing voltage (TSV) and procedure of capacitances selection of the suggested MLI are described in section 3. Power loss calculation of the introduced SC-MLI are given in section 4. In the following, in section 5 simulation results are given to prove the operating principle of the SC-MLI. In section 6, experimental results for 17-level inverter are presented. The conclusions are articulated in Section 7.

Suggested Switched-Capacitor Multilevel Inverter

In this section, the method for constructing the suggested SC-MLI is clarified by explaining the topology and operation of the basic switched-capacitor unit. Additionally, the configuration of the 17-level SC-MLI is described.

A. Basic Configuration of SC-MLI

Fig. 1 illustrate the topology of suggested switched-capacitor based inverter. The proposed unit includes a DC voltage source, V_{in}, six power switches, Q_1, Q_2, Q_3, Q_4, S_1 and S_2, a power diode, D and a capacitor, C. The recommended topology produces five levels voltage waveform in the output.

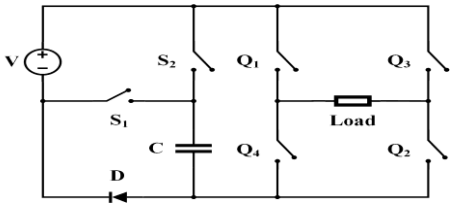


Fig. 1: Topology of proposed switched-capacitor inverter.

Fig. 2 illustrates the equivalent circuit and current flow paths of the proposed unit to produce various levels of the output voltage. In Fig. 2(a), switches S_2, Q_1 and Q_2 are turned on and switches S_1, Q_3, and Q_4 are turned off. Capacitor C is charging using the input DC voltage through diode D. In the end of this state, capacitor voltage equals to V_{in} and the output voltage equals to input DC voltage (V_O=V_{in}). If switch S_2 is off and switch S_1 is on, the output voltage is the result of adding the input voltage to the voltage across the capacitor (V_O=2V_{in}), as illustrated in Fig. 2(b). Likewise, in the negative half cycle, the equivalent circuits include two states as given in Fig. 2(c) and Fig. 2(d). In the second half cycle, switches Q_1, Q_2, Q_3 and Q_4 operate in the inverse state of the positive half cycle.

Switches Q_3 and Q_4 are turned on and Q_1 and Q_2 are turned off, and the operation of the unit components are similar to those in the positive half cycle. According to Fig. 2(c), zero voltage level in the output is possible via conduction of switches Q_1, Q_3 and switches Q_2, Q_4 in positive and negative half cycles, appropriately.

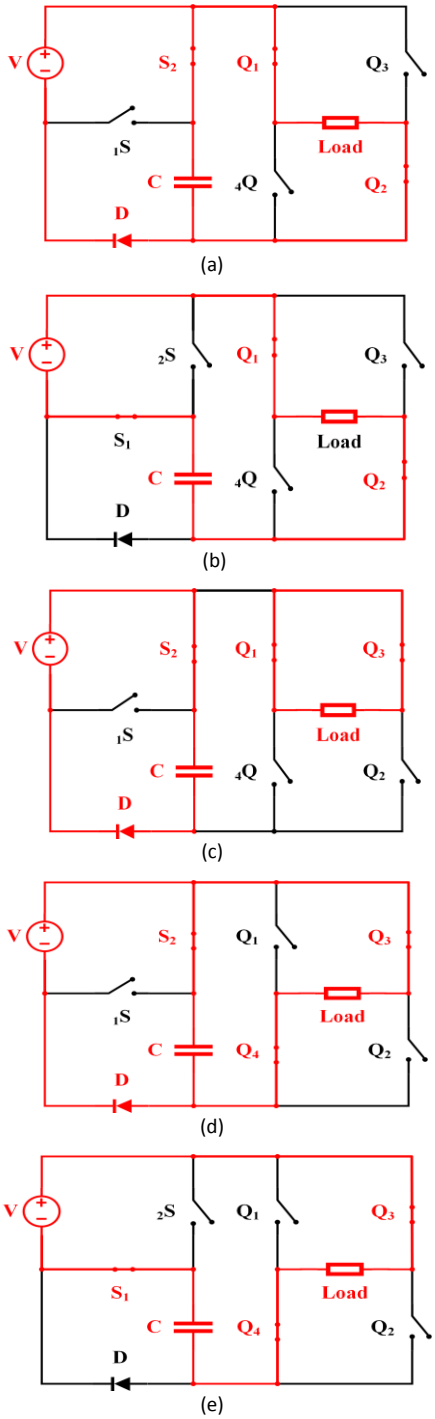


Fig. 2: Current flow paths of five-level inverter when output voltage is, (a) $+V_{in}$, (b) $+2V_{in}$, (c) 0, (d) $-V_{in}$, (e) $-2V_{in}$.

Switching states of the recommended five level unit in positive and negative half cycles is represented in Table 1. C_C and D_C describe the capacitor charging and discharging states, relatively.

Table 1: Switching states of suggested 5-level switched-capacitor based inverter

Positive half-cycle			
State Num.	**On-state switches**	**Capacitor state**	**Output Voltage**
1	S_2, Q_1, Q_2	C_C	V_{in}
2	S_1, Q_1, Q_2	D_C	$2\ V_{in}$
Negative half-cycle			
State Num.	**On-state switches**	**Capacitor state**	**Output Voltage**
3	S_2, Q_3, Q_4	C_C	$-V_{in}$
4	S_1, Q_3, Q_4	D_C	$-2\ V_{in}$

B. 17-Level SC-MLI

Fig. 3 depicts structure of the introduced 17-level SC-MLI. The presented SC-MLI uses two voltage sources V_1, V_2, ten switches, S_1, S_2, S_3, S_4, Q_a, Q_b, Q_1, Q_2, Q_3, Q_4, two diodes, D_1, D_2 and two capacitors, C_1, C_2. The first DC voltage source, V_1 equals to V, and the second one equals to $3V$.

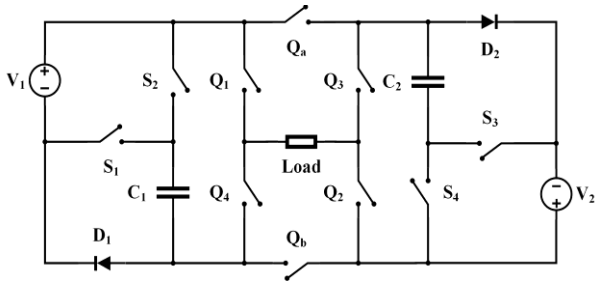


Fig. 3: Configurations of introduced 17-level SC-MLI.

Table 2: Switching states of introduced 17-level SC-MLI

First half cycle		
State Num.	**On-state switches**	**Voltage Level**
1	S_2, Q_1, Q_2, Q_b	V
2	S_1, Q_1, Q_2, Q_b	$2\ V$
3	S_4, Q_3, Q_4, Q_b	$3\ V$
4	S_2, S_4, Q_1, Q_3, Q_b	$4\ V$
5	S_1, S_4, Q_1, Q_3, Q_b	$5\ V$
6	S_3, Q_3, Q_4, Q_b	$6\ V$
7	S_2, S_3, Q_1, Q_3, Q_b	$7\ V$
8	S_1, S_3, Q_1, Q_3, Q_b	$8\ V$
Second half cycle		
State Num.	**On-state switches**	**Voltage Level**
9	S_2, Q_3, Q_4, Q_a	$-V$
10	S_1, Q_4, Q_3, Q_a	$-2\ V$
11	S_4, Q_1, Q_2, Q_a	$-3\ V$
12	S_2, S_4, Q_2, Q_4, Q_a	$-4\ V$
13	S_1, S_4, Q_2, Q_4, Q_a	$-5\ V$
14	S_3, Q_1, Q_2, Q_a	$-6\ V$
15	S_2, S_3, Q_2, Q_4, Q_a	$-7\ V$
16	S_1, S_3, Q_2, Q_4, Q_a	$-8\ V$

The suggested configuration generates 17-level voltage waveform in the converter output. In the second half cycle, semiconductors Q_1, Q_2, Q_3 and Q_4 operate in

the reverse state of those in the positive half cycle. Semiconductors Q_3 and Q_4 are turned on and Q_1 and Q_2 are turned off, and the operation of the switched-capacitor unit components are similar to those in the first half cycle, in each state. Zero voltage level in the output can be produced via operation of switches Q1, Q3 in the first half cycle and switches Q2, Q4 in the second half cycle. Operation of the suggested SC-MLI is similar to the operation of the switched-capacitor basic unit. Table. 2 indicates the switching states of the recommended 17-Level SC-MLI in the first and second half cycles.

Modulation Strategy

The most famous PWM control methods for multilevel inverters are space vector modulation (SVM) [15], phase disposition (PD-PWM) [16], phase opposite disposition (POD-PWM) [25], alternative phase opposite disposition (APOD-PWM) [21], selective harmonic elimination (SHE) [10], and hybrid modulation [22], [23]. In Table. 3, a systematic evaluation of various modulation techniques has been conducted, focusing on THD and efficiency across different modulation coefficient (m). This detailed analysis elucidates the performance characteristics of each technique in generating signals with minimal harmonic distortion while achieving optimal operational efficiency. The findings ultimately demonstrate that the PD modulation technique consistently outperforms the other examined modulation methods.

Table 3: Different PWM methods for proposed 17-level SC-MLI

PWM method	m	Fund.	THD	η_s
PD	1	350.6	6.98	98.5
	0.9	317.4	7.99	
	0.8	284.6	9.18	
POD	1	350.7	7.32	97.73
	0.9	317.5	7.98	
	0.8	284.6	9.18	
APOD	1	350.6	7.32	97.81
	0.9	317.4	8.01	
	0.8	284.6	9.18	

PD-PWM is applied as the control strategy of the suggested 5-level and 17-level SC-MLI as illustrated in Fig. 4 and Fig. 5, respectively. Results of applying this control strategy for 5-level and 17-level output voltage are given in Table. 4 and Table. 5, relatively.

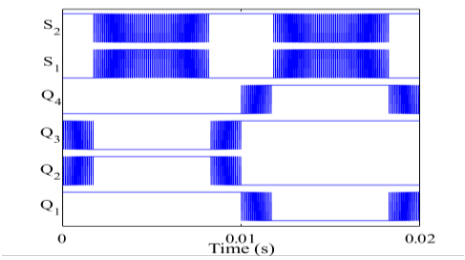


Fig. 4: PD-PWM method for proposed 5-level SC-MLI.

Table 4: Operation states of the basic 5-level SC-MLI

State Num.	Case	Equivalent circuit	On-state switches	v_o
1	$V_{ref}>V_{t2}$	Fig. 2(a)	S_2, Q_1, Q_2	V_{in}
2	$V_{t1}<V_{ref}\leq V_{t2}$	Fig. 2(b)	S_1, Q_1, Q_2	$2\ V_{in}$
3	$V_{t3}<V_{ref}\leq V_{t1}$	Fig. 2(c)	Q_1, Q_3 or Q_2, Q_4	0
4	$V_{t4}<V_{ref}\leq V_{t3}$	Fig. 2(d)	S_2, Q_3, Q_4	$-V_{in}$
5	$V_{ref}\leq V_{t4}$	Fig. 2(e)	S_1, Q_3, Q_4	$-2\ V_{in}$

Table 5: Operation states of the introduced 17-level SC-MLI

State Num.	Case	On-state switches	v_o
1	$V_{ref}>V_{t2}$	S_2, Q_1, Q_2, Q_b	V
2	$V_{t7}<V_{ref}\leq V_{t8}$	S_1, Q_1, Q_2, Q_b	$2V$
3	$V_{t6}<V_{ref}\leq V_{t7}$	S_4, Q_3, Q_4, Q_b	$3V$
4	$V_{t5}<V_{ref}\leq V_{t6}$	S_2, S_4, Q_1, Q_3, Q_b	$4V$
5	$V_{t4}<V_{ref}\leq V_{t5}$	S_1, S_4, Q_1, Q_3, Q_b	$5V$
6	$V_{t3}<V_{ref}\leq V_{t4}$	S_3, Q_3, Q_4, Q_b	$6V$
7	$V_{t2}<V_{ref}\leq V_{t3}$	S_2, S_3, Q_1, Q_3, Q_b	$7V$
8	$V_{t1}<V_{ref}\leq V_{t2}$	S_1, S_3, Q_1, Q_3, Q_b	$8V$
9	$V_{t9}<V_{ref}\leq V_{t1}$	Q_1, Q_3 or Q_2, Q_4	0
10	$V_{t10}<V_{ref}\leq V_9$	S_2, Q_3, Q_4, Q_a	$-V$
11	$V_{t11}<V_{ref}\leq V_{t10}$	S_1, Q_4, Q_3, Q_a	$-2V$
12	$V_{t12}<V_{ref}\leq V_{t11}$	S_4, Q_1, Q_2, Q_a	$-3V$
13	$V_{t13}<V_{ref}\leq V_{t12}$	S_2, S_4, Q_2, Q_4, Q_a	$-4V$
14	$V_{t14}<V_{ref}\leq V_{t13}$	S_1, S_4, Q_2, Q_4, Q_a	$-5V$
15	$V_{t15}<V_{ref}\leq V_{t14}$	S_3, Q_1, Q_2, Q_a	$-6V$
16	$V_{t16}<V_{ref}\leq V_{t15}$	S_2, S_3, Q_2, Q_4, Q_a	$-7V$
17	$V_{ref}\leq V_{t16}$	S_1, S_3, Q_2, Q_4, Q_a	$-8V$

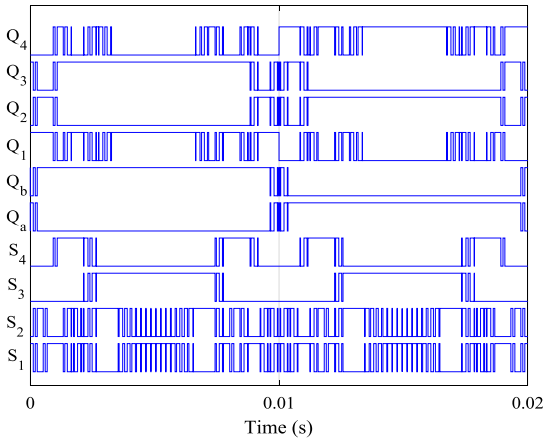


Fig. 5: PD-PWM method for proposed 17-level SC-MLI.

Total Blocking Voltage

One of the important items in the size and cost of inverters implementation is rating of semiconductors. In multilevel inverters, the semiconductors current rating equals to the supplied load current. Nevertheless, the semiconductors voltage rating is different. In the

suggested 5-level SC-MLI, voltage rating of switches S_1 and S_2 equals to V_{in} and blocking voltage of the H-bridge semiconductors (Q_1, …, Q_4) equals to $2V_{in}$. Consequently, total blocking voltage (*TBV*) of the 5-level SC-MLI is $10V_{in}$. In the recommended 17-level configuration, voltage rating of switches is equal to $8V_1$. Also, switches Q_a and Q_b has to block voltage of $8V_1$ and maximum voltage that the switches of the middle bridge (Q_1, …, Q_4) should withstand is $16V_1$. Total blocking voltage of the configuration is $32V_1$.

Capacitor Sizing

In this part, procedure of capacitor sizing for the recommended 17-level SC-MLI is explained. Similarly, this way is applicable for the basic 5-level SC-MLI. The capacitance of capacitors C_1 and C_2 are determined according to their voltage ripples. Determination of the capacitance guarantees that the capacitor maximum voltage ripple is *X*% of the charged capacitor voltage. Assume that the modulation index is *M*=1, the times t_1, t_2, …, t_{16} in Fig. 7 are calculated as follow [24]:

$$t_{(n=1,2,3,..8)} = \frac{\sin^{-1}(x_n)}{2\pi f_{ref}} \tag{1}$$

$$t_{(n=9,...,16)} = \frac{\pi - \sin^{-1}(x_{n-1})}{2\pi f_{ref}} \tag{2}$$

where x_n is calculated as given in (3).

$$x_n = \frac{n}{16}, n = 1,3,....15 \tag{3}$$

To reduce switching loss, the charging and discharging voltage of capacitors should be determined by the load current and the nearby voltage vector. If we assume that the power factor in the output is equal to 1, the discharged intervals of the capacitor C_1 are [t_2, t_3], [t_5, t_6] and [t_8, t_9]. Also, discharged time of capacitor C_2 is [t_6, t_{11}]. The ripples of the capacitors voltage are determined as follow:

$$\begin{cases} \Delta V_{C1} \simeq \left(\frac{1}{C_1}\int_{t_2}^{t_3} i_{C1}(t)\,dt + \frac{1}{C_1}\int_{t_5}^{t_6} i_{C1}(t)\,dt + \frac{1}{C_1}\int_{t_8}^{t_9} i_{C1}(t)\,dt\right) \\ \Delta V_{C2} \simeq \left(\frac{1}{C_2}\int_{t_6}^{t_{11}} i_{C2}(t)\,dt\right) \end{cases} \tag{4}$$

where ΔV_{C1} and ΔV_{C2} are capacitors C_1 and C_2 voltage ripples in the relevant time intervals. As regards the maximum voltage ripple is *X*% of the charged capacitor voltage, capacitances are valid in the following inequality:

$$C_1 \geq \max\left\{ \frac{1}{2V_{in}X\%}\int_{t_2}^{t_3} i_{C1}(t)\,dt, \frac{1}{2V_{in}X\%}\int_{t_5}^{t_6} i_{C1}(t)\,dt, \frac{1}{2V_{in}X\%}\int_{t_8}^{t_9} i_{C1}(t)\,dt \right\} \tag{5}$$

$$C_2 \geq \frac{1}{2V_{in}X\%}\int_{t_6}^{t_{11}} i_{C2}(t)\,dt \tag{6}$$

Calculation of Power Losses

SC-MLIs include three types of power losses: switching power losses (P_{sw}), conduction power loss (P_{cond}) and capacitance power loss (P_c). In a transistor combined with an anti-parallel diode, both the transistor and diode display on-state resistance and on-state voltage that contribute to conduction power loss. Although, conduction loss varies with temperature that is considered constant to simplify the analysis. In the following, the mentioned three types of power losses are determined for the suggested SC-MLI.

A. Conduction Loss

V_T and V_D are applied to denote on-state voltage of a transistor and a diode, respectively. As well as, the resistance of the mentioned semiconductors is r_T and r_D. Instantaneous power loss during conduction in a diode, $P_{C,D}(t)$, and transistor, $P_{C,T}(t)$, are determined as follow [9]:

$$p_{C,D}(t) = [V_D + R_D i(t)]i(t) \tag{7}$$

$$p_{C,T}(t) = [V_T + R_T i^{\beta}(t)]i(t) \tag{8}$$

In (8), β denotes constant of the transistor, $i(t)$ denotes the current of transistor or diode in instant *t*. If we assume N_T transistors and N_D diodes in the current path in the instant *t*, average of the conduction power loss, P_{Cond}, is calculated as described in (9).

$$P_{Cond} = \frac{1}{2\pi}\int_0^{2\pi} [N_T(t)\,p_{C,T}(t) + N_D(t)\,p_{C,D}(t)]dt \tag{9}$$

B. Switching Loss

With calculating the lost energy in the turn-on and turn-off intervals of switches, switching power loss of the multilevel inverter is obtained. Assuming that the voltage and current of a switch vary linearly during the switching interval, the energy lost during the turn-on and turn-off phases can be calculated as follows:

$$E_{off,k} = \int_0^{t_{off}} v(t)i(t)dt = \frac{1}{6}V_{sw,k}\,I\,t_{off} \tag{10}$$

$$E_{on,k} = \int_0^{t_{on}} v(t)i(t)dt = \frac{1}{6}V_{sw,k}\,I'\,t_{on} \tag{11}$$

where $E_{off,k}$ and $E_{on,k}$ are the lost energy in the turn on and turn off period of the k^{th} switch. Also, the turn on and turn off times of the switch are denoted using t_{on} and t_{off}. Additionally, the voltage across the switch prior to activation or following deactivation is denoted as $V_{sw,k}$. The currents through the switch before deactivation and after activation are represented by *I* and *I'*, respectively. In the MLI, the switching power loss, P_{sw}, is equal to the sum of all turn-on and turn-off energy losses at the line frequency of the output voltage, as specified in (12).

$$P_{sw} = f\sum_{k=1}^{N_{switch}}\left(\sum_{i=1}^{N_{on,k}} E_{on,ki} + \sum_{i=1}^{N_{off,k}} E_{off,ki}\right) \tag{12}$$

Here, *f* represents the line frequency, and the number of turn-ons and turn-offs of the k^{th} switch during a switching cycle is denoted as $N_{on,k}$ and $N_{off,k}$, respectively. Additionally, $E_{on,ki}$ is the energy lost by the switch during the i^{th} turn-on, while $E_{off,ki}$ is the energy lost during the i^{th} turn-off.

C. Capacitors Losses

Capacitor losses include internal resistance and voltage ripple of the capacitor that is given as follows [24]:

$$P_C = P_{rip} + P_{sc} \tag{13}$$

From (4), the voltage ripple loss (P_{rip}) is calculated as determined in (14).

$$P_{rip} = (\sum C_1 \Delta V_{C1}{}^2 + \sum C_2 \Delta V_{C2}{}^2) f_{ref} \tag{14}$$

In series connected capacitors, the internal resistance (r_{SC}) loss of the capacitor is determined as follows:

$$P_{SC} = \frac{1}{T}(4\int_{t2}^{t3} r_{SC1}\, i_{C1}{}^2(t)\,dt + 2\int_{t5}^{t6} r_{SC1}\, i_{C1}{}^2(t)\,dt + 2\int_{t6}^{t11} r_{SC2}\, i_{C2}{}^2(t)\,dt) \tag{15}$$

where r_{SC1} and r_{SC2} represent capacitors C_1 and C_2 internal resistances, respectively. So, total power loss of the MLI is sum of the switching, conduction and capacitor losses as described in (16).

$$P_{loss} = P_{cond} + P_{sw} + P_c \tag{16}$$

For a comprehensive analysis, Fig. 6 illustrates the switching losses, as well as the losses associated with the capacitors and diodes in the 17-level inverter. The results clearly indicate that the most significant losses in capacitor-switching inverters are attributed to the capacitor losses.

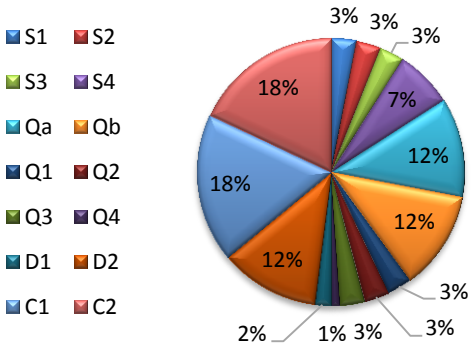


Fig. 6: Simulation results of the introduced 5-level SC-MLI.

Comparison Study

To validate the merits of the proposed configuration, it is compared with the other recently presented17-level topologies. The comparison in terms of different items such as number of output levels (N_L), number of DC sources (N_{DC}), number of switches (N_{SW}), number of capacitors (N_C), number of gate drives (N_{GD}), total standing voltage (*TSV*) and the N_L/N_{SW} ratio are given in Table 6. The N_L/N_{SW} ratio is one of the critical parameters used in the comparison because this ratio gives insight into the cost-effectiveness of the topologies. Larger value of this ratio means the topology need fewer switches to produce a specified voltage level. The difference in the number of N_{GD} and N_{SW} is due to the presence of bidirectional switches in some topologies.

Compared to the topologies presented in [23]-[26], the suggested topology uses fewer DC sources and switches and a higher N_L/N_{SW} ratio. The topology presented in [27] is similar to the introduced topology regarding the quantity of switches and N_L/N_{SW} ratio, but it uses more DC sources.

The structures presented in [28]-[30] are similar to the proposed topology in terms of the number of DC sources, but they have more switches and less N_L/N_{SW} ratio. The comparisons in this section show that the suggested MLI performs better and more favorably than other topologies.

Table 6: Comparison summary of various single DC source SC multilevel inverter topologies

	N_L	N_{DC}	N_{sw}	N_L/N_{SW}	N_c	N_{gd}	$TSV_{(P.U)}$
[23]	17	4	16	1.06	8	14	4
[24]	17	4	12	1.42	0	9	6
[25]	17	4	12	1.42	0	10	5.5
[26]	17	4	16	1.06	4	14	2.75
[27]	17	4	10	1.7	0	10	4
[28]	17	2	12	1.42	4	9	3.375
[29]	17	2	18	0.94	4	14	6
[30]	17	2	12	1.42	2	11	4.5
Proposed	17	2	10	1.7	2	10	5

Results and discussion

Proposed 5-level and 17-level SC-MLI is simulated using MATLAB/Simulink software. The converter simulation and experimental test parameters are listed in Table 7.

Table 7: Simulation and experimental tests parameters

Proposed SC-MLI	5-level	17-Level
DC voltage sources	V=100 V	V_1=45 V V_2=135 V
Capacitors	C=3000 µF	C_1= C_2= 2200 µF
Load specifications	R=30 Ω L=0.001 mH	R=75 Ω L=20 mH
Fundamental frequency (f_o)	50 Hz	50 Hz
Carrier frequency (f_C)	5 kHz	5 kHz
Diodes forward voltage drops (V_F)	0.8 V	0.8 V
Diodes internal resistance (R_D)	0.001 Ω	0.001 Ω
Internal resistance of capacitors (R_C)	-	1 Ω
Switches on-state resistance (R_{on})	0.1 Ω	0.1 Ω

At first, the recommended 5-level SC-MLI is simulated according to parameters given in Table 5. The inverter output voltage and capacitor voltage waveforms are illustrated in Fig. 7(a) and Fig. 7(b), respectively. Fig. 7(c) shows output voltage harmonic spectrum. THD of the output voltage is 33.19%.

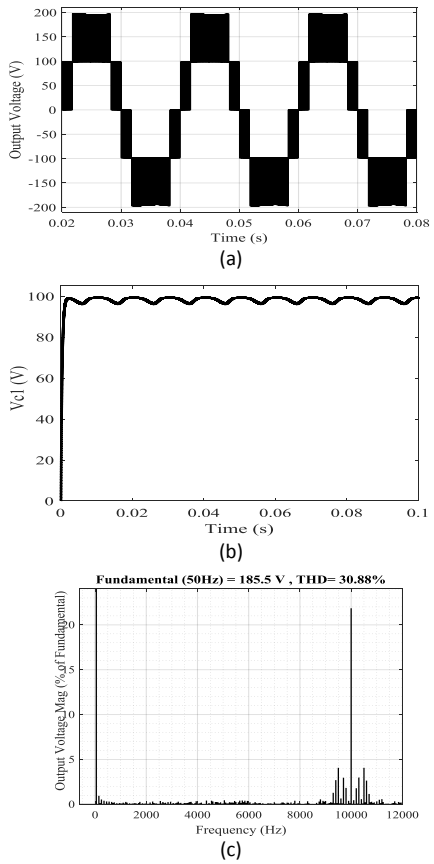


Fig. 7: Simulation results of the introduced 5-level SC-MLI, (a) output voltage waveform, (b) capacitor voltage waveform, (c) output voltage harmonic spectrum.

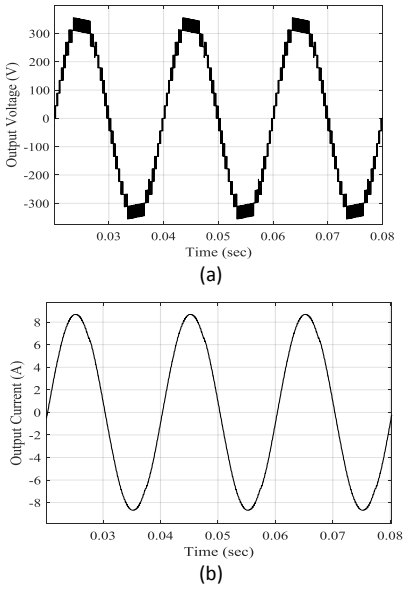


Fig. 8: Simulation results of the introduced 17-level SC-MLI, (a) output voltage waveform, (b) output current waveform.

In the following, one more SC unit with a middle bridge are added to obtain 17-level in the output voltage. Waveforms of the output voltage and current are illustrated in Fig. 8(a) and Fig. 8(b), respectively. Fig. 9(a) and Fig. 9(b) depict the capacitor voltage waveforms, respectively. Finally, Fig. 10 represent the harmonic spectrum of the output voltage. The output voltage THD is 6.97%.

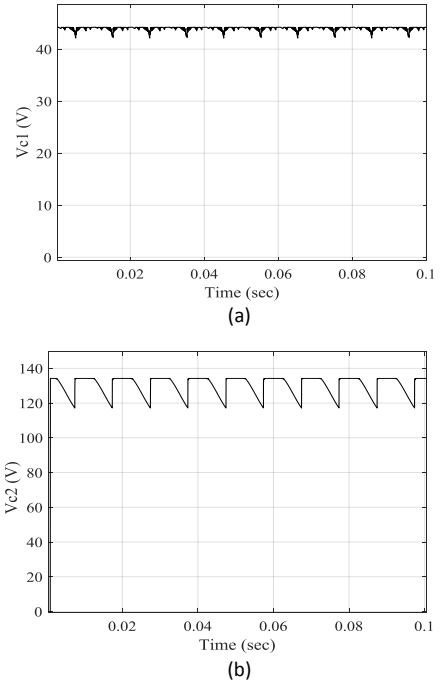


Fig. 9: Simulation results of the introduced 17-level SC-MLI, (a) capacitor C_1 voltage, (b) capacitor C_2 voltage waveforms.

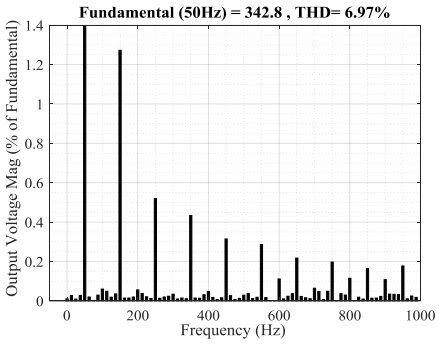
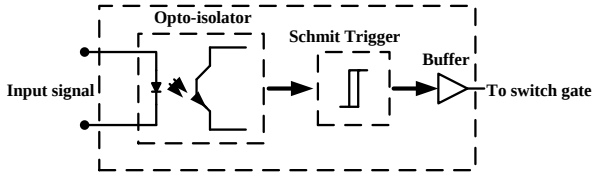


Fig. 10: Harmonic spectrum of 17-level output voltage.

To certify feasibility of proposed 17-level SC-MLI, a laboratory-scale prototype is implemented comprising IRFP450 MOSFETs (500V and 14A) and gate drivers (TLP250) as shown in Fig. 11(a). The logic-form equations related to PD-PWM modulation method is implemented using Atmel atmega8 in real time. Capacitors C_1 and C_2 values are 2200 µF. Two isolated DC supplies (V_1=10V and V_2=30V) for 17-level inverter with resistive load, R=160Ω, and two isolated DC supplies (V_1=5 and V_2=15 V) for 17-level inverter with inductive-resistive load,

R=340Ω, *L*=56mH, are used as the input sources. Fig. 11(b) illustrates schematic of the switches isolator and driver circuit that includes an opto-isolator, a buffer, and a Schmit trigger. Switches needs an isolated driver circuit. Opto-isolators operate in wide range of input signal pulse width. So, gate driver circuit based on opto-isolator is applied in the implemented converter.

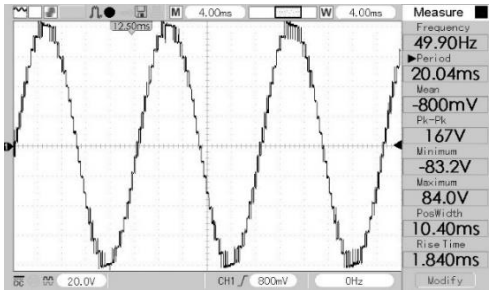
(a)



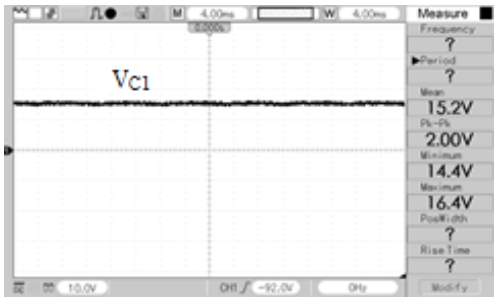
(b)

Fig. 11: Implemented set up of the 17-level SC-MLI, (b) switches gate driver circuit schematic.

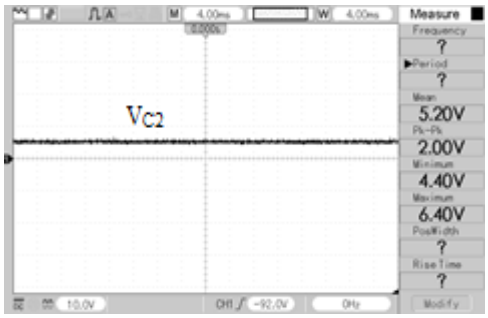
Fig.12 shows laboratory test results of output voltage and capacitors voltage waveforms of 17-level SC-MLI. As illustrated in Fig. 12(a), the proposed topology generates 17 levels voltage with the maximum of 80V. Output current waveform is proportional to the output voltage due to the resistive load. As well as, the voltage waveforms of capacitors C_1 and C_2 in full-load condition are shown in Fig. 12(b) and Fig. 12(c), respectively.



(a)



(b)



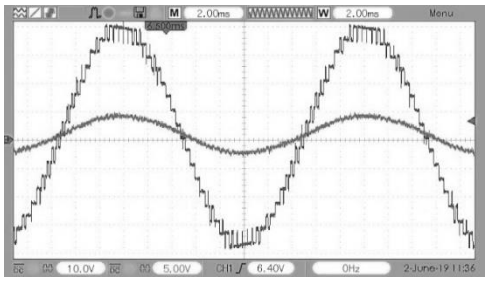
(c)

Fig. 12: Laboratory test results of introduced 17-level SC-MLI with resistive load; (a) output voltage, (b) capacitor C_1 voltage, (c) capacitor C_2 voltage.

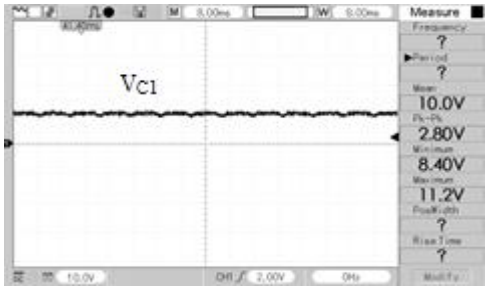
As depicted in these figures, the capacitors DC voltage are very smooth, as the voltage ripple of capacitors is nearly ±1V that is not considerable on the voltage results.

In the second study, the introduced 17-level SC-MLI is set to inductive-resistance load condition, and same as the before, the implemented topology generates 17-level output voltage with the maximum of 60V. Fig. 13 shows laboratory test results of 17-level output voltage and its related capacitors voltage waveforms. It's noted that the load current is more similar to the sinusoidal waveform than the load voltage due to low pass filter characteristics of RL load. Moreover, little phase difference between the load current and voltage waveforms is due to the inductive property of the load.

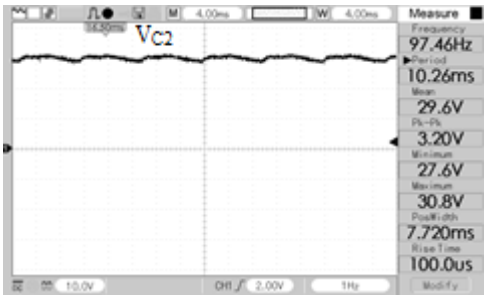
As these figures show, the test results validate the ability of the introduced converter in generating the wanted multilevel voltage waveforms and a desirable conformity between the laboratory and computer simulation test results.



(a)



(b)



(c)

Fig. 13: Laboratory test results of introduced 17-level SC-MLI with inductive-resistive load; (a) output voltage, (b) capacitor C_1 voltage, (c) capacitor C_2 voltage.

Conclusions

In this paper, two improved multilevel inverter based on composition of several DC voltage sources and switched-capacitors are presented. Each unit of proposed SC-MLI include a DC voltage source, a diode, a capacitor, and two power switches. The capacitors voltage is fixed on the DC source value with self-balancing feature.

Indeed, without using complex voltage balancing control, the capacitors are charged properly. Operation principle of the proposed SC-MLI is studied and PD-PWM method for the introduced SC-MLI switching is given. A laboratory set up of the recommended multilevel inverter was fabricated.

Computer simulation and laboratory test results for 5 and 17 level voltage waveforms validate operation of the suggested multilevel inverter. Notably, the 17-level inverter achieves a voltage boost to 80 V while successfully reducing the total harmonic distortion to 6.97.

Furthermore, the capacitors are charged to 5 V and 15 V, demonstrating minimal ripple in their voltage levels. These findings indicate a strong agreement between the simulation and experimental results, showcasing the introduced multilevel inverter capability to produce output voltages that meet the expected performance criteria.

Author Contributions

F. Sedaghati chose the field of research. S. Ebrahimzadeh and H. Dolati collected information in this field. F. Sedaghati presented the proposed topology. S. Ebrahimzadeh and H. Dolati simulated and fabricated the proposed converter converter. The authors discussed the obtained results and drew conclusions. Under the supervision of F. Sadaghti, the text of the article was prepared by S. Ebrahimzadeh and H. Dolati. F. Sedaghati submitted the manuscript.

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Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the ethical issues including plagiarism, informed consent, misconduct, data fabrication and, or falsification, double publication and, or submission, and redundancy have been completely witnessed by the authors.

Abbreviations

EV	Electric Vehicle
CHB	Cascaded H-Bridge
PWM	Pulse Width Modulation
SC	Switched Capacitor
MLI	Multilevel inverter
THD	Total Harmonic Distortion
TSV	Total Standing Voltage
FC	Flying capacitor
NPC	Neutral point clamp
BF	Boost Factor
PD	Phase-disposition
m	modulation coefficient

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