Journal of Electrical and Computer Engineering Innovations
(JECEI)
Journal homepage: http://www.jecei.sru.ac.ir

Research paper

An Efficient CMOS-Based Ternary Decoder with Negative and Positive Ternary Inverters Along with a Binary NOR Gate

Seyede Mahboobeh Mousavi Monazah [1], *Nabiollah Shiri* [2,*], *Mahmood Rafiee* [2], *Ayoub Sadeghi* [3]

[1] *Nano Opto-Electronics Research Center, Electrical Engineering Department, Shiraz University of Technology, Shiraz, Iran.*

[2] *Department of Electrical Engineering, Shi.C., Islamic Azad University, Shiraz, Iran.*

[3] *Department of Electrical and Computer Engineering, University of Illinois at Chicago, Chicago, IL.*

Article Info

Article History:
Received 09 May 2025
Reviewed 25 July 2025
Revised 04 August 2025
Accepted 14 August 2025

Keywords:
Ternary decoder
CMOS
High-speed
Don't care
Low-power

[*]Corresponding Author's Email Address: *na.shiri@iau.ac.ir*

Abstract

Background and Objectives: In modern digital design, ternary logic gives simplicity and efficiency by reducing connectivity and chip area. This paper presents a new ternary decoder with only two ternary inverters and one binary NOR gate. One of the inverters is used simultaneously as a negative ternary inverter (NTI) and a positive ternary inverter (PTI) to attain circuit area reduction. Also, using the binary NOR instead of the ternary NOR eliminates don't care states (middle voltage mode). The proposed decoder is implemented with complementary metal-oxide-semiconductor (CMOS), double pass logic (DPL), gate diffusion input (GDI), and pass transistor logic (PTL). In the proposed ternary decoder, the four mentioned technologies show an appropriate power delay product (PDP) and a smaller occupied area compared to the literature.

Methods: In this paper, all simulations are performed using the 90 nm model, BSIM4 (level 54), by the HSPICE tool. The CMOS, DPL, PTL, and GDI techniques are used in the presented ternary decoder, and the results are extracted. The decoder showed good functionality compared to the previous research when implemented by these four circuits, but the best performance in terms of PDP results is from the CMOS.

Results: The CMOS-based ternary decoder has only 10 transistors and shows the best results; while its power consumption and propagation delay are 26.393 µW and 0.095 ns, respectively. Besides, the number of transistors is reduced by 16.66% while it has a two times increase in speed compared to the best decoders in previous research. The proposed high-speed and low-complexity decoder can be used in full adders (FAs) and digital signal processors (DSPs).

Conclusion: Due to the benefits that ternary logic provides over binary logic, a ternary decoder utilizing CMOS technology has been created, featuring fewer components, a reduced footprint, and enhanced speed in comparison to current ternary decoders. This groundbreaking decoder utilizes only two ternary inverters and a single binary NOR gate, with one of the inverters serving the dual purpose of a negative ternary inverter (NTI) and a positive ternary inverter (PTI) simultaneously. Furthermore, the inclusion of a binary NOR gate eliminates don't-care states and further decreases the area of the circuit.

How to cite this paper:
S. M. Mousavi Monazah, N. Shiri, M. Rafie, A. Sadeghi, "An efficient CMOS-based ternary decoder with negative and positive ternary inverters along with a binary NOR gate," J. Electr. Comput. Eng. Innovations, 14(1): 107-116, 2026.

DOI: 10.22061/jecei.2025.11910.842

URL: https://jecei.sru.ac.ir/article_2391.html

Introduction

Digital integrated circuits (ICs) are widely used in many complex systems and can be implemented in microprocessors or mixed-mode circuits such as analog-to-digital converters (ADCs) or error correction systems [1], [2]. In the past decades, many analog circuits have been presented so that they behave digitally like radio and photography circuits [3]-[5]. As an advantage, the switching feature in the digital circuits allows the implementation of random behaviors using minimal discrete binary memory [6], [7], but digital circuits have challenges such as the large area, increased pin-out, problems with proper placement of pins to communicate with off-chip, and mechanical defects during the manufacturing process, as well as thermal sensitivities [8], [9]. These problems caused scientists to concentrate on alternatives for binary logic and to use multi-value logic (MVL). An important advantage of MVL-based systems is the ability to transmit more information in an instant or in a sample time [10], [11]. In an MVL circuit, more than two logic modes are represented, so the complexity of the system compared to a binary logic system is avoided, and the number of components and interconnections is reduced, so power consumption (PC) is reduced while the latency of the circuit is increased with bit density [12]. If MVL is used in complementary metal-oxide-semiconductor (CMOS) binary logic design, it performs better [13], [14].

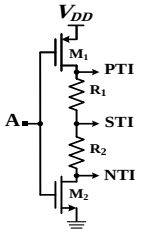
Ternary logic is an MLV state with three values of 0, 1, and 2, which denote false, undefined, and true ternary values, respectively. The ternary logic showed better results in terms of efficiency and complexity than MLVs with higher logic values [15]-[17]. Implementing a ternary circuit using CMOS logic, known as ternary CMOS (T-CMOS), yields a practical and scalable circuit design [18], [19].

In this paper, a CMOS-based ternary decoder is proposed. The proposed decoder has a low power consumption, low propagation delay (PD), and high speed. These properties enable fast decoding and make it attractive for practical applications.

This paper is organized as follows: Section 2 discusses the recent works related to the ternary logic. Section 3 presents the proposed ternary decoder. Simulation results and comparisons are discussed in Section 4. Finally, the paper concludes in Section 5.

Related Works

In research, various logic gates are used in ternary decoders, including standard ternary inverters (STIs), negative ternary inverters (NTIs), positive ternary inverters (PTIs), ternary NOR logic gates, binary AND logic gates, and binary NOR logic gates [20]. Fig. 1 (a) shows the ternary inverter structure and (b) the truth table of PTI, STI, and NTI [21], [22].



(a)

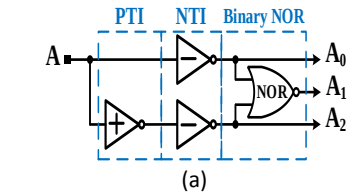
Inputs	NTI	STI	PTI
0	2	2	2
1	0	1	2
2	0	0	0

(b)

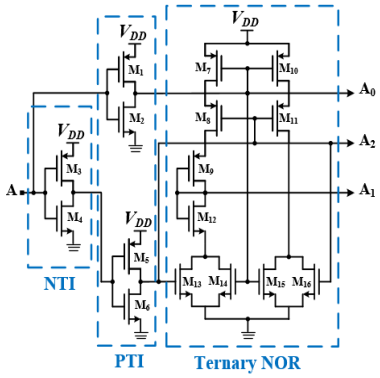
Fig. 1: (a) Ternary inverter structure and (b) truth table.

The transistor-level implementation of digital gates is performed by using pass transistor logic (PTL), double pass logic (DPL), gate diffusion input (GDI), and CMOS techniques. The GDI technique consumes low power, a small area, and it also has low complexity [23]-[25]. In the PTL technique, the number of required transistors for special logic functions is reduced, which causes both area and power reduction [26], [27]. The complementary pass transistor logic (CPL) is modified, and the DPL is formed, which improves the speed degradation and enhances the noise margins, especially at reduced supply voltages (V_{DD}s) [28], [29]. The CMOS technology has the main advantage of very low energy dissipation and almost no static energy dissipation, and only in switching conditions is power lost. These features make it possible to integrate more CMOS gates in an IC than bipolar or NMOS technologies [28], [30], [31].

Fig. 2 (a) shows a DPL-based ternary decoder that consists of fewer transistors than Fig. 2 (b) with a ternary NOR gate and carbon nanotube field-effect transistor (CNTFET) technology [20], [32], [33].



(a)



(b)

Fig. 2: (a) and (b) are ternary decoders.

The circuit of Fig. 2 (b) [32], [33] has 16 transistors, but Fig. 2 (a) [20] has 12 transistors. The results of Fig. 2 (a) [20] indicate the approach's achievements,

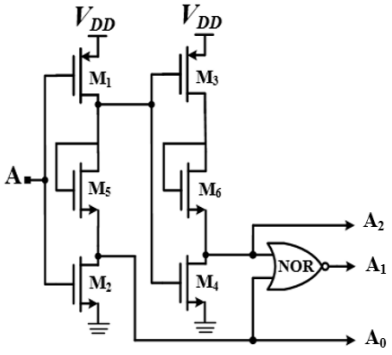
considering the reduced number of transistors by 25% compared to Fig. 2 (b) [32], [33] and using binary logic gates. In Fig. 2 (a), reducing the number of transistors increases the speed of the circuit and reduces the power compared to Fig. 2 (b).

This paper discusses a CMOS-based ternary decoder that utilizes only 10 transistors, with a power consumption of 26.393 µW and a propagation delay of 0.095 ns. The transistor count has been decreased by 16.66%, while the speed has doubled in comparison to the most efficient decoders from prior studies. Subsequently, the design of the proposed decoder across four distinct technologies is examined, and the findings are presented.

Proposed Circuit

To take advantage of binary and ternary logic, one of the most important tasks is to convert ternary to binary logic using a decoder, which is why decoder design is so important. Among the decoders, attaining low power, small area, and high speed are the desired features.

In this research, a new ternary decoder with only two ternary inverters and one binary NOR gate is expressed, as shown in Fig. 3 (a). One of the inverters in the proposed ternary decoder is used simultaneously as NTI and PTI, causing area reduction. In addition, using a binary NOR gate instead of a ternary NOR gate causes the elimination of don't care states (middle voltage mode).



(a)

A	A_0	A_1	A_2
0 (0 V)	2 (1.2 V)	0	0
1 (0.6 V)	0	2 (1.2 V)	0
2 (1.2 V)	0	0	2 (1.2 V)

(b)

Fig. 3: (a) Proposed ternary decoder circuit and (b) Input and outputs of the proposed ternary decoder.

The proposed ternary decoder only uses 10 transistors and, compared to Fig. 2 (a), has less number of transistors, lower propagation delay, and a smaller area. Here, the ternary signal A is fed as the input to the circuit, and then the three decoded outputs of A_0, A_1, and A_2 are obtained. Three-value logic is one of the most common and widely used multi-value logics that reduces power consumption, area, and the possibility of noise while increasing the speed. To create the desired logic and reduce the area, one of the inverters acts simultaneously as PTI and NTI, and a binary NOR gate is used instead of the ternary NOR gate.

The proposed ternary decoder has a ternary input and three binary outputs, as written in (1):

$$A^D = \begin{cases} 2 & \text{IF} \quad A = D \\ 0 & \quad\quad A \neq D \end{cases} \tag{1}$$

where D can take three logic values 0, 1, and 2. The decoder outputs can take only two logic values of 2 and 0, which correspond to logic 1 and logic 0 in binary logic.

Fig. 3 (b) shows the input and outputs of the proposed ternary circuit, where 0 is equal to 0 V, 1 is equivalent to 0.6 V, and 2 is equivalent to 1.2 V. The outputs only have the minimum and maximum voltages, 0 and 1.2 V, respectively, and this is the conversion from the ternary to the binary logic.

Equation (2) is the relationship between the inputs and the output at the NOR gate in Fig. 3 (a). Here, A_2 and A_0 are inputs, and A_1 is the output.

$$A_1 = \overline{A_2 + A_0} \tag{2}$$

Table 1 shows nine modes of the ternary NOR gate and four modes of the binary NOR gate. Since A_2 and A_0 are the NOR gate inputs, only states of 1, 2, and 3 occur in binary logic, and states of 1, 3, and 7 occur in ternary logic. The table has many unused states in the ternary logic, and this is why using a binary gate instead of a ternary gate is a promising technique. Here, intermediate states never occur, and this is when the inputs have logic 1 (0.6 V).

Table 1: The truth table of the ternary and binary NOR gate

State	Ternary NOR gate			Binary NOR gate		
	Inputs		Output	Inputs		Output
	A_2	A_0	A_1	A_2	A_0	A_1
1	0	0	2	0	0	2
2	0	1	1	0	1	0
3	0	2	0	1	0	0
4	1	0	1	1	1	0
5	1	1	1			
6	1	2	0			
7	2	0	0			
8	2	1	0			
9	2	2	0			

Propagation delay (t_{pd}) is the time interval when the

input crosses 50% of the V_{DD} to the output crossing 50% of the V_{DD}. Equation (3) shows the propagation delay by the Elmore method. The Elmore delay model estimates the delay from a switching source to the network nodes, requiring both the equivalent capacitance of the node, C_i, and the equivalent resistance of that node, $R_{is,}$ and calculated by (3).

$$t_{pd=\sum_i R_{is} C_i} \tag{3}$$

Dynamic power consumption is the dominant portion of the total power in the proposed ternary decoder, so the value of static power in (4) is ignored.

$$P_{total} = P_{dynamic} + P_{static} \tag{4}$$

According to (5), dynamic power consumption is the sum of the switching power and short circuit power, but the short circuit power is neglected because it just includes approximately 10% of the dynamic power, approximately.

$$P_{dynamic} = P_{switching} + P_{short\ circuit} \tag{5}$$

Equation (6) shows switching power, where the load capacitance of C_L is equal to C_{Self} + $C_{Fan\text{-}out}$ + C_{Wire}. The power supply and operating frequency are shown by V_{DD} and f, respectively, and C_{Wire} is the interconnect capacitance, $C_{Fan\text{-}out}$ is the total fan-out capacitance, and C_{Self} shows the total capacitances connected to the main output nodes.

$$P_{switching} = C_L V_{DD}^2 f \tag{6}$$

As shown in (7), the fan-out capacitance (C_g) is the sum of all gate capacitances, and it is increased by connecting transistors to the output. Here, C_{ox} shows that the oxide capacitance is dependent on transistor width (W) and transistor length (L). Also, the total overlap capacitances between the gate-drain and gate-source of the transistors are named C_{ol}.

$$C_{Fan-out} = \sum C_G = (C_{ox}L + 2C_{ol})\sum(W_n + W_p) \tag{7}$$

The effective capacitance (C_{eff}) is given by (8), where C_j is the total junction capacitance between the drain, source, and gate of a transistor. The total C_{self} and its relation with C_{eff} are shown by (9).

$$C_{eff} = C_j + C_{ol} \tag{8}$$

$$C_{self} = \sum C_{self} = C_{eff}\sum(W_n + W_p) \tag{9}$$

Equation (10) shows the average power ($P_{average}$) in the proposed ternary decoder, V_{DD} is 1.2 V, frequency is 200 MHz, W_n and W_p are equal, and their value is 300 nanometers.

$$P_{average} = [(C_{ox}L + 2C_{ol})\sum(W_n + W_p) + C_{eff}\sum(W_n + W_p) + C_{wire}] \times V_{DD}^2 \times f \tag{10}$$

Power-delay product (PDP) is known as switching energy and expresses the product of average power consumption over a switching event and the input-output delay that is given by (11).

$$PDP = P_{average} \times t_{pd} \tag{11}$$

The proposed decoder is implemented in CMOS technology; it has a small load capacitance (LC). The number of transistors in the decoder is decreased to 10 to minimize area occupation and power consumption, critical internal nodes, and delay. However, PTL, DPL, and GDI techniques are explored for the proposed decoder structure. Fig. 4 shows the different structures of the binary NOR gate. The NOR gate in this ternary decoder is implemented by CMOS, PTL, DPL, and GDI techniques.

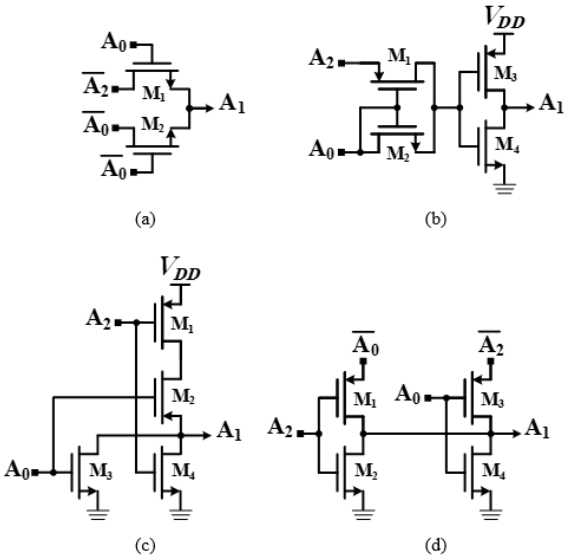


Fig. 4: NOR gate structure ((a)-PTL, (b)-GDI, (c)-CMOS, (d)-DPL).

As shown in Fig. 4(a), the PTL employs fewer transistors than the other structures; however, it uses only NMOS devices and requires inverted inputs. Consequently, four additional transistors are included to perform the input inversion.

Fig. 4 (b), the GDI, like Fig. 4 (c), the CMOS structure consists of four transistors. The PTL and DPL consist of inverted inputs. So, four transistors are added to the NOR gate. Usually, increasing the number of transistors in the circuit increases the power consumption, PDP, and circuit area. Also, the internal capacitances and propagation delay of the circuit are increased by increasing the number of nodes.

In the proposed circuit of Fig. 3, the propagation delay, power consumption, and PDP are calculated with four binary NOR gate structures, and it is observed that in all four cases, the PDP is lower than in the previous studies.

Results and Discussion

In this paper, all simulations are performed using the 90 nm model, BSIM4 (level 54), by the HSPICE tool. The

CMOS, DPL, PTL, and GDI techniques are used in the presented ternary decoder, and the results are extracted.

Table 2 shows the simulation setup of the proposed decoder. The normal V_{DD} is 1.2 V, frequency is 200 MHz, load capacitance is 1 fF, and temperature is 25 °C. The width of both NMOS and PMOS transistors is 300 nm, while their length is 100 nm. However, the sixth NMOS transistor has a width of 1000 nm. The device's parameters are set to the minimum possible without damaging the output and attaining a small value of the PDP.

Table 2: Simulation setup of the proposed decoder

Variation	V_{DD} (V)	T (°C)	LC (fF)	Freq (MHz)	Wn2,4= Wp1,3 (nm)	Wn5,6 (µm)	Ln=Lp (µm)
V_{DD}	1.1-1.5	25	1	200	300	0.3,1	0.1
T	1.2	-100 to 100	1	200	300	0.3,1	0.1
LC	1.2	25	0-15	200	300	0.3,1	0.1
Freq	1.2	25	1	200-2000	300	0.3,1	0.1

Considering Table 2, the results are extracted for V_{DD} changes from 1.1 V to 1.5 V, temperature (T) changes from -100 °C to 100 °C, frequency changes from 200 MHz to 2 GHz, and load capacitance changes from 0 to 15 fF. The decoder shows good functionality compared to the previous research when implemented by these four circuits, but the best performance in terms of PDP results is from the CMOS. The results of the ternary decoder for the variations of temperature, V_{DD}, load capacitance, and frequency are extracted, and it is observed that the CMOS has a smoother slope than other techniques in all variations.

Fig. 5 shows the relationship between the PDP and temperature variations from -100 °C to 100 °C. The best results of the PDP are approximately at low temperatures for the CMOS. By increasing the temperature, the power consumption and PDP rise. These changes occur in the CMOS decoder with a gentler slope.

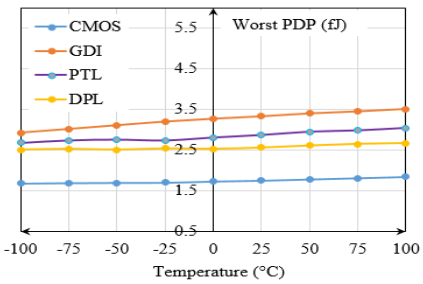


Fig. 5: PDP against temperature variations.

Fig. 6 shows the worst PDP changes based on the V_{DD} variations, for all values of the V_{DD}, the CMOS decoder has the best results. From (6), when V_{DD} increases, the power of the decoder also increases and causes the PDP to grow. Excessive reduction of the V_{DD} distorts the peak voltage and results in non-full-swing outputs. The frequency variations are checked, and the PDP results of four styles of the decoder are shown in Fig. 7, which shows higher PDP results at the higher frequencies. The dynamic power is directly proportional to the frequency, (6), which is confirmed in Fig. 7.

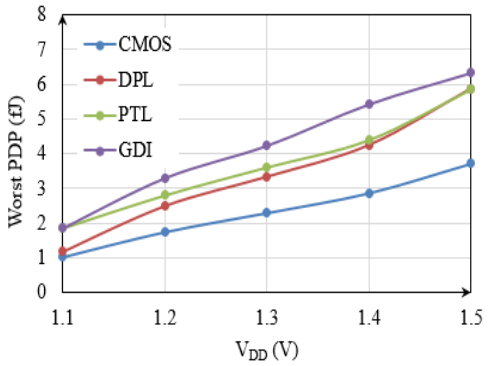


Fig. 6: PDP against V_{DD} variations.

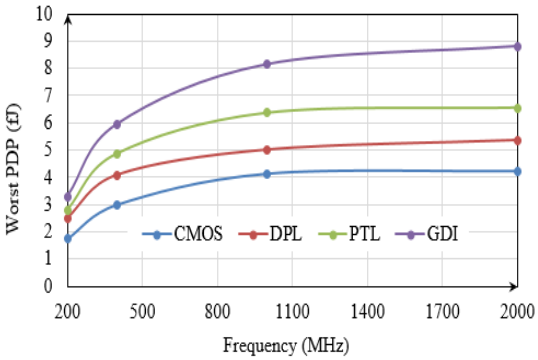


Fig. 7: PDP against frequency variations.

The results of the PDP changes according to the load capacitance variations are shown in Fig. 8. Here, the CMOS-based decoder gives the best PDP. In high load values, the propagation delay and power have high values.

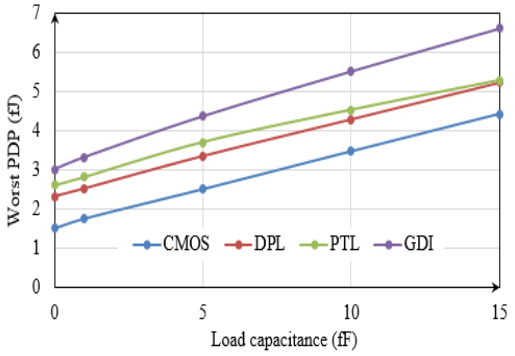


Fig. 8: PDP against load capacitance variations.

The process corners are considered, and the maximum average power results are extracted and shown in Fig. 9. Typical-typical (TT) corner means NMOS and PMOS transistors are typical. Slow-slow (SS) corner means NMOS and PMOS transistors are slow, and the fast-fast (FF) corner means NMOS and PMOS transistors are fast in this ternary decoder. For the CMOS, DPL, PTL, and GDI, the best corner is SS, while the worst one is FF. The reliability of the circuits is tested with all possible changes in the process corners. In the FF corner, the number of inputs per unit of time increases, which causes energy loss and increasing power consumption, while in the SS corner, less energy loss is observed, and the circuit works more slowly. The TT corner is considered, which shows normal conditions both in terms of speed and power.

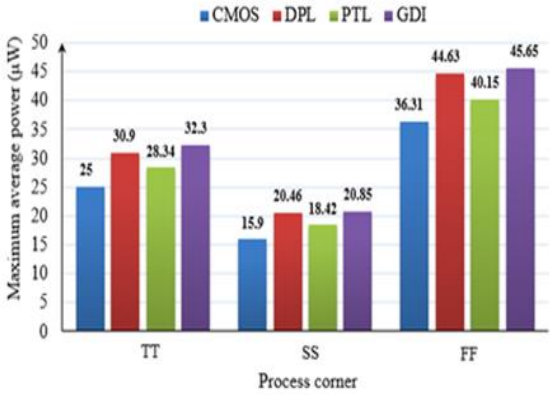


Fig. 9: Power dissipation in process corners.

The decoder is evaluated in more detail of area occupation by providing a layout using Cadence Virtuoso software based on TSMC 90 nm technology. As shown in Fig. 10, the decoder has 2.89 µm, 7.5 µm, and 21.67 µm^2 as length, width, and total die area, respectively for CMOS technology and 2.89 µm, 11.11 µm, and 32.10 µm^2 as length, width, and total die area, respectively for DPL technology and 2.89 µm, 8.84 µm, and 25.54 µm^2 as length, width, and total die area, respectively for PTL technology and 2.89 µm, 7.44 µm, and 21.50 µm^2 as length, width, and total die area, respectively for GDI technology.

The layout of the proposed decoder is drawn, and validation tests are performed. The design rule check (DRC), layout versus schematic (LVS), and parasitic extraction (PEX) are checked, and the accuracy of the encoder layout is confirmed.

Then the ternary decoder layout is located in a pad with 16 ports, consisting of 1 input port and 3 output ports for each technology and two ports for the V_{DD} and GND rails.

In Fig. 10, the three-dimensional (3D) layout is provided by an interface between the Sonnet and Cadence tools.

Table 3 shows the specifications of the proposed circuit in terms of the number of transistors, power, propagation delay, and PDP. Both in regular (ideal) and post-layout conditions, the proposed circuits are evaluated and compared, and the results are summarized in Table 3.

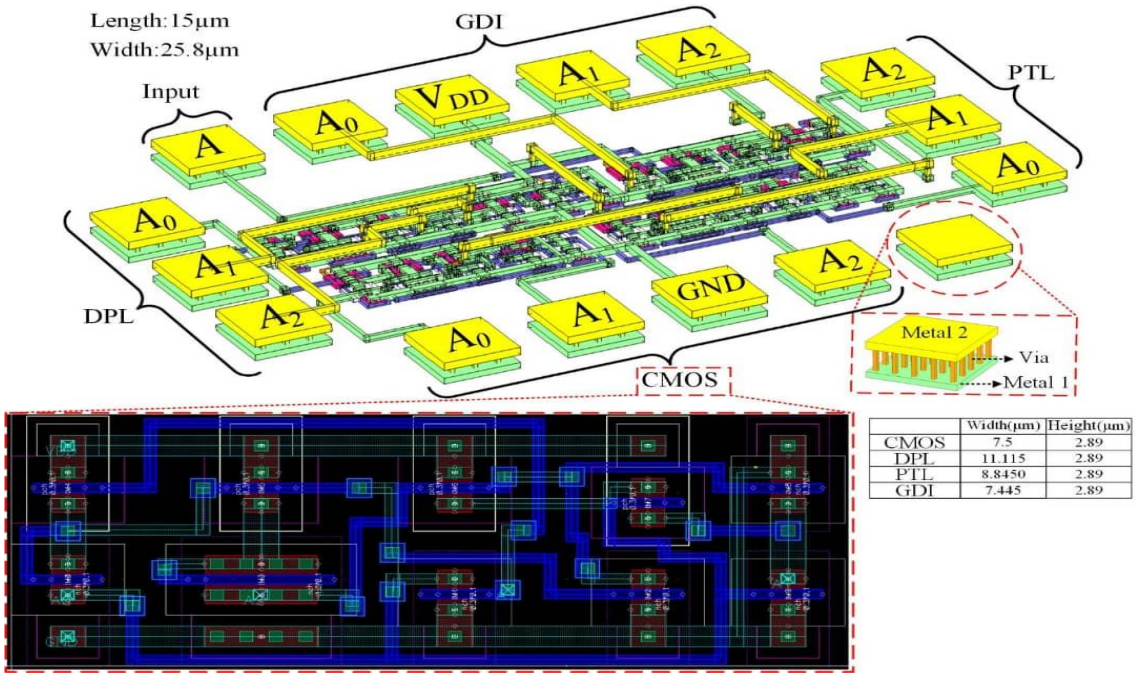


Fig. 10: The 3D layout of the ternary decoder.

Here, the number of transistors in the GDI cell is the same as the number of transistors in the CMOS, so the two circuits have an equal area. However, in the GDI, the circuit consumes more power than other techniques. In

the PTL, the circuit delay is higher than that of CMOS, and due to the use of only NMOS transistors, the circuit does not pass the maximum voltage level completely. In the DPL, the number of transistors is more than in the others, so the circuit area is higher.

In the best technology of this decoder circuit, CMOS structure, power is 26.393 µw for regular simulation results and 31.25 µw for post-layout simulation results. These results show about a 1.25-fold increase in PDP for post-layout simulation.

Table 3: Characteristics of the proposed decoder

Parameters	Type	Transistors Number	PC (µW)	PD (ns)	PDP (fJ)
Regular simulation results	CMOS	10	26.393	0.095	1.75
	DPL	14	30.9	0.08	2.5
	PTL	12	28.34	0.09	2.8
	GDI	10	32.3	0.1	3.3
Post-layout simulation results	CMOS	10	31.25	0.071	2.2
	DPL	14	38.67	0.080	3.09
	PTL	12	35.45	0.092	3.19
	GDI	10	40.4	0.1	4.04

For the proposed ternary decoder, the best-implemented technique in terms of area, power, and PDP is the CMOS, whose results are shown in Fig. 11. It can be seen that if the ternary signal A is zero, A_0 reaches the high voltage level, 1.2 V in 90 nm technology. When A is 1.2 V, the A_2 signal reaches 1.2 V, and when the voltage level of signal A is 0.6 V, A_1 is 1.2 V. In other words, A_0 decodes the low voltage level, A_1 decodes the intermediate voltage level, and A_2 decodes the high voltage level of the input ternary signal of A.

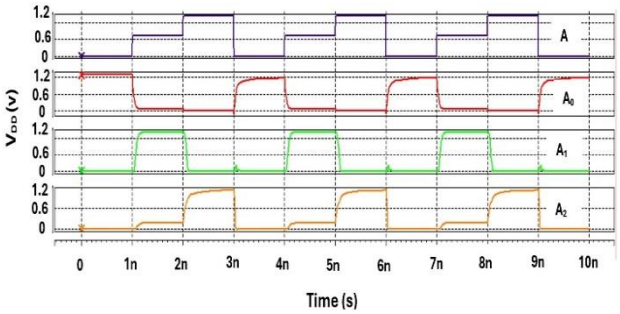


Fig. 11: Proposed CMOS-based ternary decoder results.

In 90 nm BSIM4 simulations, process variations are addressed via corner analysis, Monte Carlo, and mismatch modeling, ensuring robustness across manufacturing tolerances. The results of the Monte Carlo simulation are performed for the PVT variations. The test vector is used, the nominal value of V_{DD} is 1.2 V, and 10% of V_{DD} variations (1.1 V - 1.3 V) are considered. Also, the temperature variation is performed for the range 0 °C to 100 °C. The three process corners of TT, SS, and FF are considered, and the Monte Carlo method is performed with 100 runs.

Fig. 12 shows the PVT variations for all three corners of the design. The decoder outputs show good stability in all various random conditions.

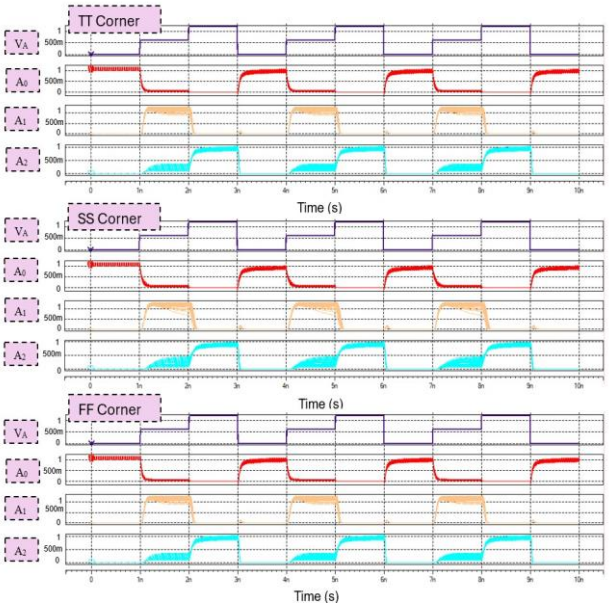


Fig. 12: PVT variations.

Fig. 13 shows the input voltage and noise margin graphs for the three output modes in the proposed circuit. In this figure, the point where the output meets the input voltage is where the difference between the output and input voltage levels reaches its minimum allowable level, and noise can cause a logic error. On the other hand, to cover all states of don't care, outputs of the A_0 and A_2 are extracted from the first and second inverters, respectively.

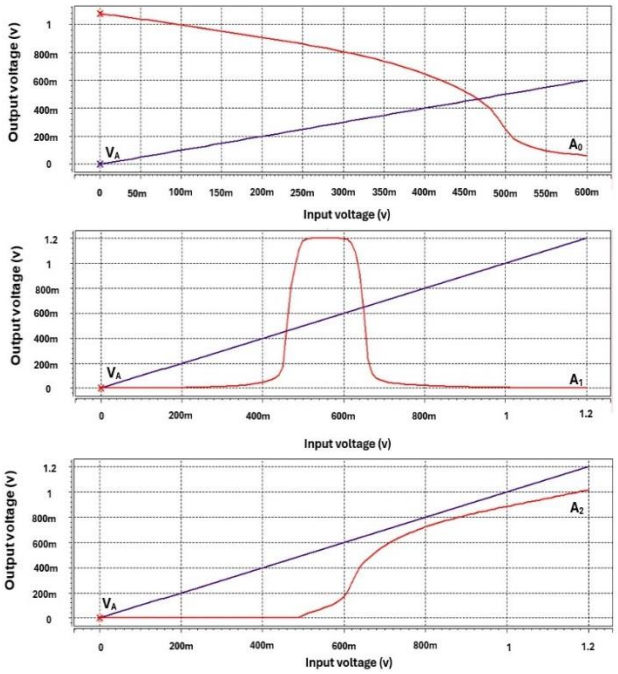


Fig. 13: Noise margin graphs for all outputs.

The high noise margin (NM_H) and low noise margin (NM_L) values for all three decoder output modes are given in Table 4. Higher noise margins mean better immunity to electrical noise, ensuring stable operation. From Table 4, the proposed decoder has good stability against noise.

Table 4: Noise margin values for the proposed decoder

Output	Low Noise Margin (NM_L)	High Noise Margin (NM_H)	Noise Margin (NM)
A_0	0.19264 V	0.51763 V	0.19264 V
A_1	0.51413 V	0.78267 V	0.51413 V
A_2	0.83079 V	0.51861 V	0.51861 V

Tables 3, 5 and 6 indicate that the power–delay product of all proposed ternary decoders employing two ternary inverters and one binary NOR gate is lower than that of the best existing ternary decoder designs.

Comparing the CMOS ternary decoder with other ternary decoder studies in terms of the number of transistors shows a 37.5% reduction in transistors compared to the circuit in [22] and a 16.66% reduction in transistors compared to the circuit in [14]. For a correct comparison, Table 5 shows the results of previous papers in 90 nm technology and circuit conditions under Table 3 conditions for ternary decoders. It shows that even under conditions similar to this paper, the proposed structure still has a high ability because it has high speed and low power consumption compared to the past works.

Table 5: Comparison of power, delay, and PDP with other studies

Number of transistors	PC (µW)	PD (ns)	PDP (fJ)	References
10	25	0.07	1.75	This model
14	30.62	0.0555	1.7	[34]
16	28.61	0.0514	1.47	[32], [33]

Table 6 shows a comparison of ternary to binary converters in previous research and this research, with different techniques. Here, the PDP of this research is much better than the best PDP of previous research [14]. Also, the speed of the proposed decoder is 2 times faster than the best decoder in the previous papers [14].

Table 6: Comparison with different technologies

Technology	PC (µW)	PD (ns)	PDP (fJ)	Inputs: Outputs	References
CMOS	25	0.07	1.75	1:3	This model
DPL	13	0.14	1.82	1:3	[20]
DPL	177.74	0.72	128	2:4	[34]
CMOS	361.45	1.319	476	2:4	[35]

Ternary decoders include configurations such as 1×3, 2×9, and others. Owing to its simplicity and its ability to illustrate the core concept of the paper, the 1×3 decoder is discussed in detail. The 2×9 decoder is also examined. In this decoder, the outputs of two 1x3 decoders are connected with a NOR gate and produce 9 outputs. The results are obtained as delay=0.95901 ns, average power=112.99 µW, and PDP=108.3 fJ. According to the new results obtained from the 2x9 decoder and Table 6, the CMOS technology in the 2x9 decoder has higher speed and appropriate power consumption compared to the decoders of other studies. This ternary decoder can be used as the main element in full adders (FAs) and digital signal processors (DSPs), and due to its high speed, it causes fast decoding.

Conclusion

Due to the application and advantage of ternary logic over binary, a ternary decoder with CMOS technique is designed that has fewer elements, a smaller area, and high speed compared to the existing ternary decoders. This new decoder includes only two ternary inverters and one binary NOR gate. One of the inverters is used as a negative ternary inverter (NTI) and a positive ternary inverter (PTI), simultaneously. Also, the use of a binary NOR gate eliminates don't care states and reduces the circuit area. The number of transistors in this ternary decoder is 10, its power consumption is 26.393 µW, and its propagation delay is 0.095 ns, which shows a 16.66% reduction in transistor numbers and a two times increase in speed compared to the best decoder studied in the previous research. This decoder can be used in full adders (FAs) and digital signal processors (DSPs), and due to its high speed, it can be used in fast decoding structures.

Author Contributions

SM. Mousavi monazah: Conceptualization, Methodology, Visualization, Data curation, Writing-original draft

N. Shiri: Supervision, Project administration, Conceptualization, Methodology, Visualization, Editing.

M. Rafiee: Writing-review & editing, Data curation, Layout.

A. Sadeghi: Writing-review & editing, Data curation, Visualization.

Acknowledgment

This work is completely self-supporting, thereby no financial agency's role is available.

Funding

This research received no external funding.

Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the

ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy, have been completely witnessed by the authors.

Abbreviations

PTI	Positive ternary inverter
CMOS	Complementary metal-oxide-semiconductor
DPL	Double pass logic
GDI	Gate diffusion input
PTL	Pass transistor logic
PDP	Power delay product
FAs	Full adders
DSP	Digital signal processors

References

[1] S. Rafiei, N. Shiri, "A neural network-based error correction in the first-stage residue of pipelined analog to digital converters," Int. J. Circuit Theory Appl. 52(12): 6001-6027, 2024.

[2] M. Tahghigh, N. Shiri, "A new ripple carry adder structure based on a swing-boosted full adder for concurrent error correction in low-resolution pipeline analog-to-digital converters," Int. J. Circuit Theory Appl., 52(9): 4741-4754, 2024.

[3] D. Etiemble, "Evolution of technologies and multivalued circuits," arXiv preprint arXiv:1907.01451, 2019.

[4] S. Reich, M. Sporer, M. Haas, J. Becker, M. Schüttler, M. Ortmanns, "A high-voltage compliance, 32-channel digitally interfaced neuromodulation system on chip," IEEE J. Solid-State Circuits, 56(8): 2476-2487, 2021.

[5] S. Thomas, J. S. Virdi, A. Babakhani, I. P. Roberts, "A survey on advancements in THz technology for 6G: Systems, circuits, antennas, and experiments," IEEE Open J. Commun. Soc., 6: 1998-2016, 2025.

[6] S. Pyle, "Leveraging the intrinsic switching behaviors of spintronic devices for digital and neuromorphic circuits," 2019.

[7] S. M. M. Monazah, M. R. Salehi, F. Emami, M. Salehi, "Design and numerical analysis of a highly sensitive nano-layer coated photonic crystal fiber biosensor," Laser Phys., 33(8): 086201, 2023.

[8] H. O. Ramos et al., "Enhanced implementation of a state machine-based decoder for optimal modulation of multilevel converters," Comput. Electr. Eng., 115: 109102, 2024.

[9] K. Qin, W. Hu, X. Yan, S. Yang, H. Cui, M. Wang, "A hybrid SAR ADC with input range extension," Microelectron. J., 150, 106259, 2024.

[10] A. Doostaregan, A. Abrishamifar, "Evaluating a methodology for designing CNFET-based ternary circuits," Circuits Syst. Signal Process., 39: 5939-5058, 2020.

[11] D. Manikkule, P. Jaronde, "Design of decoder using ternary inverter," in Proc. 2019 IEEE 5th International Conference for Convergence in Technology (I2CT): 1-3, 2019.

[12] B. Kim, "Inkjet-printed ternary inverter circuits with tunable middle logic voltages," Adv. Electron. Mater., 6(10), 2000426, 2020.

[13] Y. Yasuda, Y. Tokuda, S. Zaima, K. Pak, T. Nakamura, A. Yoshida, "Realization of quaternary logic circuits by n-channel MOS devices," IEEE J. Solid-State Circuits, 21(1): 162-168, 1986.

[14] Z. T. Sandhie, J. A. Patel, F. U. Ahmed, M. H. Chowdhury, "Investigation of multiple-valued logic technologies for beyond-binary era," ACM Comput. Surv., 54(1): 1-30, 2021.

[15] S. L. Murotiya, A. Gupta, "Design of CNTFET-based 2-bit ternary ALU for nanoelectronics," Int. J. Electron., 101(9): 1244-1257, 2014.

[16] S. K. Sahoo, G. Akhilesh, R. Sahoo, M. Muglikar, "High-performance ternary adder using CNTFET," IEEE Trans. Nanotechnol., 16(3): 368-374, 2017.

[17] S. M. Mousavi Monazah, F. Emami, M. R. Salehi, A. Hajilari, "Detection of cancer cells with selective photonic crystal fiber based on fuzzy logic," Opt. Quantum Electron., 55(5): 440, 2023.

[18] Y. Kang et al., "A novel ternary multiplier based on ternary CMOS compact model," in Proc. 2017 IEEE 47th International Symposium on Multiple-Valued Logic (ISMVL): 25-30, 2017.

[19] J. Ko, J. Kim, T. Jeong, J. Jeong, T. Song, "Exploration of ternary logic using T-CMOS for circuit-level design," IEEE Trans. Circuits Syst. I: Reg. Pap., 70(9): 3612-3624, 2023.

[20] R. Jaber, A. Elhajj, L. Nimri, A. Haidar, "A novel implementation of ternary decoder using CMOS DPL binary gates," in Proc. 2018 International Arab Conference on Information Technology (ACIT): 1-3, 2018.

[21] D. Das, A. Banerjee, V. Prasad, "Design of ternary logic circuits using CNTFET," in Proc. 2018 International Symposium on Devices, Circuits and Systems (ISDCS): 1-6, 2018.

[22] A. Doostaregan, M. H. Moaiyeri, K. Navi, O. Hashemipour, "On the design of new low-power CMOS standard ternary logic gates," in Proc. 2010 15th CSI International Symposium on Computer Architecture and Digital Systems: 115-120, 2010.

[23] F. Bahrami, N. Shiri, F. Pesaran, "A new approximate sum of absolute differences unit for bioimages processing," IEEE Embedded Syst. Lett., 16(1): 13-16, 2023.

[24] E. Esmaeili, N. Shiri, M. Rafiee, A. Sadeghi, "A multiplier-free discrete cosine transform architecture using approximate full adder and subtractor," IEEE Embedded Syst. Lett., 16(4): 441-444, 2024.

[25] N. Shiri, A. Sadeghi, M. Rafiee, "High-efficient and error-resilient gate diffusion input-based approximate full adders for complex multistage rapid structures," Comput. Electr. Eng., 109: 108776, 2023.

[26] X. Hu, J. S. Friedman, "Hybrid pass transistor logic with dual-gate ambipolar CNTFETs," arXiv preprint arXiv:2002.01932, 2020.

[27] D. Satyanarayana et al., "Design of efficient multiplier with low power and high-speed using PTL (Pass Transistor Logic)," Int. J. Electron. Telecommun., 71(2): 483-488, 2025.

[28] S. Nagaraj, G. S. Reddy, S. A. Mastani, "Analysis of different Adders using CMOS, CPL and DPL logic," in Proc. 2017 14th IEEE India Council International Conference (INDICON): 1-6, 2017.

[29] G. Mahendran, "CMOS full adder cells based on modified full swing restored complementary pass transistor logic for energy efficient high speed arithmetic applications," Integration, 95: 102132, 2024.

[30] K. Xu, "Integrated silicon directly modulated light source using p-well in standard CMOS technology," IEEE Sensors J., 16(16): 6184-6191, 2016.

[31] V. Bespalov, N. Dyuzhev, V. Y. Kireev, "Possibilities and limitations of CMOS Technology for the production of various Microelectronic systems and devices," Nanobiotechnol. Rep., 17(1): 24-38, 2022.

[32] R. A. Jaber, A. M. El-Hajj, A. Kassem, L. A. Nimri, A. M. Haidar, "CNFET-based designs of Ternary Half-Adder using a novel "decoder-less" ternary multiplexer based on unary operators," Microelectron. J., 96, 104698, 2020.

[33] S. Lin, Y. B. Kim, F. Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits," IEEE Trans. Nanotechnol., 10(2): 217-225, 2009.

[34] A. Saha, D. Pal, "DPL-based novel time equalized CMOS ternary-to-binary converter," Int. J. Electron., 107(3): 431-443, 2020.

[35] J. R. Sathiaraj, "Ternary to binary converter design in CMOS using multiple input floating gate MOSFETS," Louisiana State University and Agricultural & Mechanical College ProQuest, Dissertations & Theses, 2009.

Biographies

Seyede Mahboobeh Mousavi Monazah received her B.Sc. and M.Sc. degrees in Electrical Engineering from Islamic Azad University, Shiraz, Iran in 2016 and 2019, respectively, and Ph.D. degree in Electrical Engineering from Shiraz University of Technology, Shiraz, Iran in 2024. Her major research interests include Electronics, optimization, optics, photonics and optical fibers.

- Email: m.mousavi-monazah@sutech.ac.ir
- ORCID: 0009-0002-3736-8100
- Web of Science Researcher ID: NA
- Scopus Author ID:NA
- Homepage: NA

Nabiollah Shiri is an Assistant Professor of Electronics with the Department of Electrical Engineering, at Islamic Azad University, Shiraz Branch, Shiraz, Iran. His research interests include integrated circuits (ICs), mixed-mode circuits, approximate circuits, bioelectronics ICs, arithmetic circuit design, and biosensors.

- Email: na.shiri@iau.ac.ir
- ORCID: 0000-0003-4683-1814
- Web of Science Researcher ID: NA
- Scopus Author ID:NA
- Homepage: NA

Mahmood Rafiee received a B.Sc. degree in Electrical Engineering from Islamic Azad University, Shiraz, Iran in 2016 where he is currently toward an M.Sc. degree in VLSI design engineering. His current research contains VLSI design, ultra-low-power digital circuits, and physical structure validation of MOSFETs, CNTFETs, and MBCFETs.

- Email: rafieee.mahmood@gmail.com
- ORCID: 0000-0003-1585-6859
- Web of Science Researcher ID: NA
- Scopus Author ID:NA
- Homepage: NA

Ayoub Sadeghi received a B.Sc. degree in Electronic Engineering from Islamic Azad University, Shiraz, Iran in 2016 where he finished his M.Sc. degree in VLSI design engineering in 2019. He is currently a Ph.D. student at the University of Illinois Chicago and works on high-efficient arithmetic circuits design, approximate computing, and power converters.

- Email: asadeg3@uic.edu
- ORCID: 0000-0001-9904-9813
- Web of Science Researcher ID: NA
- Scopus Author ID:NA
- Homepage: NA