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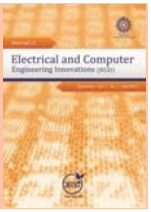

A High Efficiency Low-Voltage Soft Switching DC–DC Converter for Portable Applications

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ABSTRACT

This paper presents a novel control method to improve the efficiency of low-voltage DC-DC converters at light loads. Pulse Width Modulation (PWM) converters have poor efficiencies at light loads, while pulse frequency modulation (PFM) control is more efficient for the same cases. Switching losses constitute a major portion of the total power loss at light loads. To decrease the switching losses and to increase efficiency, converters based on soft-switching are utilized. This paper presents the design of a soft-switching DC-DC buck converter in a 90-nm CMOS technology. Simulation results by HSPICE shows a 21 mV output ripple on a 0.5 V output voltage for an input voltage of 1.4 V. Finally, the efficiency of 95% at a load current of 50 mA having 74 mA of current ripple is achievable.

1. INTRODUCTION

Battery-powered, portable electronic devices like cellular phones, laptop computers, PDAs, digital cameras, pagers, etc. need to possess high efficiencies in order to increase the time of battery usage [1]. Due to recent developments in the technology, the dimensions of CMOS transistors and subsequently the supply voltage of integrated circuits have been reduced [2]. This benefit has made low voltage integrated DC-DC converters applicable to portable devices. Moreover, it has not only lowered the voltage and power consumption, but also it has many benefits in reducing the size, weight and overall costs [3]. Usually, in these portable communication devices, the load conditions vary frequently from low to high power levels (e.x. stand-by mode to talking mode) and these devices are often used with light loads. Improving the light load efficiency in DC-DC converter is important for increasing the battery's lifetime [4].

By the use of PWM control, the switching frequency is fixed while the application period is changed to regulate the output voltage [5]. On the other hand, in PFM control, the switching frequency changes by changing the load current. A typical PWM switching has a lower efficiency in light loads due to the loss of the upper switch. The switch loss which is the main portion of the total power loss will decrease by reducing the switching frequency in PWM mode. On the other hand reducing the switching frequency increases the inductor's and the power transistor's peak current which not only causes a higher power dissipation, but also increases the circuit size which, in turn, increases the costs. Switching power supplies with PFM control have more efficiency for light loads; because the switching frequency and the switching dissipation are lowered by reducing the load current [6].

Another way to improve the efficiency is by using the soft switching technique which has received much attention in recent years. DC-DC converters with soft switching will reduce the switching losses, a major portion of power dissipation, and will increase the efficiency. The resonant technique is a major one in implementing soft switching converters. The main advantage of these converters is to reduce the switching losses which are achieved by zero-current switching (ZCS) and zero-voltage switching (ZVS) techniques. Different topologies are reported for soft switching. In portable applications that size, weight

and price are very important, quasi-square-wave converters (QSW) are the best option because only a single resonant components is used in it (the resonant capacitor). Figure 1 depicts the schematic and the waveform of a conventional QSW ZVS buck converter. In this arrangement, a reverse current in the inductor is utilized to charge the resonant capacitor during the dead time [1].

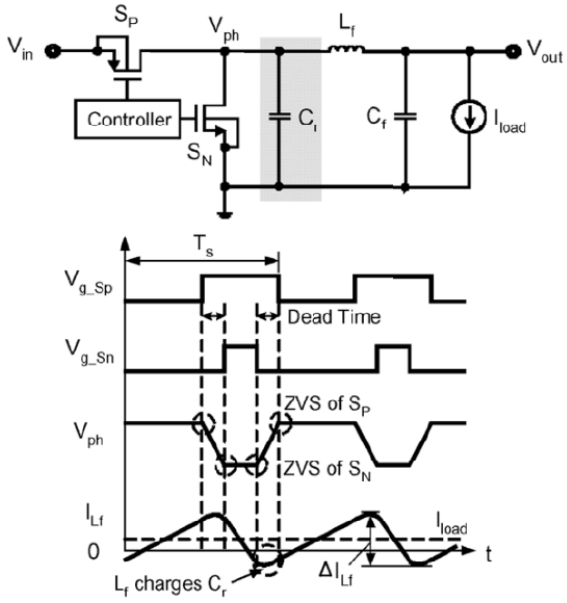


Figure 1: Circuit schematic and waveform of a conventional QSW ZVS buck converter [1].

In this paper, a synchronous buck converter with PFM control and soft switching for light loads is presented. The structure of this paper is as follows: In section two, some PFM control methods are described briefly and the desired control method is investigated. Some equations are provided for the calculation of the inductor and the capacitor values of the output filter. Then, the synchronous buck converter with PFM control and soft switching is described. In the third section, we present an integrated and a discrete circuit for the implementation of the design. In section four the results from simulations and measurements of the synchronous buck converter with PFM control and soft switching are presented. Finally, a conclusion is presented in the fifth section.

2. PFM Controller Design

Figure 2 illustrates the schematic of a synchronous buck converter with PFM control and the waveform of the inductor's current with PFM control in discontinuous conduction mode. t_{on} is a time segment within time period T in which the PMOS transistor is ON while the NMOS transistor is OFF. In this period, energy is saved in the inductor which maintains the output current as well as the capacitor's charging current. When the PMOS is OFF, the inductor's stored energy is transferred to the output capacitor and the inductor's current turns to zero via the NMOS transistor. During T_{Idle}, both switches stay OFF and the capacitor provides the required output current [6].

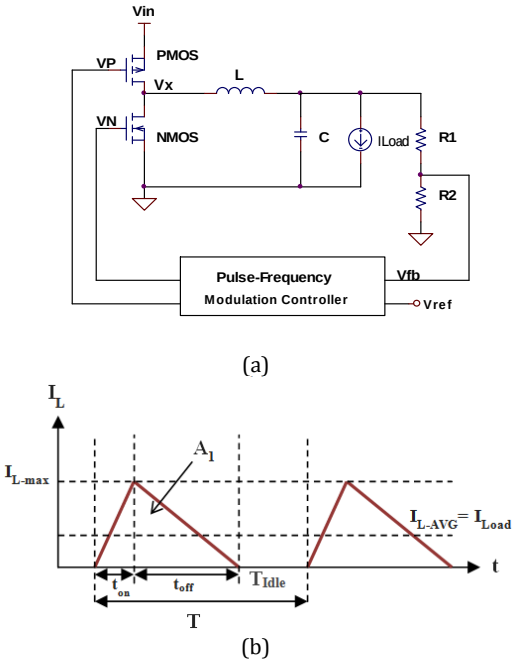


Figure 2: (a) Schematic of synchronous buck converter with PFM control. (b) Waveform of the inductor's current with PFM control.

There are different ways in order to reach PFM functionality such as constant inductor's peak current ($I_{L\text{-}max}$), constant ON-time (t_{on}) and constant OFF-time (t_{off}) all related to the PMOS transistor [7]. As can be seen in Figure 2(b), the period of storing and releasing the inductor's energy (t_{on}, t_{off}) is obtained through the following equations, respectively:

$$t_{on} = I_{L,\max}\frac{L}{Vin - Vout} \quad , \quad t_{off} = I_{L,\max}\frac{L}{Vout} \tag{1}$$

In the mode with a fixed inductor's peak current, when the control pulses of VP and VN is zero, the PMOS transistor turns ON and the NMOS transistor turns OFF. The inductor current increases linearly and the current reaches $I_{L\text{-}max}$. The control pulse is one, the PMOS transistor turns OFF and the NMOS transistor turns ON. Thus the inductor's current reduces linearly. When the current reaches zero, the PMOS transistor is ON and, thus, the cycle is repeated [8]. The load current is approximately equal to the average of the inductor's current and it is obtained via the following equations:

$$I_{Load} \cong \frac{A_1}{T} = \frac{I_{L,\max}^2}{2T}\frac{L}{Vout\left(1 - \frac{Vout}{Vin}\right)} \tag{2}$$

The switching frequency in the PFM mode with constant inductor's peak current $I_{L\text{-}max}$ can be calculated as follows:

$$F = \frac{1}{T} \cong \frac{2}{I_{L,\max}^2 \times L} Vout\left(1 - \frac{Vout}{Vin}\right) I_{Load} \tag{3}$$

Based on the waveform of the DCM convertor, the switching frequency for the constant ON-time t_{on} or the constant OFF-time t_{off} is obtained as follows:

$$F \cong \frac{2LVout}{t_{on}^2 Vin(Vin-Vout)} \cdot I_{Load} \quad (4)$$

$$F \cong \frac{2L}{t_{off}^2 Vout} \cdot \left(1-\frac{Vout}{Vin}\right) \cdot I_{Load} \quad (5)$$

According to equations (3), (4) and (5), the switching frequency of each PFM mode is determined by I_{LOAD} (load current) and by either t_{on}, t_{off} or $I_{L\text{-}max}$. The less the load current, the less the switching frequency. Hence, the consumable power, which is dependent on the switching frequency, can be reduced by the use of PFM control and the efficiency can be improved effectively [9].

A. Adaptive ON-Time PFM Control

In some applications, like Li-ion batteries, the input voltage range is 2.7 - 4.2 V. If t_{on} is designed for a narrow range of input voltages, the inductor's peak current and its stored energy is less than the state in which t_{on} is designed for a broad range of input voltage; because increasing the current linearly is appropriate with input voltage. As a result, the converter needs a quick operation of the switch to maintain regulation which leads to an increase in switching loss. On the other hand, if t_{on} is designed for a broader range of supply voltages, while the converter operates in a broad range of input voltage, the peak current is higher and consequently it causes the larger ripple in the output voltage. According to the ON-time equations, the switching state of PMOS transistor is a function of input voltage, output voltage and the inductor's peak current. According to the previous equations, the inductor's peak current may be written as:

$$I_{L,\max} = \sqrt{\frac{2C\Delta V}{L}\left|\frac{Vin-Vout}{Vin}\right|Vout} \quad (6)$$

Controlling a constant ON-time for a wide range of input voltages causes to have a variable inductor's current and consequently a variable ripple in the output voltage. To overcome this situation and to stabilize the output voltage ripple, the converter ON-time is set dynamically by changing the source voltage. In [6] a method is presented for PFM control with adaptive ON-time method.

In the design presented in [4], the PFM modulator circuit diagram includes two comparators and an SR latch, as can be seen in Figure 3. According to equation (6), the slope of the inductor's current will change proportional to the difference between input voltage V_{in} and output voltage V_{out}:

$$\Delta I_L = \frac{t_{on}(Vin-Vout)}{L} \quad (7)$$

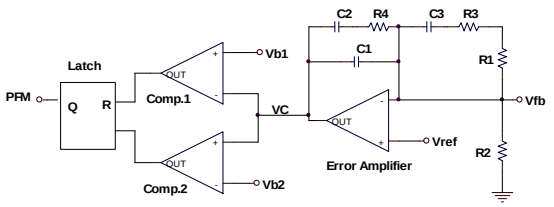


Figure 3: Schematics of PFM modulator.

For a larger V_{in}, V_{out} can reach the specified voltage in a shorter time which means by increasing V_{in}, the ON-time would be smaller. As a result, the converter's ON-time will be set with the supply voltage adaptively.

Additionally, adjusting the comparator's input voltage can adjust the output voltage ripple. It is important to note that the voltage ripple needs to be compromised with efficiency. Error signal Vc will change by changing the output voltage changed due to power level. If Vc is larger than V_{b2}, both the output of Comp.2 and the output of the SR flip-flop (Q), will be 1. If Vc is less than Vb1, the output of Comp.1 will be 1 and Q will be 0. This process is somehow similar to the one in hysteresis comparators [4].

B. Output Filter Characterization

The PFM functionality is described in the previous section. The converter operates in DCM mode. The PMOS transistor is turned on during t_{on} and the inductor's current I_L is increased and is divided between the load's and the capacitor's charge currents. When the PMOS transistor is OFF, the inductor's stored energy is transferred to the output capacitor and the inductor's current turns to zero via the body diode of the NMOS transistor then through the NMOS synchronous switch (equation 1).

When the inductor's current is zero, the NMOS switch is turned ON. In this time period, the PMOS switch remains OFF. The Inductor's current is zero and the output capacitor provides the required load current. The total energy stored in the inductor, in a switching period, is equal to the area under the curve of the inductor's current waveform:

$$Q_L = \frac{1}{2} I_{L,\max}\left(t_{on}+t_{off}\right) \quad (8)$$

In which $I_{L,max}$ equals:

$$I_{L,\max} = \frac{t_{on}(Vin-Vout)}{L} = \frac{t_{off}(Vout)}{L} \quad (9)$$

Using the equations (8) and (9), the energy stored in the inductor in a switching period is:

$$Q_L = \frac{1}{2}\frac{t_{on}^2(Vin-Vout)Vin}{LVout} \quad (10)$$

Regardless of the mount of power loss in the converter and assuming that the circuit's input

reference adjusts the output properly, the total charge stored in the inductor is equal to the charge which is delivered to the load:

$$Q_L = I_{out}.T \tag{11}$$

In which:

$$T = t_{on} + t_{off} + t_{Idle} \tag{12}$$

Inductor value: The inductor value for the maximum load current I_{out}(max) is:

$$L = \frac{t_{on}(Viv - Vout)}{2I_{out(\max)}} \tag{13}$$

Capacitor value: In the worst case, assuming that the total inductor's current is delivered to capacitor C, the output voltage ripple is calculated by the equation:

$$\Delta V = \frac{Q_L}{C} \tag{14}$$

The inductor's peak current and consequently the PMOS transistor's ON-time is determined in a way that according to the required application, the output voltage ripple remains in an acceptable range [10].

C. PFM Controller with Soft Switching

Figure 4 conveys a detailed schematic of the mentioned buck converter with variable frequency control and soft switching capability. The inductor L and the capacitor C are the output filter's components. The resonant capacitor Cr is added to the synchronous buck converter for soft switching which was indicated in Figure 2. The capacitor's voltage cannot be changed momently. The Vx node is the connecting node between the NMOS-PMOS power transistors and the inductor L. Its voltage is determined by the ON/OFF state of the power transistors and also their peak currents. When the inductor current reduces, due to the NMOS transistor being ON and the PMOS transistor being OFF, the Vx node's voltage can go below zero. By including Cr and adjusting the proper dead time, the Vx voltage will be higher than zero. When the PMOS transistor already remains OFF and the NMOS transistor is also OFF (during the dead time), Cr is charged inversely. As a result, less power is lost in the switch due to the resonant capacitor.

3. Circuit Implementation

Integrated circuits are developed using different technologies. By ever increasing advances in the CMOS technology, the dimensions of this device become smaller and subsequently the number of transistors on a chip increases. As a consequence, the supply voltages of the integrated circuits are also diminished.

An optimal design of switching power supplies leads to a reduction in their size and power consumption. Meanwhile, in designing DC-DC converters for portable applications, there should be a compromise among size, cost and easy design [10].

A. Designing a Synchronous Buck Converter with PFM Control and Soft Switching in a 90 nm CMOS Process

The minimum input voltage to a converter is determined by the technology used in fabrication, power transistor's threshold voltage and the drain-source saturation voltage. When the PMOS and NMOS transistors' threshold voltages are respectively 0.95 V and 0.75 V, the input voltage equals 1.4 V which is sufficient for a synchronous buck converter.

Today, however, a PMOS device with a 0.5-0.6 V threshold voltage is used in many technologies which will reach a minimum input voltage of around 1 V. In Figure 5, the reader can see the schematic of the designed synchronous buck converter with soft switching in a 90 nm CMOS process.

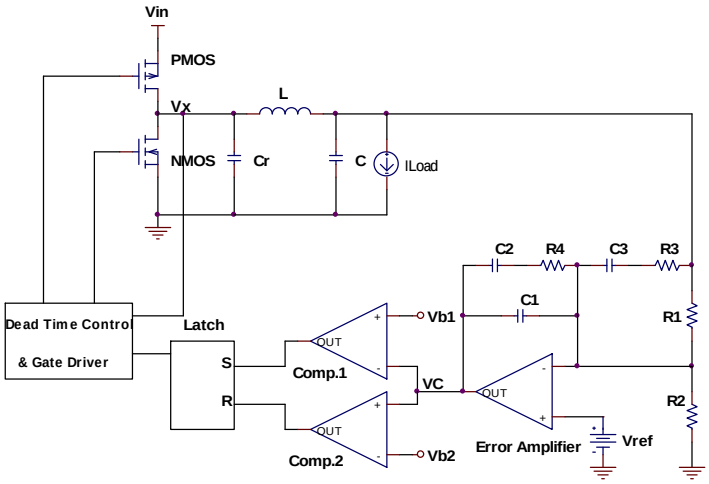


Figure 4: The proposed buck converter.

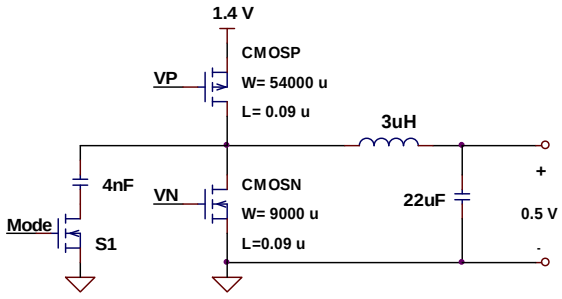


Figure 5: Schematic of a synchronous buck converter with soft switching in a 90 nm CMOS process.

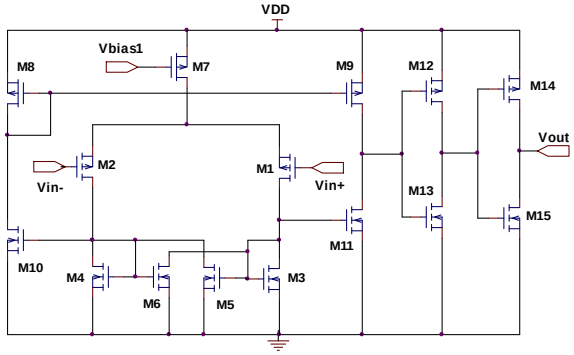


Figure 6: Schematic of the comparator.

Compared to a conventional hard-switched buck converter, an auxiliary NMOS switch (S1), a resonant capacitor (Cr) and the corresponding control circuits are added. The external signal "Mode" is selected according to the load current. For heavy loads, Mode is low, so S1 is disabled and Cr is disconnected from ground. The converter operates as a conventional hard-switched one. For light loads, Mode is high, so Cr is connected to ground via an auxiliary switch. The supply voltage equals 1.4 V and L=3 µH, C=22 µF and Cr=4 nF. The 0.5 V output was derived from a 1.4 V input supply voltage. The minimum effective channel length, L= 0.09 µm, is used. The CMOSP and CMOSN channel widths are 54000 µm and 9000 µm, respectively.

Comparator: Figure 6 represents the comparator circuit. Comparators require a *saw-tooth Wave Generator* and PWM and PFM modulators. These comparators are implemented by a differential pair with PMOS input and a positive feedback for providing high efficiency [4].

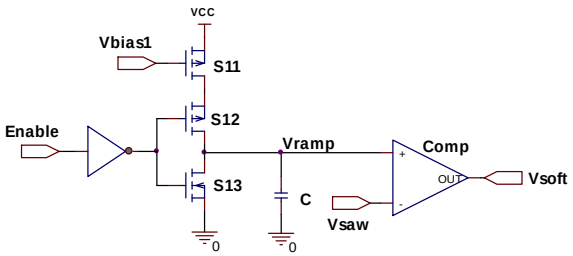
Soft-start: The aim of the soft-start circuit in buck convertor is to prevent a severe tuck during start-up which may damage the power transistors. The soft-start circuit is depicted in Figure 7(a). The Voltage V_{ramp} increases gradually to charge the capacitor and is compared to a saw tooth wave in the same Figure. As can be seen in Figure 7(b), a series of pulses with slowly increasing duty cycles are generated. This circuit can also prevent damages from large transient currents in the circuit [4].

B. Designing Buck Converters with PFM Control in Discrete Form

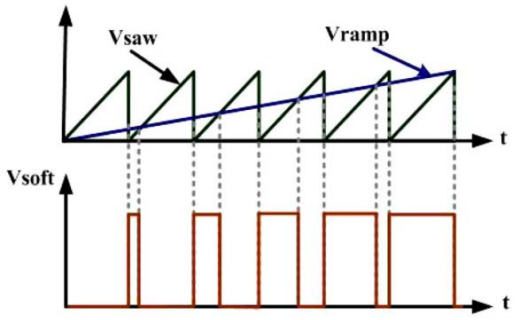
The aim of the discrete design was to ensure the accuracy of a conventional hard-switched buck converter with PFM control and its control circuits. After simulation in PSPICE, we implemented it on a PCB prototype.

In our design, an IRF9630 PMOS transistor plays the role of the main power transistor. The selected NMOS power transistor is IRF460. A 7667ICL driver is used in order to launch the power transistor gates. The PFM unit control, as can be seen in Figure 8, contains two comparators, an SR latch and a driving IC. Comparators are of LM339. The SR latch is composed of two NOR gates with two inputs with the appearance which is shown in Figure 8.

The 7402 IC consists four NOR gates with two inputs which two of them are used in this work. The Vc error signal changes by changing output voltage of power stage. When the output voltage falls, Vc rises and vice versa. If the Vc error signal is smaller than Vb1, Comp.1 becomes one. Q output falls and the Vg controlling pulse equals one. So, the PMOS is OFF and the NMOS is ON. If VEA is greater than V_{b2}, the Comp.2 output is one. Consequently, Q is equal to one and VG falls. In this state, the PMOS and NMOS transistors turn ON and OFF respectively in order to adjust the output voltage. In our design, V_{b1} value is equal to 0.9 V and Vb2 value is equal to 0.91 V.



(a)



(b)

Figure 7: (a) Schematic of the soft-start circuit. (b) The generation of the gradually increased pulse width chain [4].

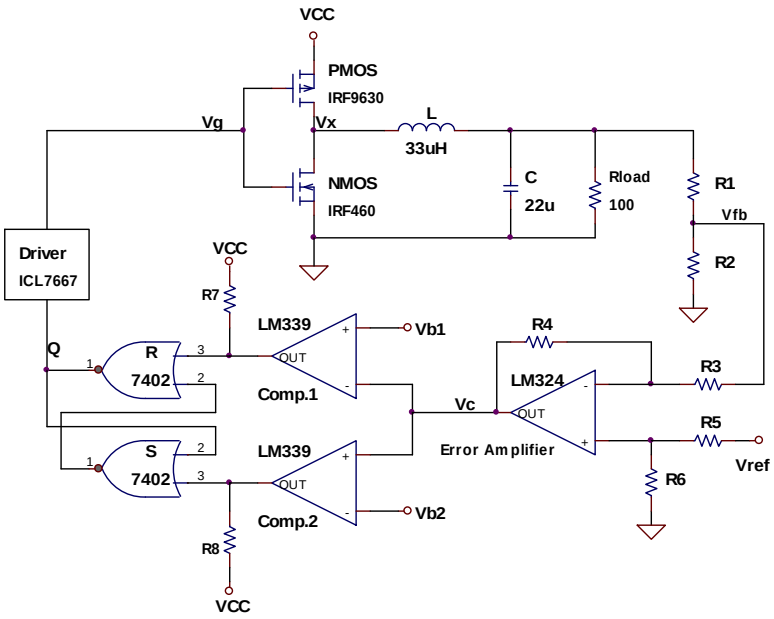


Figure 8: Circuit of the Buck converter working in PFM mode.

4. Simulation and Experimental Results

Before fabricating the discrete circuit, the design was simulated in PSPICE and then it was implemented on a PCB prototype. The double side PCB of the hard-switched buck convertor with PFM control and its assembled circuit are shown in Figure 9. Table 1 consists a short part list and some features of the designed discrete circuit.

In Figure 10 the output voltage of the synchronous buck converter with PFM control and hard switching for a load current of 30 mA is illustrated to be 1.8 V.

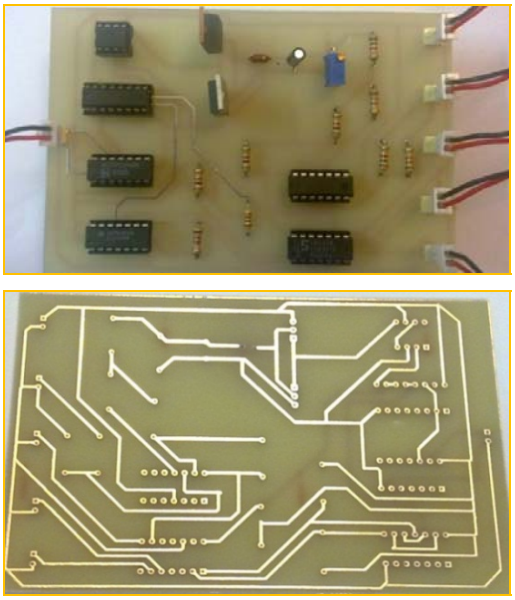


Figure 9: PCB and assembly circuit of synchronous buck converter with PFM control and hard switch.

Table 1
Converter Parameters Implemented on PCB

Component	Parameters
Input Voltage	5 V
Output Voltage	1.2 , 1.8 V
Load Current	10 – 100 mA
PMOS	IRF9630
NMOS	IRF640
L	33 µH
C	22 µF
C_r	4 nF
Operational Amplifier	LM324
Analog Comparator	LM339
Gate Driver	ICL7667

By increasing the load current, the operating frequency and the output voltage ripple increase too. In Figure 11 (a) and (b), the converter operates with PFM control and hard switching; output voltage ripple in 26.3 KHz is equal to 32 mV and in 42.1 KHz equals 28 mV.

In the integrated design, the supply voltage is held at 1.4 V, L=3 µH, C=22 µF and C_r=4 µF. All designed control circuits are supplied with 1.4 V and the output voltage is equal to 0.5V. The designed circuits within a 90 nm CMOS process are simulated in HSPICE. In Figure 12 (a) and (b), the reader can see the signals applied to the gates of PMOS and NMOS transistors, respectively. Figure 12 (c) shows the voltage at node Vx. In this state, buck the converter operates with hard switching and the load current is equal to 20 mA.

As can be seen in Figure 13(a), the inductor's peak current is equal to 243 mA for a 11 mA load current. This converter operates in 37.50 KHz frequency. In

Figure 13(b), it is shown that the converter operates with 200 mA inductor's peak current and also with 23 mA of load current in 49.86 KHz frequency. Simulation results confirm that by reducing the load current, the working frequency reduces.

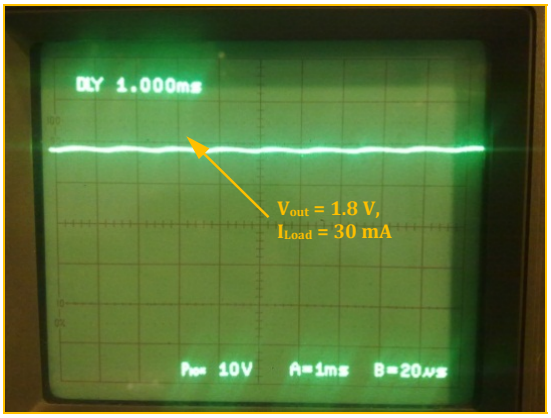
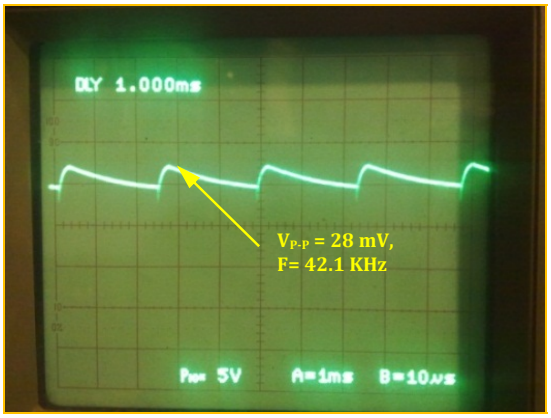
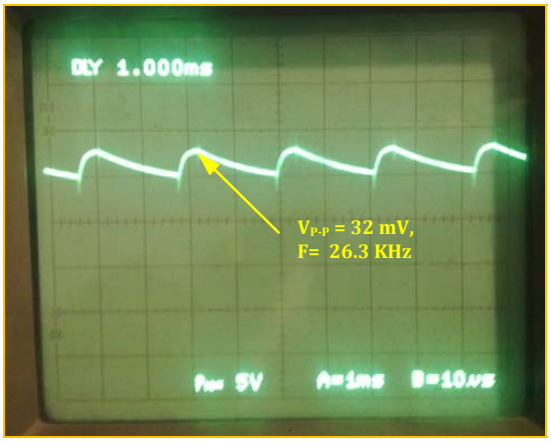


Figure 10: Experimental results of output voltage of designed buck converter in PWM mode.

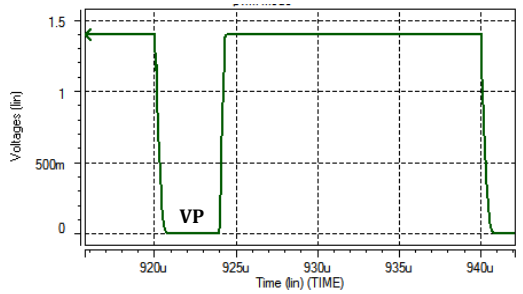


(a)

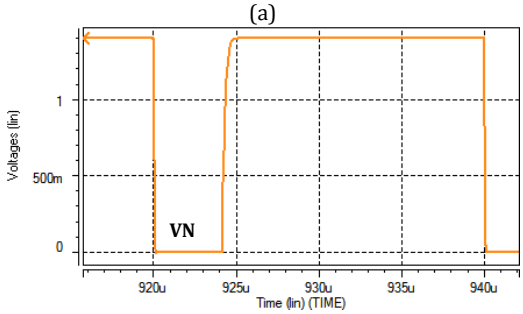


(b)

Figure 11: experimental results of output voltage ripple in PFM mode. (a) V_{P-P} = 28 mV. (b) V_{P-P} = 32 mV.



(a)



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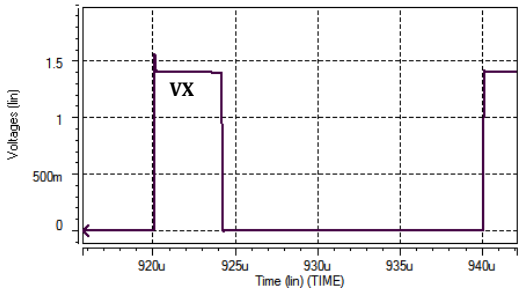

(c)

Figure 12: Simulation results of buck converter with hard switch in 20 mA load current. a) Voltage applied to PMOS transistor gate. b) Voltage applied to NMOS transistor gate. c) The node voltage Vx.

In Figure 14, you can see the voltage applied to the gates of PMOS and NMOS transistors and also the voltage at node Vx.

Figure 15 shows the inductor's current. The load current is 30 mA and the inductor's current ripple is 77 mA.

In Figure 16, the efficiency of the mentioned converter is plotted, which is compared to the synchronous buck converter with hard switching. The efficiency of this converter in light loads is 72.3% - 80.2% which occurs for a load current range of 10 – 200 mA. Switching losses are not removed completely and an extra power loss is also added due to storing and offloading in the resonant capacitor Cr. Simulation results demonstrate that by applying the soft switching technique, power dissipation is reduced in total. For a load current of 50 mA, the overall loss with soft switching is reduced to 17 mW compared to the hard switching.

The efficiency has been raised from 68.2% to 72.3%. For a 150 mA load current, the overall loss has

reduced by 21.2 mW and the efficiency has increased by 2.2%. For a 200 mA load current, the efficiency has also increased by 1.5% while extra power loss is also added due to storing and offloading in the resonant capacitor Cr. Simulation results demonstrate that in total, by applying soft switching, power dissipation will reduce.

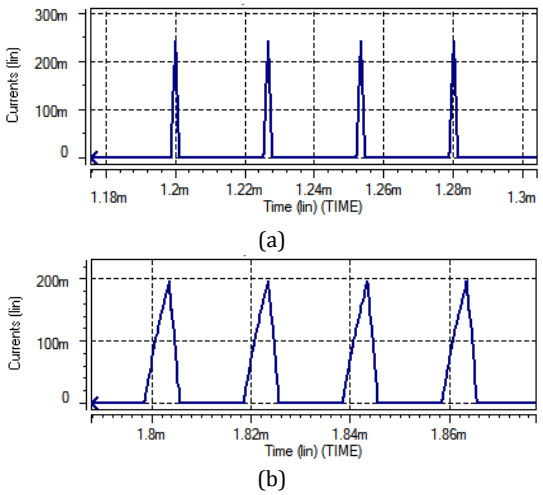

Figure 13: Steady-state measurement results with 1.8-V output voltage: (a) the inductor's current with load current of 11 mA and (b) the inductor's current with load current of 23 mA.

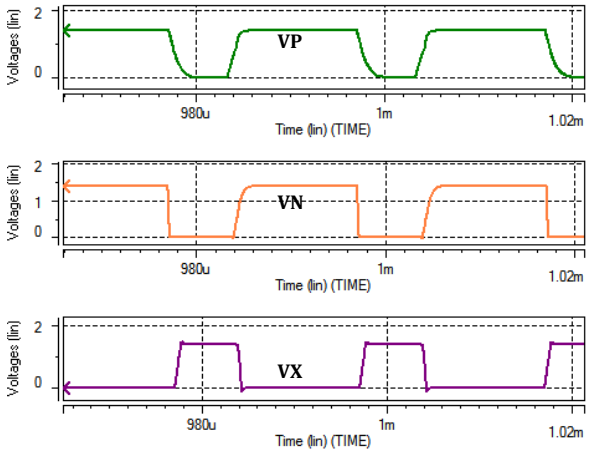

Figure 14: Simulation results of the voltage applied to the gates of PMOS and NMOS transistors and node voltage Vx related to the buck converter with PFM control and soft switching in 30mA load current.

5. Conclusion and Discussion

In this paper, a synchronous buck converter with PFM control and soft switching is presented. In portable applications such as cellular phones, size, weight and price are very important. Among various configurations reported for soft switching over the years, QSW converters are the most appropriate option due to the fewest added components.

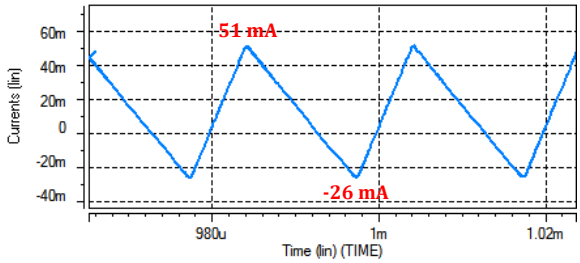

Figure 15: The inductor's current of the buck converter with PFM control and soft switching for a 30 mA load current.

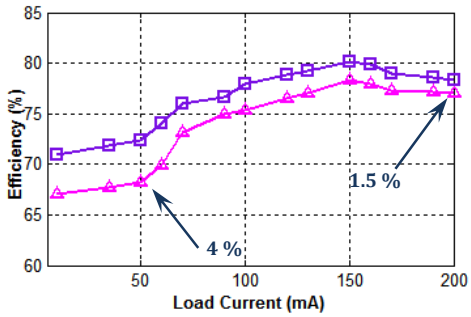

Figure 16: Comparing the efficiency of proposed converter and buck converter with hard switch.

Buck converters with PFM control and hard switching is constructed with discrete components and implemented on a PCB. Measurement results from the developed board confirmed that the PFM converter has a high efficiency in light loads.
Moreover, a QSW ZVS buck converter with PFM control in a 90 nm CMOS process was designed and simulated in HSPICE. The efficiency of the mentioned converter in a 50 mA load current has increased 4.1% compared to a synchronous buck converter with PFM control and hard switching. The maximum efficiency of this converter with a 1.4 V input voltage and a 0.5 V output voltage is 80.2% in a load current range of 10 – 200 mA.

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