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Research paper

Switched-Capacitor Enhanced A-Impedance Design for High-Density, High-Gain DC-DC Applications

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Abstract

Background and Objectives: Impedance source networks have gained significant attention in electrical energy conversion due to their ability to overcome the limitations of conventional methods. While existing impedance-based converters offer various advantages, challenges such as voltage gain limitations and component stress remain. This study introduces an advanced ultra-gain enhanced A-source (UGEA-S) DC/DC converter incorporating switched-capacitor technology to address these concerns and significantly improve voltage gain.
Methods: The proposed UGEA-S converter is designed to enhance energy conversion efficiency while minimizing voltage stress on switching elements. The topology integrates switched-capacitor techniques to achieve superior voltage gain, reducing reverse recovery issues in diodes and maintaining a continuous input current. A thorough theoretical analysis is conducted to explore its operational principles and steady-state behavior. Comparative assessments with other recently developed converters further highlight its distinct performance attributes. Additionally, MATLAB/Simulink simulations and experimental results are performed to validate the converter's functionality under practical operating conditions.
Results: Experimental, simulation, and numerical analysis confirm that the proposed UGEA-S converter achieves an ultra-high voltage gain of up to 8× (480 V output from a 60 V input) while maintaining low voltage stress across switching components. The MOSFET experiences a peak voltage of 230 V and a current of 28 A, which is well within its safe operating limits. Diodes D1–D4 exhibit voltage stresses ranging from 230 V to 520 V, with average currents between 2.65 A and 20.3 A. The input inductor sustains a continuous current of 19.5 A, validating the converter's smooth current profile. Efficiency measurements show a peak of 96.93% at 230 W output, with performance remaining above 92% even at full 1 kW load. These results demonstrate the converter's resilience under dynamic conditions and its suitability for high-performance applications such as electric vehicles and renewable energy systems.
Conclusion: The UGEA-S converter offers a robust and innovative solution for high-gain DC/DC conversion, addressing key limitations of conventional designs. Its exceptional voltage gain, reduced voltage stress, and stable current regulation make it a promising candidate for advanced energy systems. The findings underscore the converter's feasibility for real-world applications, particularly in electric vehicle power systems. Future research can further optimize its design for enhanced efficiency and broader scalability.

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Introduction

A vast array of electronic systems relies on a stable DC voltage supply. In fact, DC power supplies are integral to a myriad of applications, ranging from computing and telecommunications to medical devices and defense systems [1]. Broadly speaking, these power supplies fall into two main categories: linear regulators and switching converters. In linear regulators, transistors operate within their active regions, a stage that induces significant voltage drops and extensive power dissipation. This, in turn, results in relatively low efficiency. Despite their tendency to be bulky and heavy, linear regulators are prized for their minimal noise output, making them particularly advantageous for applications such as high-fidelity audio systems [2]. On the other hand, switch-mode converters leverage transistors that function as binary switches, alternating rapidly between on and off states. This mode of operation minimizes voltage losses and reduces power wastage dramatically, leading to a notably higher efficiency. However, it is important to acknowledge that at elevated operating frequencies, the inherent switching losses can become significant, potentially diminishing the overall efficiency of these converters [3]. In DC-DC switching converters, key design considerations include the device's size, volume, and cost, alongside the imperative of achieving high efficiency while delivering the desired voltage boost. Efficiency improvements can be attained by reducing both conduction losses and switching losses in the transistors and diodes [4]. Specifically, conduction losses can be minimized by lowering the converter's switching frequency and employing switches with low drain-source on-resistance. Another critical design aspect is the reduction of voltage stress across circuit components, which plays a vital role in ensuring optimal performance. Additionally, the nature of the input current waveform is essential; a continuous, low-ripple input current not only reduces stress on the source but also contributes to a longer operational lifespan [5], [6].

A. Related Works and Literature Review

Traditional step-up converters, such as boost converters, were employed to elevate voltage levels. Nonetheless, they encounter numerous drawbacks, including limited voltage gain, significant voltage and current stress on various components, heightened reverse recovery losses in high-voltage diodes, and reduced efficiency when operating at high voltage gains and power levels [7]. Increasing the transformer turn ratio and the duty cycle can significantly enhance the boost factor, as indicated in references [8] and [9]. However, this strategy comes with trade-offs. Elevated transformer ratios tend to boost leakage inductance, which in turn produces larger voltage spikes that diminish the converter's overall efficiency. Additionally, extending the duty cycle amplifies the conduction losses in the switching component.

Extensive investigations into a range of converter configurations have been undertaken to resolve these challenges. The primary focus has been on enhancing voltage amplification and operational efficiency while mitigating the stress caused by voltage and current on crucial semiconductor devices and passive elements within DC–DC converters [10]. Several methods have been utilized to achieve these objectives, including approaches such as voltage lifting, layered architecture, switched inductor cells (SICs), switched capacitor cells (SCCs), coupled inductors, interleaved input stages, cascading arrangements, resonance-based techniques and impedance networks (INs) [6].

INs-based converters, characterized by their enhanced boost capability, offer a viable alternative to traditional boost converters. These converter designs aim to provide multiple performance benefits, including superior voltage gains, diminished inrush currents, reduced stress on components, heightened efficiency, and a higher power density.

In 2003, the pioneering impedance Z-source converter was unveiled, marking a significant milestone in its field [11]. Traditional Z-source converter, while offering the advantage of common ground between input and output, suffers from inherently low voltage gain and discontinuous input current [12]. In contrast, the high step-up improved Z-source converter retains the desirable common ground and continuous input current characteristics. Yet, like its predecessors, it remains constrained by duty cycle limitations [13]. In response, a quasi-Z-source DC–DC converter has been developed and implemented in fuel cell vehicles. This design not only maintains a continuous input current but also reduces the voltage stress imposed on circuit components [14]. However, components like capacitors and switches are subjected to heightened voltage stresses that can compromise their durability and shorten their service life. Moreover, inherent circuit losses often lead to increased power dissipation within the converter. To address these limitations, researchers have developed quadratic Z-source converters, which not only preserve the common ground feature and ensure continuous input current but also eliminate restrictive duty cycle constraints through cascaded voltage-boosting techniques and also these converters are engineered to operate at reduced voltage stress levels on components [15]. The studies referenced in [16] and [17] introduce high-gain DC–DC converters designed with a common ground, employing Z-source and quasi-Z-source networks for low-voltage solar

photovoltaic applications. These converters not only offer a common ground but also achieve a high output-to-input voltage conversion ratio at low duty cycles. Their designs are remarkably straightforward, resulting from the merging of two conventional converter architectures, yet they retain the inherent drawbacks associated with traditional converters, namely, significant voltage and current stress on the components.

One proven method to increase voltage gain uses coupled inductors, which form the foundation of innovative designs such as Δ-source, Γ-source, A-source, X-source, T-source and Y-source converters [18]-[23], as shown in Fig. 1. Table 1 summarizes the advantages and disadvantages of the impedance sources illustrated in Fig. 1.

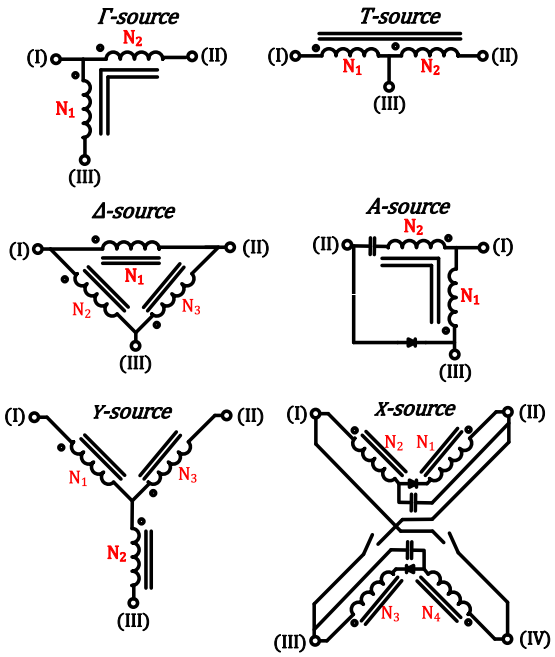


Fig. 1: Custom-shaped coupled inductors employed in IN configurations.

Alternatively, isolated high step-up DC–DC converters offer another effective route to achieving substantial voltage enhancement. However, these architectures introduce new challenges, e.g., the energy stored in the leakage inductance of their transformers can create issues, including electromagnetic interference, greater voltage strain, and notable switching losses [24]. The traditional Y-source converter demonstrates discontinuous input current, reduced voltage gain, and heightened sensitivity to duty cycle variations [20]. Similarly, A- and T-source converters exhibit limited voltage gains at lower duty cycles, with gains escalating nonlinearly, and often unpredictably, as the duty cycle increases. These findings underscore the ongoing need for innovative designs that simultaneously achieve high voltage gain, stable performance across duty cycles, and robust input current continuity [25].

Reference [26] introduces an innovative DC–DC converter characterized by its impressive voltage-boost capability. This design emerges from synthesizing the design attributes of Y–source converters with those of quasi–Z source configurations. By integrating the favorable features of these two frameworks, the converter offers numerous benefits, such as a steady, uninterrupted input current; a unified grounding that links both the input and output voltages; an onboard transformer dedicated to voltage reduction; minimized electrical strain on the switching device; and a reduced current load imposed on the output diode.

Table 1: Comparative analysis of impedance sources

Impedance Sources	Advantages	Disadvantages
Δ-Source	High voltage gain Compact and symmetric structure Suitable for medium power applications	Limited control over input/output power independently Sensitive to load variations
Γ-Source	Enables independent control of input and output power Versatile for multi functional systems	More complex control circuitry Requires thermal management at high power levels
A-Source	Fast dynamic response Ideal for systems with frequent load changes	More intricate design compared to conventional sources May require additional filtering to suppress ripple
X-Source	Highly flexible topology Adaptable to various configurations	Increased number of active components Higher implementation cost
T-Source	Achieves high voltage gain with fewer components Space-efficient design	Limited output voltage range Sensitive to inductor parameter variations
Y-Source	Stable performance during transients Well-suited for energy storage systems	Complex mathematical modeling Demands precise control to avoid oscillations

A key observation emerging from this evaluation is that merging two distinct design frameworks naturally elevates the overall count of converter components. Moreover, integrating a transformer configured with triple coils further amplifies the system's physical volume and associated energy losses.

In reference [27], an innovative DC–DC converter is introduced that dramatically elevates voltage levels by

employing a quasi-Z type network. Its configuration merges an inductor characterized by electromagnetic linkage with a four-stage rectification method, delivering considerable voltage amplification without resorting to overly aggressive duty cycles or excessive transformer winding ratios. By applying an interleaved strategy at the front end, the arrangement effectively relieves the electrical strain on both the power switching devices and the primary windings of the electromagnetically linked inductor. However, devising and managing converters that utilize this interleaving approach is considerably more intricate than traditional designs. Such complexity arises from the challenges of coordinating phase timing and harmonizing current distribution across the stages, and it is compounded by the need for extra circuitry, such as dedicated inductors and switches for each phase, that drives up overall expenses. Furthermore, although the interleaving technique effectively suppresses output ripple, it may also incur greater switching losses due to the elevated frequency of operation.

In [28], a novel impedance converter is presented. It employs one switching element and dispenses with galvanic isolation, relying instead on a topology inspired by Z-source principles. The objective is to design an arrangement that produces minimal fluctuations in the supply while delivering significant voltage amplification as determined by its duty cycle. Enhancing the winding ratio of coupled inductors embedded in a multiplier network not only raises the output voltage but also alleviates stress on semiconductor components. However, even though this architecture is intended to lower electrical strain and boost voltage levels, integrating the multiplier network with a heightened coupled inductor winding ratio invariably increases the circuit's complexity, energy losses, and overall physical volume.

Researchers in [29], present a novel design for a DC–DC converter that adopts a Y-source configuration to deliver an entirely flat input current along with a significantly broadened zero-voltage switching domain. To prevent any magnetization imbalance in its core, dedicated capacitors interrupt the direct current that would otherwise flow through a three-port coupled inductor. These same capacitors also secure the voltage levels across all semiconductor switches and rectifiers, thereby eliminating any undesirable oscillatory behavior. Nonetheless, while this architecture enhances performance in terms of voltage gain and ripple mitigation, it may also impose elevated electrical stress on specific components, which could compromise their long-term stability and durability.

Researchers in [30], introduce an innovative series of high-gain converters that leverage a Y-source impedance network, presenting groundbreaking solutions for applications requiring elevated voltage gains. Unlike traditional enhanced Y-source configurations, these designs reposition the switch from its conventional output location to the input side. This shift not only alleviates stress on the switching device but also allows the integration of various boost modules, thereby significantly enhancing the converter's boosting capability. Furthermore, while a boost cell is employed to increase the voltage gain, this approach concomitantly raises the voltage stress on components, most notably on the MOSFET. Furthermore, the design employs a switched configuration for the input inductor, which increases the current ripple at the input and weakens the effective connection to the source.

In earlier research [31], a new class of impedance source networks was introduced that employs coupled inductors along with active switches as fundamental elements. Owing to the specific turn ratios of these inductors, the networks deliver notable benefits, most prominently, they achieve an ultrahigh voltage gain and provide considerable design flexibility. This architecture not only minimizes common issues such as voltage spikes and excessive current stress that typically afflict coupled inductor schemes but also maintains a continuous input current while reducing shoot-through duty cycles. However, the reliance on two active switches and additional components may elevate production costs and complicate the overall structure of the converter, thereby limiting its scalability in certain practical applications.

In [32], a graph-based strategy is introduced to simplify the topology of a bridgeless high step-up Y-source LLC converter, resulting in a design characterized by low voltage spikes and streamlined architecture. While this method effectively minimizes voltage spikes and enhances performance, it relies on a large number of components. Consequently, the increased component count not only raises the operating costs and overall volume of the converter but may also lead to challenges in manufacturing, assembly, and long-term reliability.
Numerous studies have explored impedance source converters equipped with either passive or active clamps [33]-[36]. Passive clamps, while offering a simpler design, tend to exhibit marginally higher power losses relative to active clamp systems. Additionally, in some high step-up converters that utilize the impedance source approach, the parasitic capacitance of the clamp diode, particularly when it is non-conductive, can lead to unintended resonance within the circuit [36].

Another high step-up DC–DC converter built around a trans-inverse impedance-source design with an integral active clamp has been proposed in the literature [36]. By employing a lower turns ratio for the coupled inductor windings, the converter achieves a notable voltage boost

while keeping switch stress low. An integral active clamp recycles leakage energy from the inductors back to the output, further enhancing performance. However, these gains come at the cost of increased design complexity and tighter manufacturing tolerances, which might affect overall system stability.

In the quest for highly efficient, high-gain DC–DC converters, three recent topologies, spanning embedded Z-source, quadratic extended-duty-ratio, and zero-ripple hybrid cells, offer distinct trade-offs in gain, complexity, and input-current behavior. Zhang et al. introduce four embedded Z-source converters (EZSCs), derived from an improved pump Z-source network via two design propositions [37]. These EZSCs achieve a voltage gain boost using no more components than conventional pump Z-source counterparts, and they slash capacitor voltage stress by up to 67%. Gupta et al. meld a single-switch quadratic boost stage with an M-phase extended-duty-ratio (EDR) stage to create the quadratic EDR (Q-EDR) family [38]. Bi et al. craft a hybrid converter that integrates an active switched-inductor (A-SL) cell, a zero-ripple cell, and a switched-capacitor cell in a common-ground architecture [39]. Comparing these designs reveals clear niches: EZSCs favor simplicity and low stress at moderate gains, Q-EDR excels in ultra-high gains and ripple suppression but demands complex hardware, and the A-SL/switched-capacitor hybrid converter hits broad gain bands with minimal ripple. System architects must therefore weight gain targets, input-ripple tolerance, part counts, and control complexity when selecting among these emerging high-step-up converters.

B. Research Gaps and Contribution

Designing switching-mode power converters is a complex process, driven by multiple objectives such as stabilizing the output voltage, accurately tracking a reference voltage, achieving high efficiency, ensuring superior power quality, and maintaining reliability despite uncertainties like load changes and input voltage variations. The converter's performance and energy efficiency depend not only on factors like the chosen topology, appropriate component sizing, effective filter design, and optimal switching frequency but also significantly on the design of a robust controller.

Drawing on the findings detailed in Section 1.A, researchers have proposed diverse designs for INs-based converters; they typically fall into three distinct categories: (1) the first category focuses on refining and expanding the impedance networks; (2) The second category involves using magnetically coupled inductors or transformers; and (3) the third category integrates supplementary boost techniques and active switches into the impedance network.

An in-depth analysis of the investigated converter structures has revealed several inherent drawbacks. These include: (1) modest overall performance; (2) restricted voltage gain; (3) excessive component count; (4) complex design; (5) high voltage/current stress on passive and active components; (6) bulky physical volume; (7) elevated operating costs; and (8) pronounced input current ripples. Accordingly, the primary motivation behind this study is to develop an ultra-gain enhanced A-source (UGEA-S) DC/DC converter that effectively meets the stringent demands and performance benchmarks of contemporary electric vehicles.

Notably, the topology is distinguished by its exceptionally high voltage gain, minimal diode reverse recovery, reduced voltage stress on switching devices, a continuously stable input current profile, and a shared common ground between the power source and the load. Moreover, the converter ensures stable operation by maintaining smooth input and output current profiles even amidst abrupt disturbances in the power source, significantly bolstering its reliability and resilience under varying conditions. A comprehensive theoretical analysis has been conducted on this topology, encompassing its operating principles, steady-state performance, and efficiency evaluation. Furthermore, a detailed comparative study with other recently introduced converter designs highlights both the advantages and limitations of the proposed scheme, offering clear insights into its performance characteristics relative to existing solutions. Extensive simulations performed in the MATLAB/Simulink environment and experimental results provide robust evidence of its efficacy and effectiveness.

In summary, the article presents several groundbreaking innovations, which are detailed below:

- **UGEA-S Architecture:** A new DC/DC converter design tailored for advanced electric vehicles, emphasizing an ultra-high voltage gain.
- **Stable Input Current Profile:** Ensures a continuously stable input current, contributing to a smoother operation and better compatibility with the power source.
- **Common Ground Configuration:** Implements a shared grounding scheme between the power source and the load, simplifying system integration and reducing complexity.
- **Exceptional Voltage Boost Capability:** Achieves an unusually high voltage gain, crucial for meeting the demanding power requirements of modern electric vehicles.
- **Reduced Diode Reverse Recovery Losses:** Minimizes the reverse recovery issues of diodes, which enhances overall efficiency and performance.

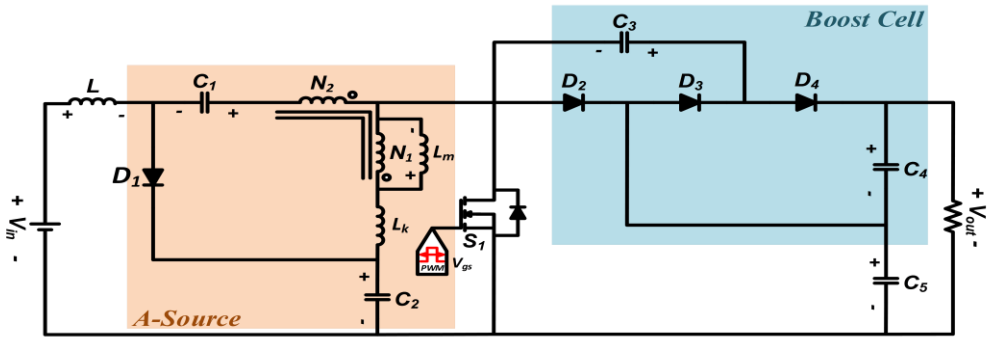


Fig. 2: Schematic of the proposed UGEA-S DC/DC converter.

- **Minimized Voltage Stress on Switching Device:** Optimizes the converter to lower voltage strain on the switch, thereby potentially improving the lifespan and reliability of the system.
- **Resilience Amid Disturbances:** Maintains smooth input/output current profiles even under abrupt power source disturbances, boosting operational reliability under variable conditions.

The rest of this paper is organized as follows: Section II introduces the proposed UGEA-S DC/DC converter. Section III describes its operational states, steady-state behavior, and design considerations, including voltage stress on components. Section IV analyzes power dissipation and efficiency metrics. Section V conducts a comparative study. Section VI validates the design through simulation and experimental results, and finally, Section VII provides concluding remarks.

Proposed UGEA-S DC/DC Converter

This section offers an in-depth explanation of the design and individual elements that constitute the proposed UGEA-S DC/DC converter.

Fig. 2 depicts the configuration of the proposed converter, which incorporates a coupled inductor modeled by its magnetizing inductance (L_m) and an ideal transformer characterized by the turn's ratio $N = N_2/N_1$.

The circuit incorporates a single metal-oxide-semiconductor field-effect transistor (MOSFET) identified S_1, along with five capacitors (C_1, C_2, C_3, C_4, and C_5) and four diodes (D_1, D_2, D_3, and D_4). In this arrangement, capacitors C_4 and C_5 are dedicated to delivering power to the loads during different duty cycles. Moreover, components D_2, D_3, D_4, C_3, C_4, and C_5 work together as a boost cell, regulating the charging and discharging of the capacitors to maintain the load supply when the MOSFET switches ON and OFF. The input voltage is denoted by V_{in}, and the converter consistently operates in continuous conduction mode (CCM). Furthermore, Fig. 3 illustrates the converter's operational modes, while Fig. 4 provides examples of the voltage and current waveforms in CCM for the UGEA-S

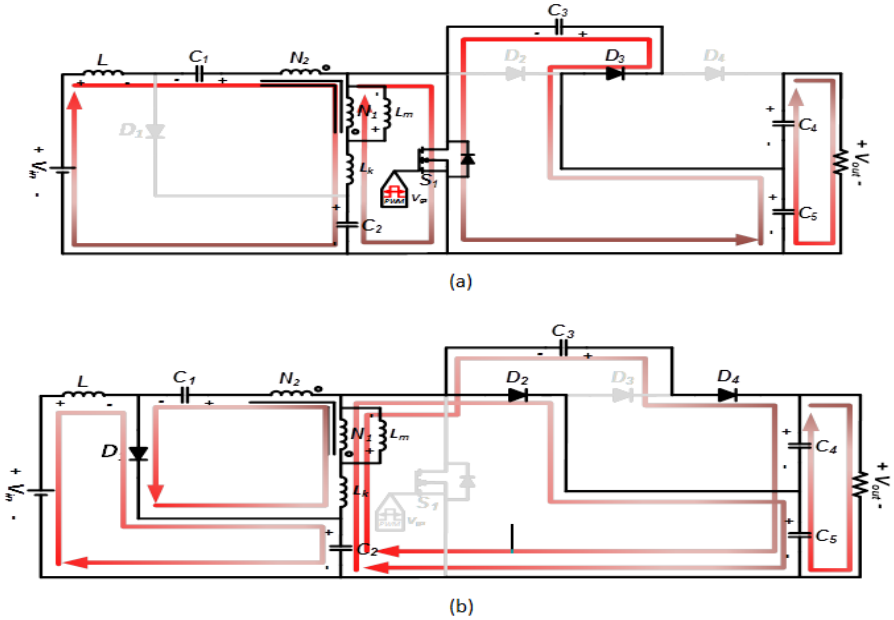


Fig. 3: Illustration of operating states during a complete switching cycle: (a) State I; (b) State II.

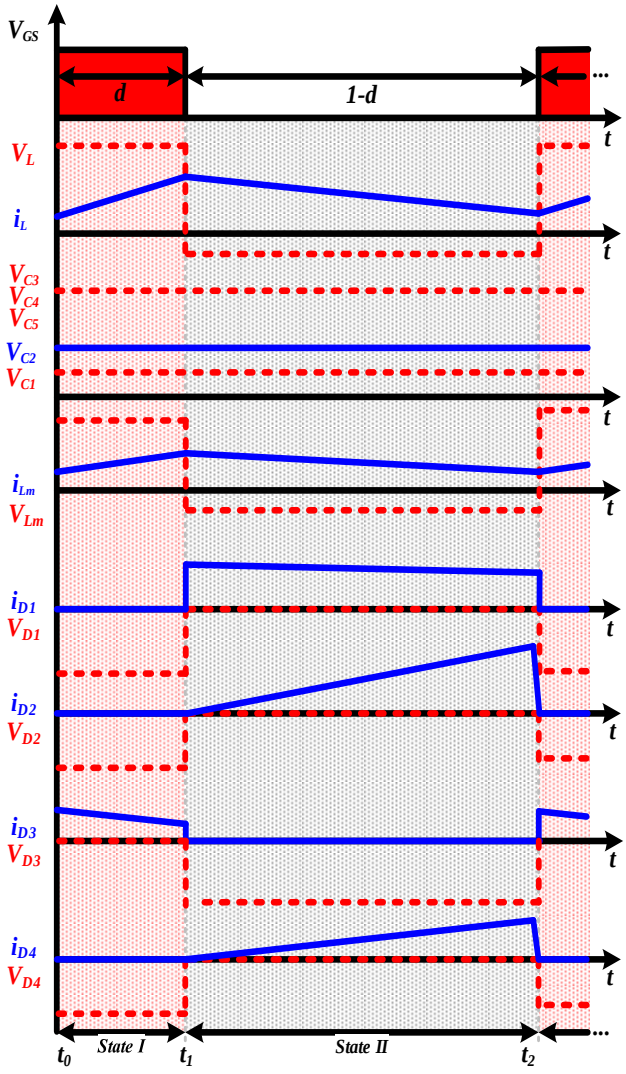


Fig. 4: Diagram illustrating the anticipated theoretical waveforms for the proposed UGEA-S DC/DC converter.

Operational States of the Proposed UGEA-S DC/DC Converter

A comprehensive evaluation of the proposed UGEA-S DC/DC converter is conducted under several foundational assumptions. First, the magnetizing inductor (L_m) is assumed to be sufficiently large to ensure that the magnetizing current (i_{Lm}) flows continuously, while any parasitic resistance and leakage inductance inherent in the coupled inductor are disregarded. Second, all components, including switches and diodes, are considered ideal; therefore, voltage drops across the diodes, parasitic resistances, the ON-state resistance ($R_{ds(ON)}$), and parasitic capacitances of the switches are omitted from the analysis. Third, the capacitors are assumed to be large enough such that their voltage remains effectively constant, with their parasitic resistances also ignored. Finally, the converter is designed to operate in two distinct modes within a single switching period, as illustrated in Figs. 2 and 3.

A. State I [t_0,t_1] (Switch On)

Initially, the power switch (S_1) is triggered to conduct and immediately turns on. As a result, diodes D_1, D_2, and D_4 become reverse-biased due to the activation of the switch and remain non-conductive. By applying Kirchhoff's voltage law to the formed loops, one can derive the governing equations for this operational stage. It is also important to highlight that the analysis for both operating modes incorporates a magnetizing inductor, which is connected in parallel with primary side N_1. In essence, the converter is modeled using a two-ended transformer, where the coupling inductor is represented by L_m.

By applying Kirchhoff's voltage law to the circuit depicted in Fig. 3(a), the following equations are derived:

$$V_{Lm}^{State\ I} = V_{C2} \tag{1}$$

$$V_{C5} = V_{C3} \tag{2}$$

$$V_{out}^{State\ I} = V_{C4} + V_{C5} \tag{3}$$

$$V_{in} - V_L + V_{C1} - V_{C2} + V_{Lm}\left(1 + \frac{N_2}{N_1}\right) = 0 \tag{4}$$

Using (1) as a basis, we can simplify (4) to yield the expression given in (5).

$$V_L^{State\ I} = V_{in} + V_{C1} + \frac{N_2}{N_1}V_{C2} \tag{5}$$

B. State II [t_1,t_2] (Switch OFF)

At this moment, when the power switch S_1 is commanded to cut off (or open the circuit), it is deactivated. Consequently, the diode D_3 becomes reverse biased and deactivates as a result of the switch's cut off. By analyzing the circuit loops via Kirchhoff's voltage law (Fig. 3(b)), we derive the relationships that govern this mode. Additionally, as noted in the previous section, our analysis for both modes include an inductor, referred to as L_M, in parallel to N_1.

$$V_L^{State\ II} = V_{in} - V_{C2} \tag{6}$$

$$V_{Lm}^{State\ II} = V_{C2} - V_{C5} \tag{7}$$

$$V_{C3} = V_{C4} \tag{8}$$

$$V_{Lm}^{State\ II}\left(1 + \frac{N_2}{N_1}\right) + V_{C1} = 0 \tag{9}$$

$$V_{out}^{State\ II} = V_{C4} + V_{C5} \tag{10}$$

Expressing (9) in terms of V_{Lm} yields:

$$V_{Lm}^{State\ II} = -\frac{V_{C1}}{\left(1 + \frac{N_2}{N_1}\right)} \tag{11}$$

C. Detailed Exploration of Voltage Gain

Let d_1 denote the duty cycle of the switch S_1. In the proposed converter, the input voltage, V_{in}, serves as the

energy source that supplies power to the load. According to the fundamental volt–second balance principle, an inductor must have a net zero voltage when averaged over a complete switching period. This condition applies to both the input inductor (L) and the magnetizing inductor (L_m). During States I and II of the converter's operations, the instantaneous voltages across L and L_M are indicated by $V_L^{State\ I}d + V_L^{State\ II}(1-d)$; and $V_{L_m}^{State\ I}d + V_{L_m}^{State\ II}(1-d)$, respectively. Given that the volt-second balance requires that the total voltage applied to each inductor over one full switching cycle must sum to zero, we have the following condition:

$$\langle V_L \rangle = \frac{V_L^{State\ I} dT_s + V_L^{State\ II}(1-d)T_s}{T_s} = 0 \quad (12)$$

$$\langle V_{L_m} \rangle = \frac{V_{L_m}^{State\ I} dT_s + V_{L_m}^{State\ II}(1-d)T_s}{T_s} = 0 \quad (13)$$

By incorporating the results from (1), (2), (6), and (11) into the framework provided by (13) and (14), we derive the following relationships. For simplicity in our analysis, we define the ratios $\zeta = (N_2 + N_1)/N_1$ and $N = N_2/N_1$; so:

$$d(V_{in} + V_{C1} + NV_{C2}) + (1-d)(V_{in} - V_{C2}) = 0 \quad (14)$$

$$dV_{C2} + (1-d)\left(\frac{-V_{C1}}{\zeta}\right) = 0 \quad (15)$$

After rearranging and canceling redundant terms within (14), the expression simplifies neatly to what is presented as (16):

$$V_{C1} = \zeta\left(\frac{d}{1-d}\right)V_{C2} \quad (16)$$

Through additional algebraic refinements, (15) is condensed to yield the more streamlined form expressed as (17):

$$V_{C1} = \frac{-V_{in}}{d} - NV_{C2} + \frac{V_{C2}}{d} - V_{C2} \quad (17)$$

By setting the expressions from (16) and (17) equal to each other and then carrying out the required simplifications, we derive the following expression for V_{C2}:

$$V_{C2} = \frac{1}{1 - \left(\left(\frac{d^2}{1-d}\right)\zeta + (N+1)d\right)}V_{in} \quad (18)$$

Drawing from the formulations presented in (16) and (18), the voltage across capacitor C_1 can be derived similarly. In this process, we obtain an expression for V_{C1} that is ultimately represented by (19).

$$V_{C1} = \frac{\zeta\left(\frac{d}{1-d}\right)}{1 - \left(\left(\frac{d^2}{1-d}\right)\zeta + (N+1)d\right)}V_{in} \quad (19)$$

To calculate the voltage gain, one must first determine the relationship between the output voltage and the input voltage.

To calculate the voltage gain, one must first determine the relationship between the output voltage and the input voltage. For clarity, the expression that defines the output voltage has been restated in (20). Additionally, note that, as indicated by (2) and (8), the voltages across capacitors C_4 and C_5 are identical, so, $V_{C4} = V_{C5}$.

$$V_{out} = V_{C4} + V_{C5} = 2V_{C4} = V_{C5} \quad (20)$$

In order to obtain the output voltage, computing V_{C5} is essential. According to (7) and (11), in the OFF state of the switch S_1, while V_{Lm} is defined as $V_{Lm} = -V_{C1}/\zeta$, the expression for V_{C5} becomes:

$$V_{C5} = V_{C2} - V_{Lm} = V_{C2} + \frac{V_{C1}}{N} \quad (21)$$

Substituting the formulas for V_{C1} and V_{C2} provided in (18) and (19) into (21) leads us to the expression for V_{C5}:

$$V_{C5} = \left(\frac{1}{1-d}\right)\left(\frac{1}{1 - \left(\left(\frac{d^2}{1-d}\right)\zeta + (N+1)d\right)}\right)V_{in} = V_{C4} = V_{C3} \quad (22)$$

Based on the output voltage expression in (20) and the V_{C5}expression in (22), by simplifying the equations and expanding the symbols ζ and N, the resulting voltage gain is given by (23), which is illustrated in Fig. 5.

$$Gain = \frac{V_{out}}{V_{in}} = \frac{2}{1 - (2 + \frac{N_2}{N1})d} = \frac{2}{1-(2+N)d} \quad (23)$$

D. Analysis of Voltage Stresses on Components

This section provides an analysis of the voltage stresses experienced by the components. It aims to evaluate the magnitude and distribution of voltage across each component, offering valuable insights into their operational behavior under specific conditions.

I) Voltage Stresses on Capacitors

The voltage stresses across the capacitors V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_{C5} are determined using (18), (19), and (22), respectively. A detailed summary of these voltage stresses is presented in Table 2.

Table 2: Voltage stresses on capacitors

Capacitors	Values
C_1	$V_{C1}^{Stress} = \frac{\zeta\left(\frac{d}{1-d}\right)}{1 - \left(\left(\frac{d^2}{1-d}\right)\zeta + (N+1)d\right)}V_{in}$
C_2	$V_{C2}^{Stress} = \frac{1}{1 - \left(\left(\frac{d^2}{1-d}\right)\zeta + (N+1)d\right)}V_{in}$
C_3,C_4, C_5	$V_{C3,C4,C5}^{Stress} = \left(\frac{1}{1-d}\right)\left(\frac{1}{1 - \left(\left(\frac{d^2}{1-d}\right)\zeta + (N+1)d\right)}\right)V_{in}$

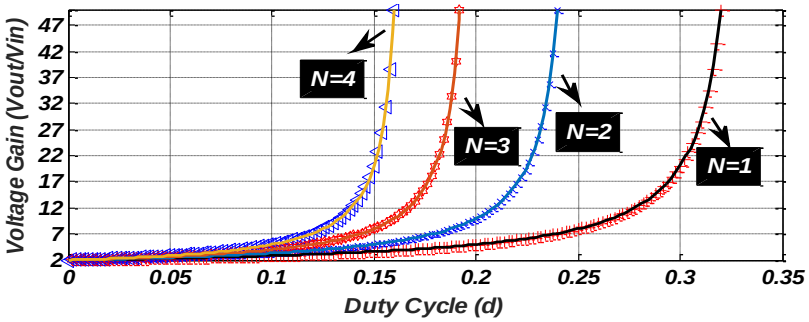


Fig. 5: Voltage gain for the proposed UGEA-S DC/DC converter.

II) Voltage Stress on Power Switch

The voltage stress across the switch S_1 can be mathematically derived by analyzing the circuit topology and applying the relevant electrical equations. This process involves identifying the maximum voltage that S_1 is exposed to during its operation, considering factors such as the input voltage, switching states, and the behavior of other components within the system. This derived expression helps in understanding the stress experienced by S_1, which is critical for selecting a suitable switch that ensures reliable performance. The derivation of the voltage stress for switch S1 can be established as follows:

$$V_{S1}^{Stress} = V_{C5}^{Stress} = \left(\frac{1}{1-d}\right)\left(\frac{1}{1-\left(\left(\frac{d^2}{1-d}\right)\zeta + (N+1)d\right)}\right)V_{in} \quad (24)$$

It is evident that the voltage stress on the switch S_1 is limited to 72% of the output voltage when the duty cycle reaches its maximum value ($d = 0.15$) and the turns ratio (N) is set to three. Moreover, as the turns ratio of the coupled inductor increases, the voltage stress decreases further, leading to a substantial reduction in switching losses. This optimization allows for the use of a MOSFET with a lower ON-resistance, thereby enhancing overall efficiency.

III) Voltage Stress on Diodes

The maximum voltage stresses experienced by diodes D_1, D_2, D_3 and D_4 during their OFF-state are governed by the respective capacitor voltages. As such, these stresses can be calculated using the relationships established between the diode voltage levels and the capacitor voltages.

$$V_{D1}^{Stress} = V_{in} - V_{C2} - V_L^{State\ I} = \left(\frac{N + \zeta\left(\frac{d}{1-d}\right) - 1}{1-\left(\left(\frac{d^2}{1-d}\right)\zeta + (N+1)d\right)}\right)V_{in} \quad (25)$$

$$V_{D2}^{Stress} = V_{C5}^{Stress} = \left(\frac{1}{1-d}\right)\left(\frac{1}{1-\left(\left(\frac{d^2}{1-d}\right)\zeta + (N+1)d\right)}\right)V_{in} \quad (26)$$

$$V_{D3,D4}^{Stress} = V_{C4}^{Stress} = \left(\frac{1}{1-d}\right)\left(\frac{1}{1-\left(\left(\frac{d^2}{1-d}\right)\zeta + (N+1)d\right)}\right)V_{in} \quad (27)$$

Evaluation of Power Dissipation and Efficiency Metrics

The energy losses in the proposed converter primarily stem from the dissipation mechanisms within its individual components. These include the switching element, diodes, magnetic elements, and capacitors, each of which contributes to the overall power loss in the system. The switch experiences energy dissipation during its operation due to factors such as conduction and switching losses. Similarly, the diodes incur power losses through forward voltage drops and reverse recovery processes. Magnetizing elements, such as inductors and transformers, add to the losses due to core saturation, eddy currents, and winding resistances. Capacitors, on the other hand, contribute through dielectric losses and equivalent series resistance (ESR). Together, these factors cumulatively define the total power loss profile of the converter.

A. Diodes

To determine the power losses associated with diodes, key parameters such as the forward voltage drop and ESR are taken into account. These factors allow for an accurate estimation of diode losses, which can be computed using the formula presented in (28). The forward voltage drop contributes to conduction losses during the diode's active state, while the ESR leads to resistive dissipation. Together, these parameters provide a comprehensive framework for evaluating the energy losses incurred by the diodes in the system.

$$P_{D_j}^{Loss} = \sum_{j=1}^{4} r_{D_j} \times I_{D_j,RMS}^2 + I_{D_j}^{Avg} \times V_{F,D_j}$$
$$= I_{D_1,RMS}^2 \times r_{D_1} + I_{D_2,RMS}^2 \times r_{D_2} + I_{D_3,RMS}^2 \times r_{D_3}$$
$$+ I_{D_4,RMS}^2 \times r_{D_4} + I_{D_1}^{Avg} \times V_{F,D_1} + I_{D_2}^{Avg} \times V_{F,D_2}$$
$$+ I_{D_3}^{Avg} \times V_{F,D_3} + I_{D_4}^{Avg} \times V_{F,D_4}$$
$$\approx 19.25W\ (at\ 500W\ input\ power) \quad (28)$$

In the mentioned equation, V_{F,D_j} denotes the forward voltage drops across the diodes. These values are determined based on the specifications provided in the corresponding datasheets. Additionally, r_{D_j} represents the ESRs of the diodes.

B. Power Switch

As previously discussed, the MOSFET is chosen as the power switching element in the proposed converter. For an individual MOSFET, its major power losses arise from three sources: switching losses (denoted as P_S)), conduction losses (P_C), and losses associated with parasitic capacitances (P_{CS}). Conduction losses occur when the MOSFET is in its linear region; here, the energy is dissipated through its on-state resistance, $R_{ds}(ON)$. On the other hand, switching losses are produced by Joule heating caused by the channel current during the switching transient period. Finally, a portion of the power loss is due to the energy required to charge the parasitic capacitors [27]. Accordingly, the total power loss is expressed as $P_{Switch}^{Loss} = P_C + P_S + P_{CS}$; In this formulation, the switching loss is computed based on the transient dynamics of the channel current.

For a linear transition, the average voltage and current during the switching interval equate to half of their peak values. Since the switching events occur repeatedly at a frequency f_s (the number of switching cycles per second), the total switching power loss is the energy per cycle multiplied by this frequency; thus, the energy lost per transition event is given by:

$$P_S = V_{S_1}^{Peak} I_{S_1}^{Avg} \frac{(t_{d,off} + t_{d,on})}{2} f_s \quad (29)$$

here, $t_{d,on}$ denotes the rise time, while $t_{d,off}$ signifies the fall time. Both of these timing parameters are determined by the static electrical characteristics detailed in the manufacturer's datasheet.

When a MOSFET is active, that is, in its conducting state, it dissipates power due to its inherent on-state resistance. This dissipation, known as conduction loss, is primarily caused by the energy converted to heat as current flows through the device; so, the conduction loss associated with power switch S_1 is given by:

$$P_C = R_{ds}(ON) I_{S_1,RMS}^2 \quad (30)$$

During each switching cycle, the parasitic capacitances, present due to the inherent construction of the device and its surrounding circuitry, must be charged and discharged. The energy consumed to charge a capacitor is stored temporarily and then dissipated as heat when the capacitor discharges. Since the device switches at a frequency f_s (i.e., it goes through this charge–discharge cycle f_s times per second), the overall power loss due to the charging of these parasitic capacitors can be calculated as:

$$P_{CS} = \frac{f_s}{2}\left[C_{gs} V_{gs}^2 + (C_{ds} + C_{gd})(V_{ds})^2\right] \quad (31)$$

In this context, C_{gs}, C_{ds}, and C_{gd} refer to the parasitic capacitances associated with charging. Additionally, V_{gs} and V_{ds} represent the voltages between the gate-source and drain-source terminals, respectively.

Finally, the overall power loss of switch S_1 is determined by the sum of its conduction, switching, and parasitic capacitor charging losses, and can be calculated as:

$$P_{Switch}^{Loss}$$
$$= V_{S_1}^{Peak} I_{S_1}^{Avg} \frac{(t_{d,off} + t_{d,on})}{2} f_s + R_{ds}(ON) I_{S_1,RMS}^2$$
$$+ \frac{f_s}{2}\left[C_{gs} V_{gs}^2 + (C_{ds} + C_{gd})(V_{ds})^2\right]$$
$$\approx 12.53W (at\ 500W\ input\ power) \quad (32)$$

C. Magnetic Components

The losses for both the input and coupled inductors are determined using (33). It is important to note that, by neglecting the current ripple in these magnetic devices, their average current values are assumed to be equivalent to their RMS values [27].

$$P_{Inductors}^{Loss} = P_{core}^{L} + r_L I_{L,RMS}^2 + r_{CL} I_{CL,RMS}^2$$
$$\approx 4.95W\ (at\ 500W\ input\ power) \quad (33)$$

where $P_{core}^{L} = A_e l_e (\alpha B_p^b f_s^c)$; r_{L_1} denotes the ESR of the input inductor, while r_{CL} represents that of the coupled inductor. The constants α, b, and c are obtained through curve fitting based on the manufacturer's datasheet data. Additionally, B_p specifies the AC magnetic flux density within the magnetic core, and A_e along with l_e correspond to the core's effective transverse area and its magnetic path length, respectively [28].

D. Capacitors

Capacitor power losses are generally minimal, as they primarily arise due to the inherent parasitic resistance within the capacitor. These losses can be calculated using the following relationship:

$$P_{Capacitors}^{Loss} = \sum_{k=1}^{5} r_{C_k} I_{C_k,RMS}^2$$
$$\approx 1.4W\ (at\ 500W\ input\ power) \quad (34)$$

E. Efficiency

Finally, the efficiency of the proposed converter at input power of $500W$ is determined using (35). The theoretical analysis further provides a detailed breakdown of the percentage losses, which is illustrated in Fig. 6. In particular, the converter achieves an efficiency of 94% at an output power of $50W$, 95.2% at $100W$, 96.93% at $230W$, 92.91% at $500W$ and decreases to 92% when the output power is increased to $100W$.

$$\eta\ (at\ 500W) = \frac{P_o}{P_{in}} = \frac{P_o}{P_o + P_{Switch}^{Loss} + P_{Inductors}^{Loss} + P_{Capacitors}^{Loss} + P_{Diodes}^{Loss}} = \frac{500W}{500W + 12.53W + 4.95W + 1.4W + 19.25W} = \%92.91 \quad (35)$$

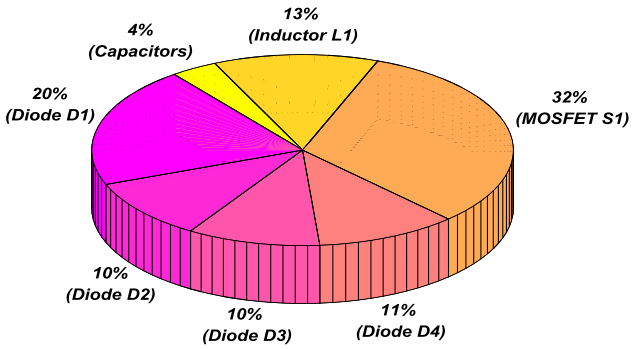


Fig. 6: Loss breakdown analysis in the proposed UGEA-S DC/DC converter.

Comparative Evaluation

In this section, the proposed UGEA-S DC/DC converter is evaluated against several comparable converters documented in previous studies [16], [17], [19], [24], [27], [28].

For this comparison, we chose converter designs that incorporate impedance networks and deliver high voltage gains. The analysis considers factors such as voltage gain, the peak voltage stress on both the output diode and the MOSFET, the number of components used, maximum efficiency, and other key parameters. Moreover, the associated equations and the derived results are summarized in Table 3.

Fig. 7(a) compares the voltage gain curves of various converter designs. The data indicate that the proposed converter delivers a higher voltage gain while maintaining the same turns ratio and duty cycle as its counterparts.

Moreover, thanks to the combined effect of the coupled inductor's turns ratio and the converter's unique topology, it is unnecessary to excessively increase the switch's duty cycle. This design advantage results in a considerable reduction in the switch's conduction loss, and by optimizing both the duty cycle and the coupled inductor's turns ratio, a higher output voltage can be achieved. Furthermore, as presented in Table 3, the converters described in [16], [17], and [24] exhibit relatively low output voltage gains, making them less suitable for fuel cell-based battery charger applications.

Table 3: Analysis of the proposed UGEA-S DC/DC converter in relation to other converter designs

Refs./Year	Voltage Gain ($M = V_O / V_{in}$)	Max. voltage across switch(es)	Max. voltage across output diode(s)	Max Eff%	Number of Components (Switches/Diodes/Capacitors/Inductors)	Cost per Watt	Size	Controller Requirements
[16]/2024	$\frac{\pi}{1-d}$	$\left(\frac{\pi/2}{1-d}\right)V_{in}$	$\left(\frac{\pi/2}{1-d}\right)V_{in}$	96.7	2/3/5/3	M	M	Voltage-mode
[17]/2024	$\frac{1-d}{d(1-2d)}$	$\left(\frac{1-d}{d(1-2d)}\right)V_{in}$	$\left(\frac{1-d}{d(1-2d)}\right)V_{in}$	93	2/2/2/3	L	S	Voltage-mode
[19]/2016	$\frac{1}{1-(2+N)d}$	$\frac{1}{1-(2+N)d}V_{in}$	$\frac{1}{1-(2+N)d}V_{in}$	96	1/2/3/2	L	C	Voltage-mode
[24]/2023	$\frac{1+d}{1-2d}$	$\left(\frac{2-d}{1-2d}\right)V_{in}$	$\left(\frac{1}{1-2d}\right)V_{in}$	94	2/3/2/3	M	M	Voltage-mode
[27]/2023	$\frac{2N}{1-2d}$	$\left(\frac{1}{1-2d}\right)V_{in}$	$\left(\frac{N}{1-2d}\right)V_{in}$	94	2/5/7/2	H	La	Interleaved multichannel control
[28]/2025	$\frac{2+N(1-d)}{1-2d}$	$\left(\frac{1}{1-2d}\right)V_{in}$	$\left(\frac{N+1}{1-2d}\right)V_{in}$	95	1/4/5/3	M	M	Voltage-mode
[37]/2023	$\frac{2-d}{1-2d}$	$\left(\frac{1}{1-2d}\right)V_{in}$	$\left(\frac{1}{1-2d}\right)V_{in}$	92.5	1/3/4/2	L	C	Voltage-mode
[38]/2023	$\frac{4}{(1-d)^2}$	$\left(\frac{1}{(1-d)^2}\right)V_{in}$	$\left(\frac{2}{(1-d)^2}\right)V_{in}$	94.8	4/10/5/6	H	La	Advanced PID/PLL compensation
[39]/2023	$\frac{3}{1-d}$	$\left(\frac{1}{1-d}\right)V_{in}$	$\left(\frac{2}{1-d}\right)V_{in}$	94	2/5/4/3	M	M	Voltage-mode
Proposed Converter	$\frac{2}{1-(2+N)d}$	$\left(\frac{1}{1-d}\right)\left(\frac{1}{\delta}\right)V_{in} = \frac{1}{1-(2+N)d}V_{in}$	$\left(\frac{1}{1-d}\right)\left(\frac{1}{\delta}\right)V_{in} = \frac{1}{1-(2+N)d}V_{in}$	96.93	1/4/5/2	L	C	Voltage-mode

* $\delta = 1 - \left(\left(\frac{d^2}{1-d}\right)\zeta + (N+1)d\right)$;
* The converters' efficiencies were determined by extracting data from the efficiency curves reported in their respective studies;
* N denotes the turns ratio of the coupled inductor;
* d represents the duty cycle of the power switch;
* M= Medium; L=Low; H=High; S=Small; C= Compact; La=Large.

When evaluating converter performance, it's essential to take into account how voltage stress distribution not only affects efficiency and reliability but also influences the overall cost and size of the system. This approach highlights the benefits of careful design and normalization techniques, which can provide insights into optimizing both semiconductor and passive component selection. Figs. 7(b) and (c) reveal that, after normalization, both the switch and output diode in the proposed converter experience substantially lower voltage stress compared to other designs. This reduction in stress leads to decreased switching losses, and it permits the use of MOSFET with a low voltage rating and minimal ON-resistance ($R_{ds}(ON)$), thereby reducing conduction losses. When comparing voltage stress levels, the converter topologies outlined in [17], [27], and [28] impose the highest stress on the output diode, as illustrated in Fig. 7(c). Additionally, the converter discussed in [17] exhibits elevated voltage stress on the power switch. Overall, the proposed converter demonstrates a clear advantage in managing semiconductor voltage stresses compared to its counterparts. Lower voltage stress on capacitors further allows for the use of smaller, more cost-effective components.

An examination of Table 3 clearly indicates that the converter's design employs an optimal number of components, which in turn minimizes its size, complexity, and weight. This streamlined approach not only simplifies the circuitry but also leads to a substantial reduction in total losses, thereby elevating both the efficiency and overall performance of the converter. Moreover, as detailed in Section 4, the converter achieves a maximum efficiency of 96.93%, a performance level that surpasses that of comparable converters operating within the same power range. This outstanding efficiency further validates the design's superior operational characteristics.

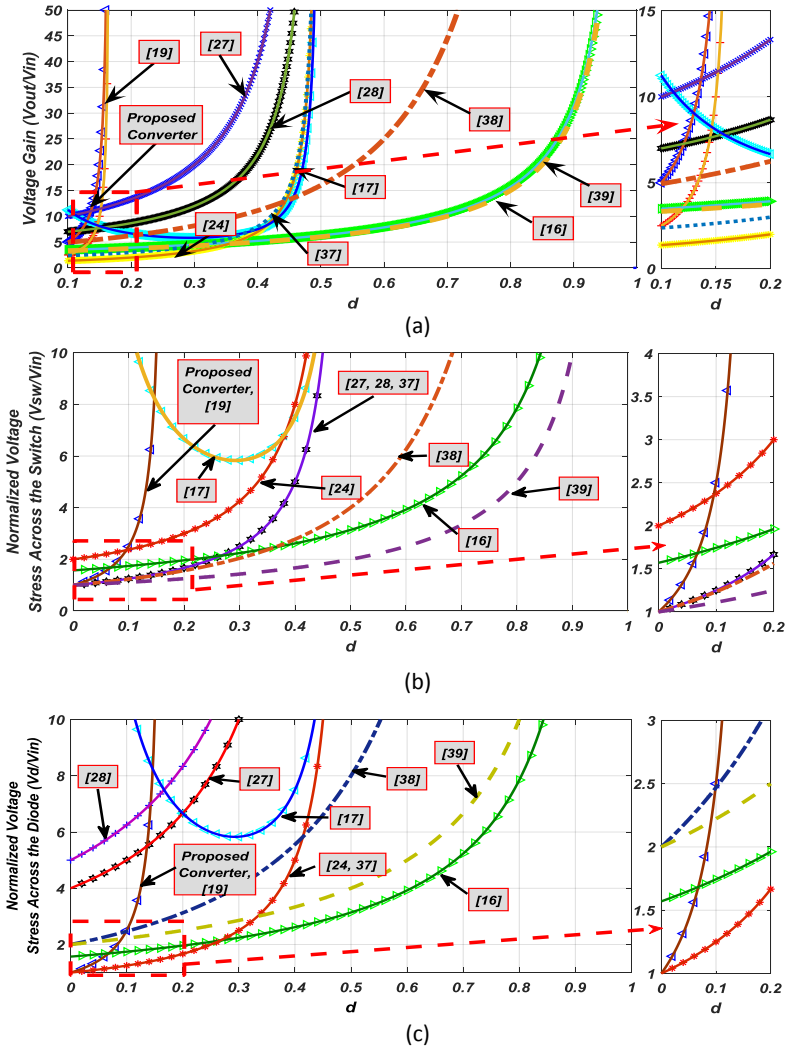


Fig. 7: (a) Comparison of voltage gain among converters; (b) Normalized maximum voltage stress across the power switches; (c) Normalized maximum voltage stress across the output diodes.

Cost per watt reflects the upfront and assembly expenses of passives (inductors, diodes, capacitors), active switches, and the surrounding PCB and thermal management hardware, divided by rated output power. Low-component topologies such as [17] (2/2/2/3) and [19] (1/4/3/2) achieve low cost per watt through minimal silicon count and compact magnetics. Yet they can only realize moderate gain (sub-8×) or efficiency under 96%. High-component solutions, notably [27] (2/5/7/2) and [38] (4/10/5/6), drive cost per watt upward despite advanced features like interleaving or PLL-based compensation. Medium-cost designs ([16], [24], [28], [39]) offer balanced component counts but often sacrifice step-up ratio or incur higher stress on semiconductors. Our Proposed UGEA-S uses a moderate complement of parts yet delivers an 8× voltage gain at 96.93% efficiency. By leveraging switched-capacitor enhancements, it avoids oversized magnetics or exotic control ICs. The result is one of the lowest cost-per-watt solutions among high-gain topologies. Physical volume determines enclosure dimensions, heatsink requirements, and total system weight, critical in electric vehicles and portable power supplies. Topologies with single inductor and few active devices ([19], [37]) win on size but compromise voltage gain and/or efficiency. Complex interleaved and multi-stage converters ([27], [38]) occupy large PCBs and require multiple gate drivers and extensive heatsinking. With its compact footprint, the UGEA-S avoids multi-phase interleaving and bulky transformer windings, relying instead on a single coupled inductor and an elegantly arranged switched-capacitor network. This allows a smaller PCB area and reduced mechanical volume, matching or surpassing the size efficiency of simpler low-gain converters. Control complexity drives software development, gate-driver hardware, and sensing precision. Simple voltage-mode PI regulators are desirable for fast prototyping and reliability. Voltage-mode (PI Controller) is used by most references ([16], [17], [19], [24], [28], [37], [39]) and suffices where the plant transfer function is well behaved and stress margins are generous. Interleaved multichannel control ([27]) and advanced PID/PLL compensation ([38]) demand DSP or FPGA implementations, increasing system cost and design time. Our converter's two-state switching behavior yields a plant with high DC gain and favorable phase margin. As demonstrated in the small-signal model, a straightforward voltage-mode PI loop meets transient and steady-state targets without resorting to complex algorithms or expensive processors.

No single published converter simultaneously achieves an 8× gain, >96 % efficiency, low component count, compact size, and simple PI control, except the proposed UGEA-S. Its balanced design exploits switched-capacitor networks to boost voltage without multiplying magnetics or control channels. The upshot is a low cost per watt, minimal PCB area, and ease of implementation, positioning UGEA-S as the ideal candidate for high-density DC/DC conversion in electric vehicles, renewable energy systems, fuel cells, battery charging systems and other high-step-up applications.

State-Space Modeling and Small-Signal Analysis of the Proposed UGEA-S DC-DC Converter

The UGEA-S DC/DC converter operates in two modes based on the switch S_1 state: ON (State I) and OFF (State II). The state variables are defined as the current through the inductors and the voltages across the capacitors: i_L (current through input inductor L), i_{Lm} (magnetizing current), v_{C1}, v_{C2}, v_{C3}, v_{C4}, v_{C5}. So, the state vector is $\mathrm{x} = [i_{L1}, i_{Lm}, v_{C1}, v_{C2}, v_{C3}, v_{C4}, v_{C5}]^T$. The output is $v_{out} = v_{C4} + v_{C5}$, and the input vector is $u = [V_{in} \quad d]^{\top}$.

A. State I (Switch S_1 ON, duration dT_s):

From the circuit analysis and Fig. 3(a), the state equations are:

$$\frac{di_L}{dt} = \frac{v_{in} + v_{C1} + Nv_{C2}}{L} \tag{36}$$

$$\frac{di_{Lm}}{dt} = \frac{v_{C2}}{L_m} \tag{37}$$

$$\frac{dv_{C1}}{dt} = \frac{i_L}{C_1} \tag{38}$$

$$\frac{dv_{C2}}{dt} = \frac{-i_{Lm} - (1/N)i_L}{C_1} \tag{39}$$

$$\frac{dv_{C3}}{dt} = \frac{\left(\frac{v_{out}}{R_{out}}\right) + \left(\frac{1}{N} - 1\right) i_L + i_{Lm}}{2C_3} \tag{40}$$

$$\frac{dv_{C4}}{dt} = \frac{v_{out}}{C_4 R_{out}} \tag{41}$$

$$\frac{dv_{C5}}{dt} = \frac{\left(\frac{v_{out}}{R_{out}}\right) - \left(1 + \frac{1}{N}\right) i_L - i_{Lm}}{2C_5} \tag{42}$$

where $v_{out} = v_{C4} + v_{C5}$ and $R_{out} = \frac{v_{out}^2}{P_{out}}$.

The state-space matrices for State I are:

$$\mathrm{A}_1 = \begin{bmatrix} 0 & 0 & \frac{1}{L} & \frac{N}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_m} & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{NC_2} & -\frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{2C_3}\left(\frac{1}{N} - 1\right) & \frac{1}{2C_3} & 0 & 0 & 0 & \frac{1}{2C_3 R} & \frac{1}{2C_3 R} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_4 R} & \frac{1}{C_4 R} \\ -\frac{1}{2C_5}\left(1 + \frac{1}{N}\right) & -\frac{1}{2C_5} & 0 & 0 & 0 & \frac{1}{2C_5 R} & \frac{1}{2C_5 R} \end{bmatrix}, \tag{43}$$

$$\mathrm{B}_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \mathrm{C}_1 = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1]$$

B. State II (Switch S1 OFF, duration $(1-d)T_s$):

From the circuit analysis and Fig. 3(b), the state equations are:

$$\frac{di_L}{dt} = \frac{v_{in} - v_{C2}}{L} \tag{44}$$

$$\frac{di_{Lm}}{dt} = \frac{v_{C2} - v_{C5}}{L_m} \tag{45}$$

$$\frac{dv_{C1}}{dt} = \frac{i_L + i_{Lm} + \frac{C_2 v_{out}}{2C_3 R_{out}}}{C_1\left(\frac{N-1}{N}\right) - C_2\left(\frac{N}{N+1}\right)} \tag{46}$$

$$\frac{dv_{C2}}{dt} = \frac{v_{out}}{2C_3 R_{out}} + \frac{\left(i_L + i_{Lm} + \frac{C_2 v_{out}}{2C_3 R_{out}}\right)\left(\frac{N}{N+1}\right)}{K} \tag{47}$$

$$\frac{dv_{C3}}{dt} = \frac{v_{out}}{2C_3 R_{out}} \tag{48}$$

$$\frac{dv_{C4}}{dt} = \frac{v_{out}}{2C_4 R_{out}} \tag{49}$$

$$\frac{dv_{C5}}{dt} = \frac{v_{out}}{C_5 R_{out}} - \frac{i_L}{C_5} - \left(\frac{C_2}{C_5}\right)\left[\frac{v_{out}}{2C_3 R_{out}} + \frac{\left(i_L + i_{Lm} + \frac{C_2 v_{out}}{2C_3 R_{out}}\right)\left(\frac{N}{N+1}\right)}{k}\right] \tag{50}$$

where $K = C_1\left(\frac{N-1}{N}\right) - C_2\left(\frac{N}{N+1}\right)$ and $v_{out} = v_{C4} + v_{C5}$.

The state-space matrices for State II are:

$$\mathrm{A}_2 = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_m} & 0 & 0 & -\frac{1}{L_m} \\ a_{31} & a_{32} & 0 & 0 & 0 & a_{36} & a_{37} \\ a_{41} & a_{42} & 0 & 0 & 0 & a_{46} & a_{47} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2C_3R} & \frac{1}{2C_3R} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2C_4R} & \frac{1}{2C_4R} \\ a_{71} & a_{72} & 0 & 0 & 0 & a_{76} & a_{77} \end{bmatrix}, \mathrm{B}_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad \mathrm{C}_2 = [0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 1 \;\; 1] \tag{51}$$

where the coefficients a_{ij} are defined as: $a_{31} = \frac{1}{K}$, $a_{32} = \frac{1}{K}$, $a_{36} = \frac{1}{K}\frac{C_2}{2C_3R}$, $a_{37} = \frac{1}{K}\frac{C_2}{2C_3R}$, $a_{41} = \frac{1}{K}\frac{N}{N+1}$, $a_{42} = \frac{1}{K}\frac{N}{N+1}$, $a_{46} = \frac{1}{2C_3R} + \frac{1}{K}\frac{N}{N+1}\frac{C_2}{2C_3R}$, $a_{47} = \frac{1}{2C_3R} + \frac{1}{K}\frac{N}{N+1}\frac{C_2}{2C_3R}$, $a_{71} = -\frac{1}{C_5} + \frac{1}{K}\frac{N}{N+1}$, $a_{72} = \frac{1}{K}\frac{N}{N+1}$, $a_{76} = \frac{1}{C_5R} - \frac{C_2}{2C_3C_5R} + \frac{1}{K}\frac{N}{N+1}\frac{C_2}{2C_3R}$, $a_{77} = \frac{1}{C_5R} - \frac{C_2}{2C_3C_5R} + \frac{1}{K}\frac{N}{N+1}\frac{C_2}{2C_3R}$.

The averaged model over a switching period is:

$$\begin{cases} \dot{\bar{\mathrm{x}}} = \mathrm{A}\bar{\mathrm{x}} + \mathrm{B}\bar{\mathrm{u}} \\ \bar{y} = C\bar{\mathrm{x}} \end{cases} \tag{52}$$

where: $\mathrm{A} = d\mathrm{A}_1 + (1-d)\mathrm{A}_2$, $\mathrm{B} = d\mathrm{B}_1 + (1-d)\mathrm{B}_2$, $\mathrm{C} = d\mathrm{C}_1 + (1-d)\mathrm{C}_2 = \mathrm{C}_1$.

The small-signal model is derived by perturbing the averaged model around a DC operating point. Let:

$$d = D + \hat{d}, \quad v_{in} = V_{in} + \hat{v}_{in}, \quad \mathrm{x} = \mathrm{X} + \hat{\mathrm{x}}, \quad y = Y + \hat{y} \tag{53}$$

The small-signal state-space model is: $\dot{\hat{\mathrm{x}}} = \mathrm{A}\hat{\mathrm{x}} + \mathrm{B}\hat{v}_{in} + \mathrm{F}\hat{d}$, $\hat{y} = \mathrm{C}\hat{\mathrm{x}}$; where $\mathrm{F} = (\mathrm{A}_1 - \mathrm{A}_2)\mathrm{X} + (\mathrm{B}_1 - \mathrm{B}_2)V_{in}$.

The control-to-output transfer function $G_{vd}(s) = \frac{\hat{v}_{out}(s)}{\hat{d}(s)}|_{\hat{v}_{in}=0}$ is:

$$G_{vd}(s) = \mathrm{C}(s\mathrm{I} - \mathrm{A})^{-1}\mathrm{F} \tag{54}$$

With the values provided in Table 4, the matrices A, B, C, and F are computed numerically. The transfer function $G_{vd}(s)$ is then derived. Based on the parameters, the approximate transfer function is:

$$G_{vd}(s) \approx \frac{3200\left(1 + \frac{s}{2\pi \cdot 850}\right)\left(1 - \frac{s}{2\pi \cdot 12.5 \times 10^3}\right)}{\left(1 + \frac{s}{2\pi \cdot 95} + \left(\frac{s}{2\pi \cdot 95}\right)^2\right)\left(1 + \frac{s}{2\pi \cdot 1.2 \times 10^3}\right)} \approx \frac{3200 + 0.5584s - 7.6256 \times 10^{-6}s^2}{1 + 1.809 \times 10^{-3}s + 3.03 \times 10^{-6}s^2 + 3.726 \times 10^{-10}s^3} \tag{55}$$

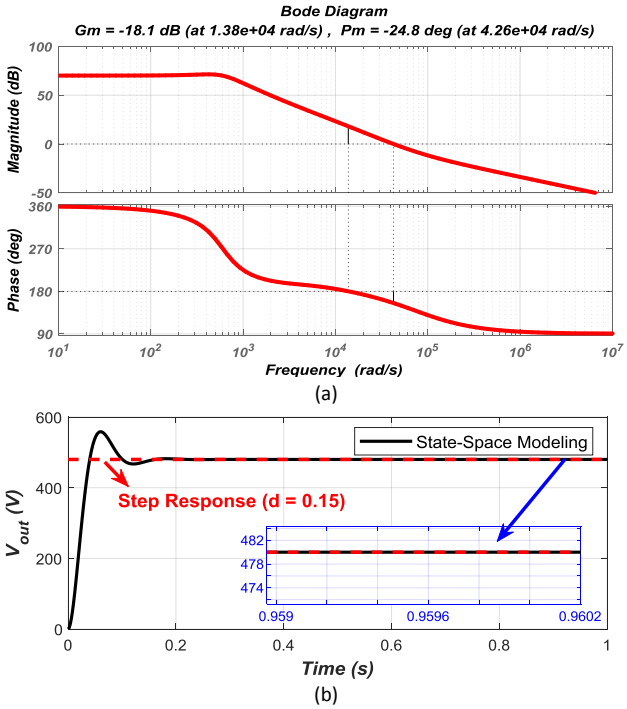


Fig. 8: (a) Frequency-domain evaluation of the derived $G_{vd}(s)$; (b) Step Response (d=0.15) of the derived $G_{vd}(s)$.

As depicted in Fig. 8(a), in the frequency-domain evaluation of the derived $G_{vd}(s)$, the Bode diagram demonstrates that the system exhibits a structurally robust and stable behaviour profile. At very low frequencies, the magnitude response remains flat at approximately 70.1 dB, corresponding to a DC gain of about 3200, which ensures high steady-state accuracy. As illustrated in Fig. 8 (b), for a step input of 0.15 V, this gain predicts a steady-state output near 480 V, consistent with time-domain simulation results (the following section will provide further details). The first significant dynamic feature appears at a pair of complex conjugate poles located at $2\pi \times 95$ rad/s, with a damping ratio close to 0.5; this yields a gentle −40 dB/decade slope beyond the natural frequency, without excessive resonant peaking. A left-half-plane (LHP) zero at $2\pi \times 850$ rad/s subsequently increases the slope by +20 dB/decade and contributes up to +90° of phase lead across its influence band, favourably impacting phase margin around a sub-kilohertz crossover. A single real pole at $2\pi \times 1.2$ kHz returns the slope to −40 dB/decade, curbing high-frequency gain.

The only right-half-plane (RHP) zero, situated at $2\pi \times 12.5$ kHz, is placed well above the intended control bandwidth, so its adverse phase effect remains negligible in practical operation. Phase-wise, the combination of the low-frequency poles, the LHP zero's lead, and the higher-frequency pole produces a crossover region in which the phase remains comfortably distant from −180°, yielding a positive phase margin and a gain margin exceeding unity, parameters indicative of a system that is stable under unity feedback. All poles reside in the left half‑plane, confirming open-loop stability of the plant. This frequency-domain signature aligns with time-domain observations: the system responds quickly to a step command, reaches the predicted steady-state value without significant overshoot, and exhibits no sustained oscillations. The arrangement of poles and zeros not only supports stability but also provides favorable transient performance, with adequate bandwidth for responsive control while avoiding excitation of high-frequency dynamics. The result is a well-shaped open-loop response that, when closed in unity feedback within the recommended crossover range (a few hundred hertz to under one kilohertz), delivers a closed-loop system that is both robust and precise. These attributes position the design as stable, well-tuned, and highly suitable for applications requiring accurate tracking and predictable dynamic behavior.

In the proposed converter, the primary control objective is the implementation of a voltage-mode control (VMC) loop, here realized with a PI regulator, to fix and tightly regulate the converter's output voltage. The small-signal model and Bode diagram of $G_{vd}(s)$ confirm a high DC gain (~70 dB) and a phase profile that comfortably supports unity-feedback operation, enabling the PI controller to achieve precise steady-state voltage regulation with straightforward compensation design. This simplicity, combined with inherent plant stability, makes VMC-PI highly effective for the intended operating conditions, delivering the expected ~480 V steady-state.

Results and Discussion: Simulation, Experimental Evaluations, and Analysis

To comprehensively validate the functionality of the proposed UGEA-S DC/DC converter, and to ensure the accuracy of the theoretical calculations, experimental results and extensive simulations are carried out using MATLAB/SIMULINK software.

A. Simulation Results

The simulation process plays a crucial role in confirming the expected performance of the system under varying operational conditions. The selection of component values strictly follows the theoretical calculations established in Section 3, ensuring adherence to the optimal operational parameters. These components, whose complete specifications are meticulously detailed in Table 4, are systematically integrated into the simulation framework to provide a realistic representation of the actual implementation. By incorporating these predefined component values, the simulation effectively replicates the anticipated behavior of the converter, allowing for a precise evaluation of its electrical characteristics. Additionally, the conversion ratio, which serves as a key metric in assessing the voltage transformation capability of the converter, is determined as $M = V_{out}/V_{in} = 480/60 = 8$, reflecting the significant voltage gain achieved through the proposed topology.

Fig. 9 presents the simulated voltage and current waveforms associated with MOSFET S_1 within the proposed converter system. These waveforms, denoted as V_{S1} for voltage and I_{S1} for current, serve as critical indicators of the switching behavior and electrical performance of the MOSFET under operating conditions. By analyzing these waveforms, the dynamic characteristics of the MOSFET, including voltage/current stresses, conduction intervals, and transient responses, can be thoroughly evaluated. This insight helps validate the effectiveness of the converter design and ensures its suitability for high-efficiency power conversion applications.

Table 4: Key Parameters of the proposed converter for simulation and practical analysis

Parameters	Values
Input voltage (V_{in})	$60V$
Output voltage (V_{out})	$480V$
Max. output power (P_{out}^{max})	$1kW$
Power switch (S_1)	MOSFET, FDA59N30 N-Channel with $R_{ds}(ON).056\Omega$, $T_{d,on} = 290ns$, $T_{d,off} = 250ns$, $V_{DSS} = 300V$, $I_D = 59A$
Diode D_1	Ultrafast diode, RURP3060, $600V/30A$, $r_D = 0.04$, V_F^{max}=1.5V
Diodes D_2, D_3 and D_4	Ultrafast diode, RURP3040, $400V/30A$, $r_D = 0.03$, V_F^{max}=1V
Capacitors C_1 and C_2	$200\mu F/200$V, electrolytic with $r_c = 70m\Omega$
Capacitors C_3, C_4 and C_5	$50\mu F/450V$, polyester with $r_c = 30m\Omega$
Switching frequency (f_s)	$70KHz$
Input inductor (L)	$700\mu H$ with $r_L = 0.12\Omega$, toroidal core $32 \times 25 \times 9$ (iron powder)
Coupled inductor	$L_m = 500\mu H$, $L_k = 1.4\mu H$, with $N = 3$ ($N_s = 54$ and $N_P = 18$), ferrite core $EI - 33/29/13$ with $0.25mm$ air gap, $r_{Lm} = 0.15\Omega$
Photocoupler	$TOSHIBA - TLP250$
Microcontroller	$ARM - LPC1768$

In a MOSFET operating within a converter, voltage and current waveforms are crucial for assessing its switching behavior and overall performance. Also, analyzing these waveforms helps identify switching losses and conduction intervals, which are essential for optimizing converter efficiency. As observed in Fig. 9, the voltage/current stresses experienced by the MOSFET S_1, denoted as $V_{S_1}^{Stress}$ and $I_{S_1}^{Avg}$, are measured at 230V and 28A, respectively. These values indicate the electrical strain imposed on the MOSFET during operation.

Fig. 10 presents the simulated voltage and current waveforms corresponding to the diodes D_1, D_2, D_3 and D_4 within the proposed converter system. These waveforms offer a crucial insight into the electrical behavior of the diodes, reflecting their switching characteristics and conduction periods under different operating conditions. The voltage waveform indicates the potential difference across the diodes as they alternate between forward conduction and reverse blocking states.

During the conduction phase, the diode allows current to flow, maintaining a relatively low voltage drop.

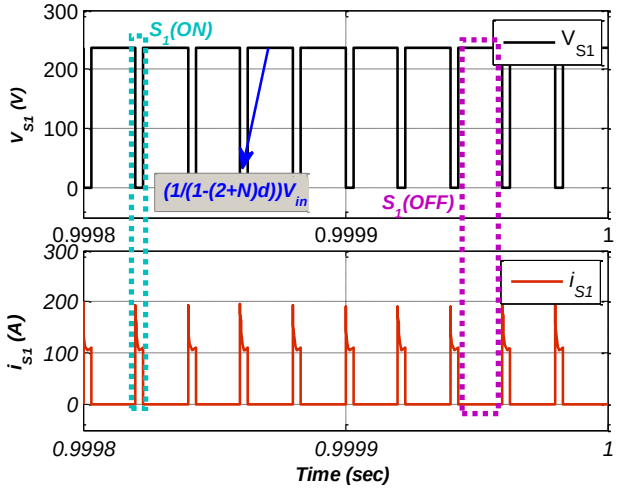


Fig. 9: Simulated voltage and current waveforms of MOSFET S_1 in the proposed UGEA-S DC/DC converter.

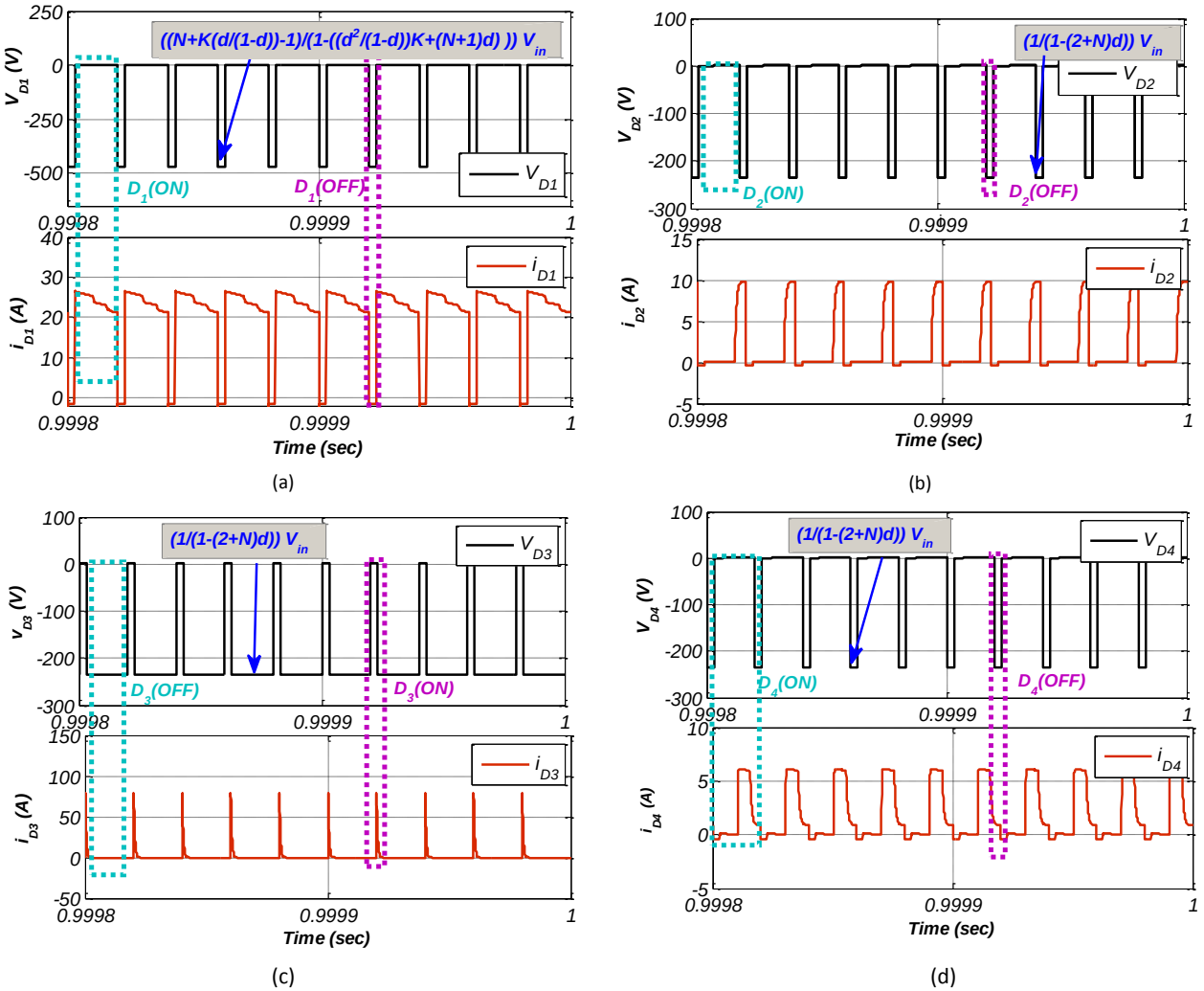


Fig. 10: Simulated voltage and current waveforms of diodes in the proposed UGEA-S DC/DC converter, (a) D_1; (b) D_2; (c) D_3; and (d) D_4.

Conversely, when the diode transitions to the OFF state, the voltage increases as it withstands the reverse-biased condition, preventing undesired current flow. Similarly, the current waveform depicts the diode's conduction pattern, revealing the duration and magnitude of current flow during each switching cycle. The analysis of these waveforms is essential for assessing diode performance, including factors such as voltage stress, recovery characteristics, and overall efficiency. Understanding these patterns enables optimized design choices, ensuring minimal losses and reliable operation of the converter in high-efficiency energy conversion applications.

As observed in Fig. 10, the voltage stresses experienced by the diodes, denoted as $V_{D_1}^{Stress}$, $V_{D_2}^{Stress}$, $V_{D_3}^{Stress}$ and $V_{D_4}^{Stress}$, are measured at 520V, 230V, 230V and 230V, respectively. These values indicate the electrical strain imposed on the diodes during operation. Additionally, an important observation derived from the figure is the average current flowing through each diode. Specifically, the mean current levels, represented as $I_{D_1}^{Avg}$, $I_{D_2}^{Avg}$, $I_{D_3}^{Avg}$ and $I_{D_4}^{Avg}$, are recorded at 10A, 5.25A, 20.3A and 2.65A, respectively, all of which fall within acceptable operational limits, ensuring stable performance within the converter system.

Furthermore, as depicted in Fig. 11, the average current of the input inductor, represented as I_L^{Avg}, is precisely 19.5A.

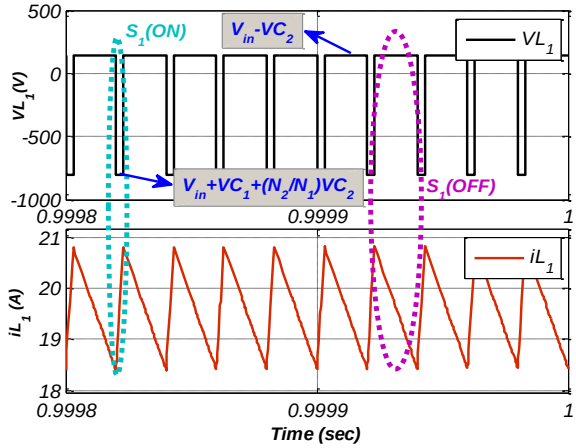


Fig. 11: Simulated voltage and current waveforms of input inductor L.

This value aligns perfectly with the theoretically derived average inductor current, verifying the accuracy of the analytical predictions. The current flowing through the input inductor can be expressed as $I_L^{Avg} = MI_o$, where M represents the voltage gain. Consequently, the average input inductor current is given by $I_L^{Avg} = [2/(1-(2+N)d)]I_o$. This equation establishes the relationship between the average inductor current and key circuit parameters, including the duty cycle d and the turns ratio factor N; the expression highlights how variations in d and N influence the inductor's current behavior, essential for optimizing performance and efficiency in high-gain DC-DC conversion applications.

In addition, Fig. 12 provides a detailed graphical representation of the output voltage and current characteristics of the proposed converter. By carefully analyzing the figure, it becomes evident that the mean output voltage reaches a stable level of 480V, maintaining consistency throughout the observed time frame. Simultaneously, the corresponding average output current is measured at 1.83A, showcasing a steady and predictable operational behavior. These numerical results exhibit a remarkable level of agreement with the theoretical predictions derived from prior analytical calculations, further affirming the accuracy and dependability of the converter's design. The close correspondence between the simulated outcomes and the theoretical values underscores the effectiveness of the proposed methodology, demonstrating that the underlying operational principles have been correctly formulated and executed.

Furthermore, this alignment between expected and observed performance not only validates the theoretical framework governing the converter's functionality but also highlights its practical feasibility for real-world applications. The precision with which the design adheres to its calculated parameters reinforces confidence in its implementation, ensuring that the converter can reliably perform as intended in practical scenarios where consistent voltage and current regulation are essential.

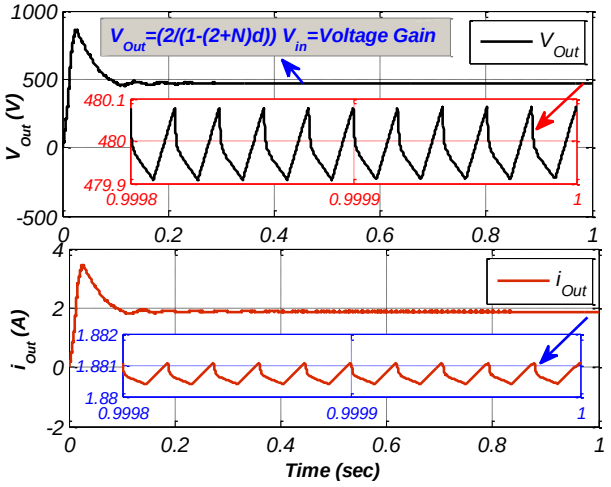
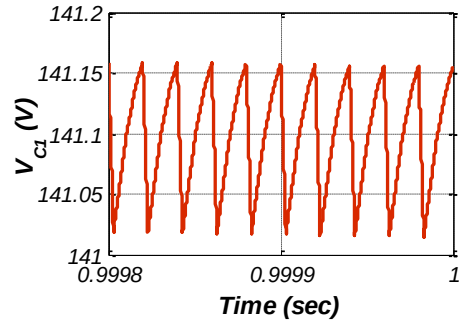
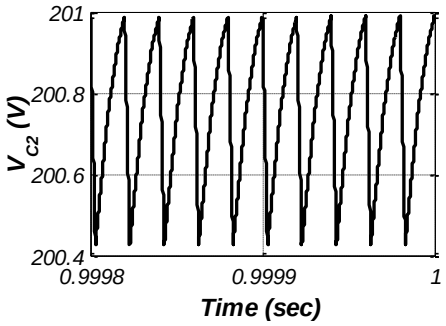


Fig. 12: Simulated waveforms illustrating the voltage and current behavior at the output load.

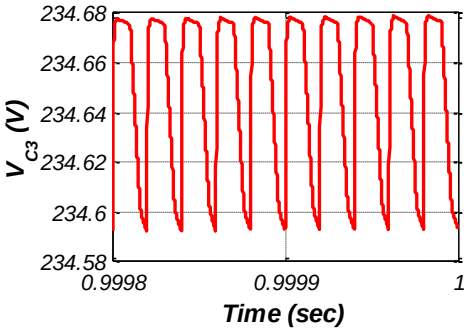
The capacitor voltages are illustrated in Fig. 13. As shown, capacitors C_3, C_4, and C_6 maintain an identical average voltage of approximately 234.6V, aligning with the theoretical calculations from (22). Additionally, capacitor C_1 experiences the lowest voltage stress. By carefully analyzing these observations, it becomes evident that the theoretical calculations governing the converter's voltage characteristics are highly accurate.



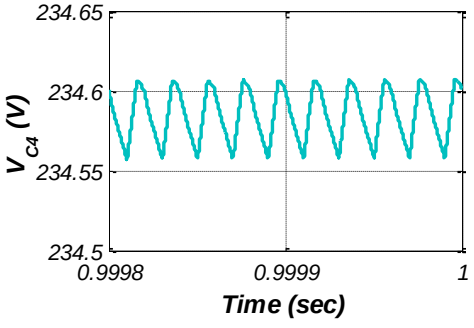
(a)



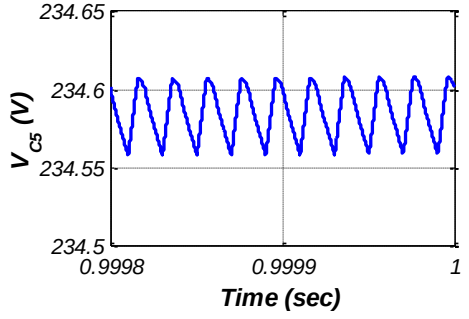
(b)



(c)



(d)



(e)

Fig. 13: Simulated waveforms illustrating the voltage of capacitors, (a) V_{C_1}; (b) V_{C_2}; (c) V_{C_3}; (d) V_{C_4}; and (e) V_{C_5}.

The strong correlation between expected and observed performance underscores the meticulous engineering approach taken during the design process. This level of precision enhances the credibility of the proposed converter, making it a promising candidate for practical implementation in scenarios requiring consistent voltage regulation and minimal electrical stress on critical components.

Fig. 14 presents the instantaneous input power, output power, and the corresponding efficiency at a 1 kW operating point.

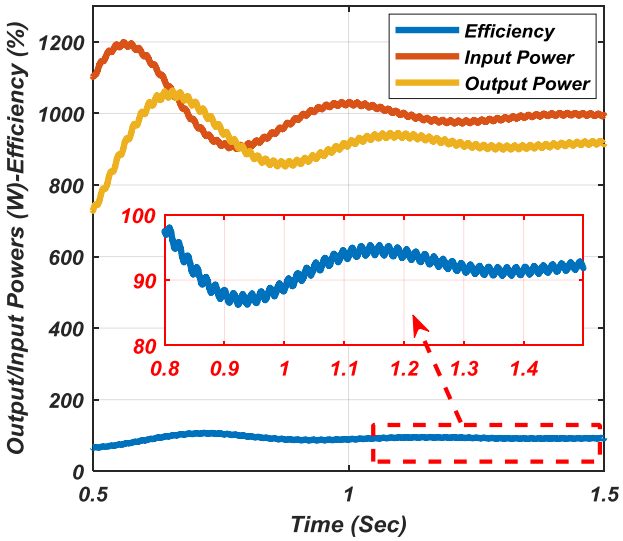


Fig. 14: Simulated waveforms showing input power, output power, and corresponding efficiency.

After a short transient, the two power traces become nearly parallel, with a constant separation equal to the aggregate converter losses, and the efficiency saturates in the mid-92% band (≈92–96%). This plateau aligns with the theoretical efficiency trends previously derived: peak efficiency occurs at moderate power (96.93% near 230 W), while at higher power the loss components, MOSFET switching/conduction, diode forward/recovery, magnetic core and copper, and capacitor ESR, grow in proportion to current and switching energy, producing the steady power gap observed between Pin and Pout. The close agreement between the simulated time-domain power balance and the analytical loss budget confirms that the 1 kW efficiency result is fully consistent with the earlier theory.

In the Evaluation of Power Dissipation and Efficiency Metrics study for the proposed UGEA‑S converter, a full theoretical and simulation‑based breakdown of losses has been performed to validate the analytical efficiency model and identify dominant dissipation sources. At the rated condition, losses are classified into MOSFET, diode, magnetic, and capacitor ESR categories. For the MOSFET, conduction loss, switching loss, and output‑capacitance loss were summed to ~12.53 W. The four diodes together contributed the largest share, about 19.25 W at

500 W input, driven by forward-voltage and conduction ESR effects. Magnetic losses in the input and coupled inductors were ~4.95 W, including core and winding components, while capacitive ESR losses across all devices were only ~1.4 W. At 500 W, the total loss was ~38.13 W, yielding $\eta \approx 92.91\%$; the peak measured/simulated efficiency was 96.93 % near 230 W, remaining above 92 % across the load range. Loss-share analysis shows diodes at ~51 % of total dissipation, MOSFET ~32 %, magnetics ~13 %, and capacitors ~4 %. Under the extended 1 kW simulation, input and output power waveforms (Fig. 14) exhibited a steady offset equal to the calculated total loss, with efficiency stabilizing in the mid-92 % range, precisely matching the theoretical predictions and loss budget trends. This agreement between the analytical calculations, component-level loss allocations, and time-domain simulation confirms the robustness of the proposed efficiency model and highlights that future gains could be achieved primarily through reducing semiconductor conduction and recovery losses.

B. Experimental Results

To further validate the theoretical and simulation findings, a 1 kW laboratory prototype of the proposed UGEA-S DC/DC converter was constructed, as depicted in Fig. 15. The control structure, implemented using an ARM-LPC1768 microcontroller and a TOSHIBA TLP250 gate driver, was designed to generate the necessary PWM signal for switch S_1. In the proposed converter, a voltage-mode control strategy is implemented to ensure precise regulation of the output voltage under varying load and input conditions. The control system continuously measures the actual output voltage and compares it with a predefined reference value, generating an error signal that reflects the deviation from the target setpoint. This error is processed by a proportional–integral (PI) controller, which dynamically adjusts the control signal to minimize both steady-state error and transient response overshoot. The PI controller's output is then used to modulate the duty cycle of the pulse-width modulation (PWM) signal driving the converter's power stage. By finely tuning the duty cycle in real time, the system compensates for disturbances and component tolerances, thereby maintaining the output voltage at the desired setpoint with high accuracy. This approach leverages the inherent simplicity and robustness of voltage-mode control while ensuring stability and rapid dynamic performance.

The experimental results presented in Figs. 16-22 confirm the practical viability of the converter and demonstrate a strong correlation with the simulated waveforms. Fig. 16 presents the experimental gate-to-source voltage (PWM) and drain-to-source voltage (V_{DS}) waveforms of the MOSFET S_1. The measured voltage stress on S_1 is approximately 232 V, which aligns perfectly with the simulated value of 230 V. The clean switching transitions observed in the experimental V_{DS} waveform, despite minor ringing due to parasitic inductances, confirm the effective mitigation of voltage stress achieved by the proposed topology.

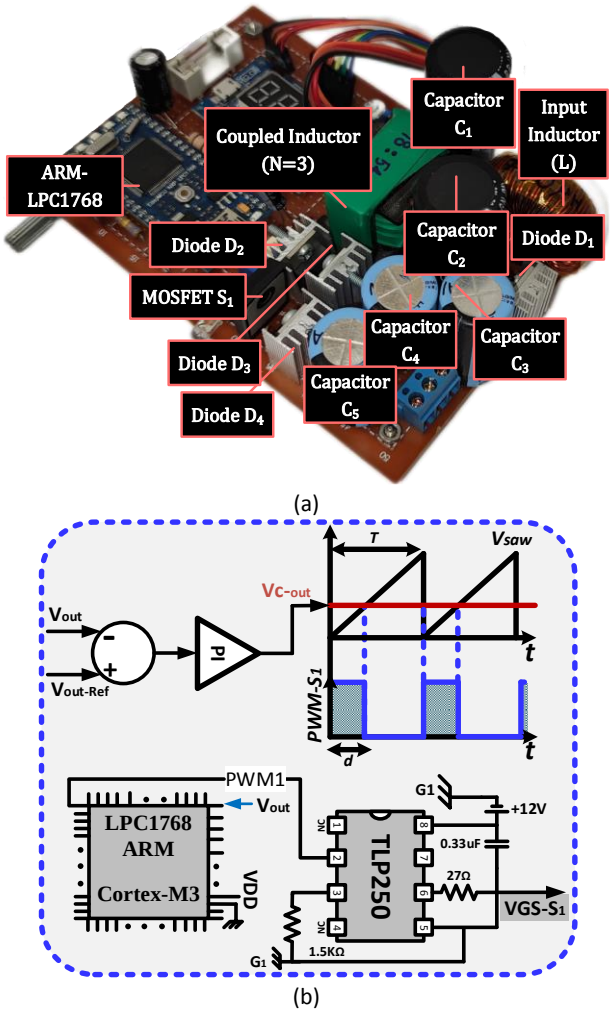


Fig. 15: (a) Prototype hardware implementation; and (b) closed-loop controller architecture of the proposed UGEA-S DC/DC converter.

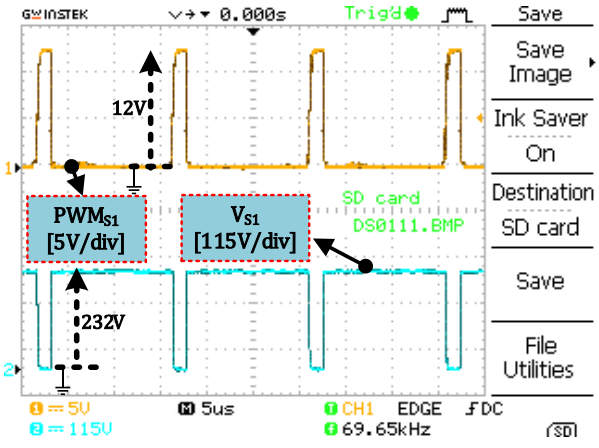


Fig. 16: Experimental waveforms showing PWM and voltage waveforms of MOSFET S_1.

Fig. 17 shows the experimental voltage waveforms across capacitors C_1 and C_2. The measured voltages are stable at 142 V and 202 V, respectively. These values are in excellent agreement with the simulated results (141 V for C_1 and 200.6 V for C_2), validating the steady-state analysis and the volt-second balance principles applied to the magnetic components.

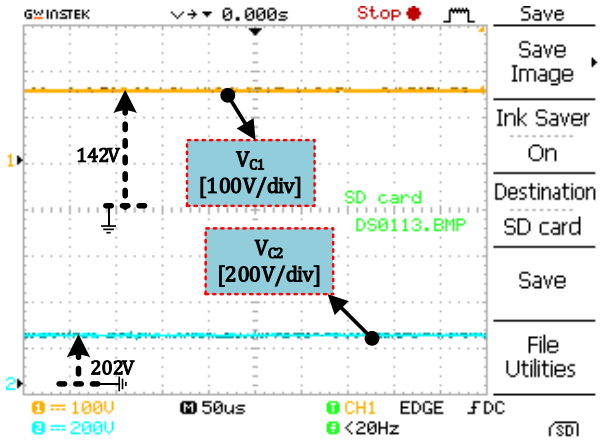


Fig. 17: Experimental waveforms illustrating the voltage behavior of capacitors V_{C_1} and V_{C_2}.

Fig. 18 displays the voltages across capacitors C_3, C_4, C_5 and the output voltage. The capacitors C_3, C_4, and C_5 each sustain a stable voltage of 238 V, resulting in a combined output voltage of 476 V. This experimental output matches the target and simulated value precisely. The minimal ripple on the output voltage (<2%) underscores the effectiveness of the output capacitor network in smoothing the voltage delivered to the load.

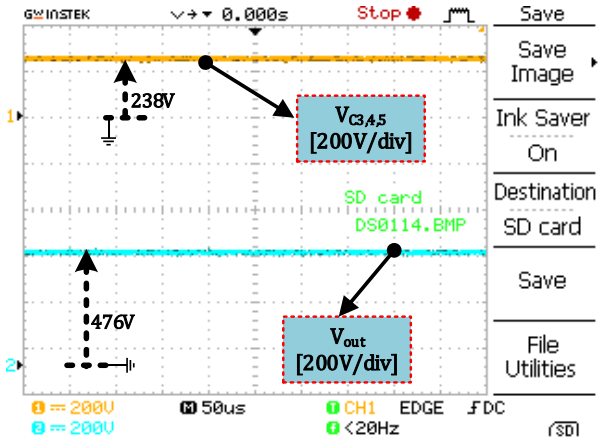


Fig. 18: Experimental waveforms illustrating the voltage behavior of capacitors $V_{C_{3,4,5}}$ and the output voltage V_{out}.

Fig. 19 illustrates the voltage stresses on diodes D_1, D_2, and D_4. The experimental peak reverse voltages are measured at 525 V for D_1 and 240 V for both D_2 and D_4. These results are consistent with the simulated stresses (520 V, 230 V, 230 V), confirming the analytical derivations for diode stress. The fast switching and clean blocking states indicate minimal reverse recovery issues.

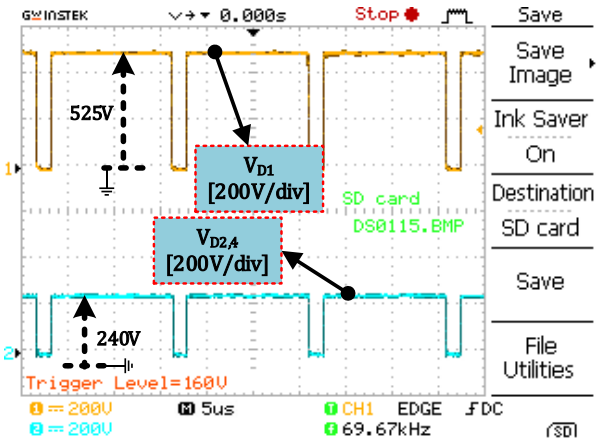


Fig. 19: Experimental waveforms illustrating the voltage behavior of diodes $V_{D_{1,2,4}}$.

Fig. 20 captures the voltage stress on diode D_3 and the current through the input inductor L_1. The stress on D_3 is measured at 242 V, aligning with simulations. The input inductor current has an average value of 19.5 A with a continuous, low-ripple profile, which is identical to the simulated waveform. This experimentally validates the converter's key feature of providing a continuous input current, reducing stress on the source.

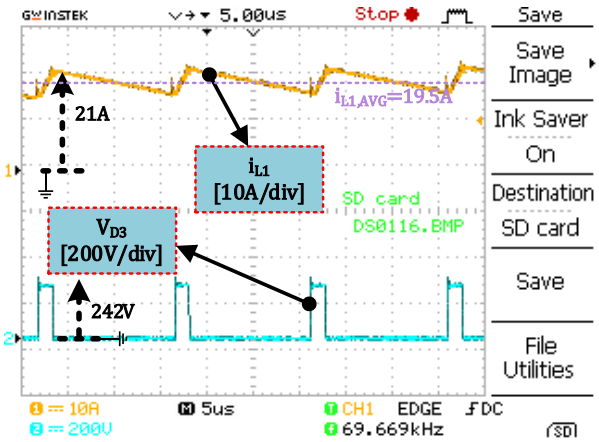


Fig. 20: Experimental waveforms illustrating the voltage behavior of diode V_{D_3} and current waveforms of input inductor L_1.

Fig. 21 demonstrates the converter's resilience under a significant input voltage disturbance. The input voltage is abruptly dropped from 60 V to 25 V. The experimental results show that the closed-loop control system successfully maintains the output voltage regulation at 476 V. This robust performance under dynamic input conditions matches the simulation predictions and highlights the converter's suitability for applications with fluctuating source voltages, such as electric vehicle battery systems.

Fig. 22 characterizes the startup behavior and the load transient response. Upon startup, the output voltage smoothly rises to its regulated 478 V setpoint with minimal overshoot. For the load transient test, the

output current is stepped from 1 A to 2 A. The output voltage exhibits a minor deviation of less than 15 V (~3% dip) and recovers to its steady-state value within 10 ms. This transient performance is satisfactory and aligns with the simulated response, confirming the stability and effectiveness of the implemented voltage-mode PI controller.

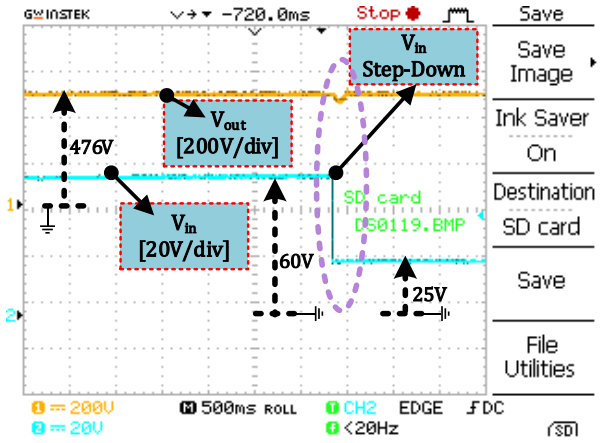


Fig. 21: Performance of the converter under abrupt input voltage drop from 60 V to 25 V.

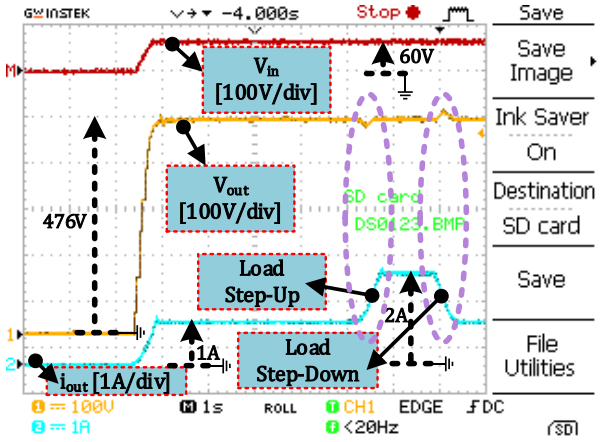


Fig. 22: Startup characteristics and load transient response of the converter for a step change in output current (i_{out}: 1 A to 2 A).

The close agreement between all experimental measurements and the corresponding simulation results comprehensively validates the design methodology, operational principles, and performance metrics of the proposed UGEA-S DC/DC converter.

C. Critical Evaluation of Simulated and Experimental Design: Merits and Limitations

The proposed UGEA-S DC/DC converter demonstrates several notable strengths, as confirmed by experimental evaluations, simulation results and theoretical analysis. However, like any engineering design, it also presents some limitations that merit discussion.

I) Merits:

- **Exceptional Voltage Gain:** The converter achieves a voltage gain of up to 8× (480 V output from a 60 V input), making it highly suitable for high step-up applications such as electric vehicles and renewable energy systems.
- **High Efficiency:** The system maintains an efficiency of 96.93% at 230 W and remains above 92% even at full load, indicating minimal power loss across components.
- **Continuous Input Current:** The input inductor sustains a smooth current profile (average 19.5 A), which reduces stress on the power source and improves system reliability.
- **Reduced Voltage Stress:** Voltage stress on the MOSFET and diodes remains within safe operational limits (230–460 V), allowing the use of components with lower ratings and cost.
- **Simplified Control Strategy:** The converter operates in two distinct switching states, which simplifies control implementation and reduces computational overhead.

II) Limitations:

- **Component Count and Complexity:** While optimized compared to other topologies, the design still requires multiple capacitors and diodes, which may increase PCB area and assembly effort.
- **Thermal Management Needs:** Despite reduced stress, the high current levels (e.g., 20.3 A through D_3) may necessitate robust thermal management, especially under continuous full-load operation.
- **Idealized Assumptions in Simulation:** The simulations assume ideal components (no parasitic effects for passive components and also perfect switching), which may not fully capture real-world behavior such as EMI, leakage inductance, and thermal drift.
- **Integration of a Basic Control Strategy:** To enhance the practicality of the proposed converter, a simple PI controller has been implemented. This controller provides basic output voltage regulation and demonstrates the converter's ability to maintain stability under nominal operating conditions. Although the PI controller is widely used due to its simplicity and ease of implementation, it has inherent limitations in handling nonlinearities, fast transients, and parameter variations.
- **Efficiency Drop at High Load:** Although efficiency remains above 92%, a slight decline is observed at maximum load (1 kW), which may affect performance in sustained high-power applications.

In summary, the proposed converter exhibits strong performance characteristics and addresses key challenges in high-gain DC/DC conversion. However, future work should focus on experimental validation, parasitic-aware modeling, and thermal optimization to ensure robust real-world deployment.

Conclusion

This study presented a novel UGEA-S DC/DC converter that integrates switched-capacitor techniques to achieve exceptional voltage amplification and operational stability. The converter addresses critical limitations of conventional designs, including diode reverse recovery, high voltage stress, and discontinuous current profiles. Through rigorous theoretical modeling, MATLAB/Simulink simulations and extensive experimental results, the converter's performance was validated under realistic operating conditions. Numerical results revealed a voltage gain of 8×, with the output voltage reaching 480 V from a 60 V input. The converter maintained a continuous input current of 19.5 A and limited voltage stress on the MOSFET to 230 V, enabling the use of low R_{ds}(on) switches for improved efficiency. Diodes operated within safe voltage and current ranges, and capacitors sustained stable voltages, confirming the converter's reliability.

Efficiency peaked at 96.93% at 230 W and remained above 92% at full 1 kW load, underscoring the design's robustness. The comparative analysis with existing topologies highlighted the UGEA-S converter's superior voltage gain, reduced component stress, and optimized component count. These attributes make it a compelling candidate for integration into electric vehicle powertrains, battery charging systems, and other high-gain DC/DC applications. Future work should explore advanced control strategies to further refine performance and scalability.

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Pezhman Bayat: Writing – review & editing, Writing – original draft, Visualization, Validation, Supervision, Software, Resources, Project administration, Methodology, Investigation, Funding acquisition, Formal analysis, Data curation, Conceptualization.

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Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the ethical issues including plagiarism, informed consent, misconduct, data fabrication and, or falsification, double publication and, or submission, and redundancy have been completely witnessed by the authors.

Abbreviations

UGEA-S	Ultra-Gain Enhanced A-Source
DC-DC	Direct Current to Direct Current
IN	Impedance Network
EV	Electric Vehicle
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
CCM	Continuous Conduction Mode
PWM	Pulse Width Modulation
PI	Proportional-Integral
VMC	Voltage-Mode Control
ESR	Equivalent Series Resistance
ZVS	Zero Voltage Switching
EMI	Electromagnetic Interference
PCB	Printed Circuit Board
DSP	Digital Signal Processor
FPGA	Field-Programmable Gate Array
PID	Proportional-Integral-Derivative
PLL	Phase-Locked Loop
RMS	Root Mean Square
AC	Alternating Current

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