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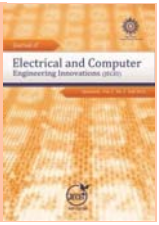

THD Analysis in Closed-Loop Analog PWM Class-D Amplifiers

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ABSTRACT

In this paper, we investigate the parameters affecting Total Harmonic Distortion (THD) and Power Supply Rejection Ratio (PSRR) in PWM Class D Amplifiers (CDAs) on the basis of linear models with feedback. From our mathematical analysis, we show that the THD of a PWM Class D amplifier with feedback can be improved by increasing the gain of the integrator through adding another amplifier at the output of the integrator. We also show that the THD can be further improved by means of two cascaded amplifiers with a single pole. We verify our analysis by means of PSPICE simulations. Simulation results show that the THD of the gain boosting and the two cascaded amplifiers with a single pole CDAs can be improved by as much as 1.4 times and 2 times, respectively.

1. INTRODUCTION

Class D amplifier is known for its high power efficiency. In fact, its theoretical efficiency is 100%. Therefore, CDA can achieve a higher power efficiency compared to other types of amplifiers such as Class-A or Class-AB [1]. This is primarily due to the switching mode operation of its output stage. However, its poor linearity performance limits a complete market acceptation. Class D audio power amplifiers are mainly used in hearing aids, headphone amplifiers, wireless phones, audio portable players, notebooks, and portable video games, where a high efficiency performance is essential to maximize the battery life. Of the modulation techniques used in CDAs, the pulse width modulation (PWM) [2] is the most popular architecture. Its circuitry is simple and stable with low power consumption. This is the modulation of interest in this paper. The CDA shown in Figure 1 comprises a comparator, an output stage, and an LC low-pass filter. At the PWM, the comparator compares the input modulating signal with an internally generated carrier waveform, usually saw-tooth-like or triangular like [3],[4] which generates a series of width modulated pulses, the PWM signal. The Class-D output stage is half bridge and is still employed by most of the current art commercial CDA designs due to its simple structure, reduced material cost and smaller form factor [5].

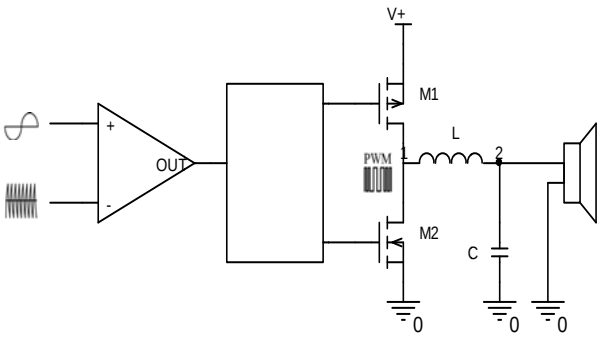

Figure 1: Schematic diagram of an open loop CDA.

The LC low-pass filter attenuates the unwanted carrier signal component of the PWM signal, hence retrieving an equivalent amplified analog input signal at the load. In some applications [6], the sound quality of an audio amplifier is determined by its performance in terms of distortion (e.g. THD). One of the problems with open-loop Class D amplifier is the susceptibility of the PWM or output stage to non-

linearity and noise [7]-[9]. In Class D audio power amplifiers, these problems can be eliminated by negative feedback from the Class D output back to the input. As a result, the THD of the closed-loop Class D amplifier usually suffer from poorer THD performance when input signal frequency increases beyond 3 kHz [8]. In this paper, we investigate the mechanism for THD in closed-loop CDAs on the basis of linear models. We show how the THD can be improved byincreasing the gain of the integrator through the gain boosting and the two cascaded amplifiers with a single pole in the feed-back loop.

2. Modeling A Closed-Loop Class D Amplifier

A. A 2nd-order closed-loop class D amplifier

A 2nd-order closed-loop class D amplifier is depicted in Figure 2. This design is typical for some commercial CDAs [10], [11].

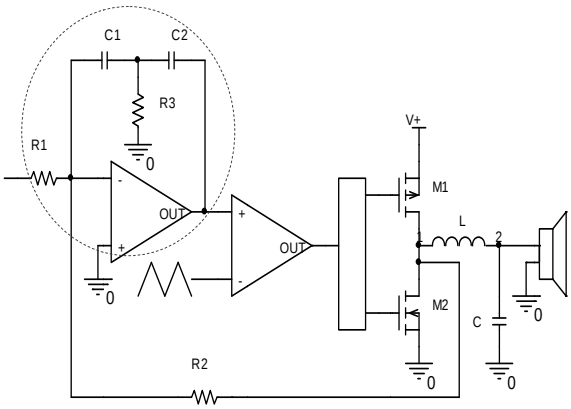

Figure 2: Closed-Loop PWM-CDA.

The 2nd-order closed-loop CDA comprises: an open-loop PWM CDA, a 2nd-order integrator, a feedback network ($R_1$and R_2) and the load (including the low pass filter and the loudspeaker). The 2nd-order integrator serves as an integrator and a Sumer that sums the input and the feedback signals [11]. Now, the relationship between the circuit elements in the loop filter is recorded. The closed-loop CDA can be modeled linearly. Therefore, we model this closed-loop PWM CDA simply by applying a feedback to the open-loop PWM CDA that is shown in Figure 3.

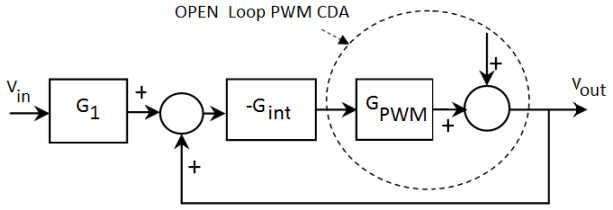

Figure 3: A linear model of the 2nd-order closed-loop Class D amplifier.

In this model, the transfer function of each sub-block is given as:

$$G_1 = \frac{R_2}{R_1} \tag{1}$$

$$G_{\text{int}} = \frac{-R_1}{R_1 + R_2} \frac{Av\,[s(C_1 + C_2)R_3 + 1]}{s^2 A + s[R_3(C_1 + C_2) + (R_1 \| R_2)C_1] + 1} \tag{2}$$

$$A = (R_1 \| R_2)(1 + Av)\,C_1 C_2 R_3$$

The transfer function of the integrator in equation (2) can be simplified as follows:

$$\frac{v_{\text{int}}}{v_o} = \frac{s(C_1 + C_2)R_3 + 1}{s^2 C_1 C_2 R_2 R_3} \tag{3}$$

For simplicity, v_{out} voltage is written just as v_o. In this model, the nonlinearities due to harmonic distortion is denoted as V_n, and G_{pwm} represents the gain of the PWM stage, which is equal to the ratio of supply voltage V_{DD} and the modulation index M [11].

$$G_{PWM} = \frac{V_{DD}}{V_{carrier}} = M.V_{DD} \tag{4}$$

We derive the system transfer function ($\frac{V_{out}}{V_{in}}$) as:

$$\frac{V_{out}}{V_{in}} = \frac{G_1 G_{\text{int}} G_{PWM}}{1 + G_{in} G_{PWM}} \tag{5}$$

Using the above equation, the loop gain can be calculated as:

$$LOOP\,GAIN = G_{\text{int}} G_{PWM} \tag{6}$$

The established definition of THD is

$$\%THD = \frac{\sqrt{V^2_{rms@2f} + V^2_{rms@3f} + \ldots + V^2_{rms@nf}}}{V^2_{rms@f}} \times 100 \tag{7}$$

Where $V_{rms@f}$is the output fundamental component at f and $V_{rms@2f}$, $V_{rms@3f}$, and $V_{rms@nf}$are the output harmonic components at 2, 3 and n, respectively. We can show that the THD of this closed-loop Class D amplifieris:

$$\%THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^{\,2}}}{G_1 (LOOP\ GAIN)\, V_{in}} \times 100 \tag{8}$$

And, PSRR is given by [11]:

$$PSRR = \frac{V_{out}}{N}\Big|_{V_{in}=0} = \frac{\frac{V_n}{N}}{1+G_{\text{int}}G_{PWM}} \quad (9)$$

where N is the noise of the supply line, and $\frac{V_n}{N} = \frac{1}{2}$ is determined for an open-loop PWM CDA[12].

From (8) it is noted that THD is largely determined by (a) the gain of the integrator, G_{int}, (b) the gain of the PWM stage, G_{pwm}, or the loop gain and (c) the gain of the input stage, G_1. Equation (9) shows that the PSRR is dependent on two parameters, G_{int} and G_{pwm}. Equations (8) and (9) indicate that the THD and the PSRR of a PWM CDA with feedback can be improved by increasing these parameters. From the above parameters, the gain of the integrator is the dominant factor that determines the THD and the PSRR of the closed-loop CDA. This individual parameter will now be discussed in detail.

B. The gain of the integrator, G_{int}

Amongst the 3 parameters, the gain of the integrator, G_{int}, is the most critical parameter because it contributes the major part to the loop gain in (8).

The frequency response of a 2nd-order integrator based on the RC values as R_3=3kΩ and C_1=C_2=470 pF is shown in Figure 4.

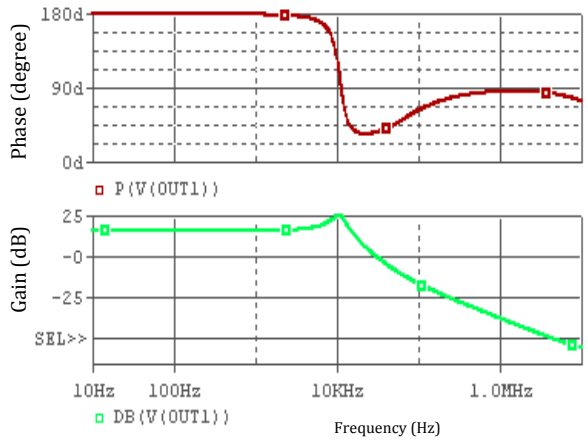

Figure 4: Frequency response of a 2nd-order integrator.

We remark from Figure 4 that in the low frequency range (Less than 1 kHz), the integrator gain is, as expected, very close to the opamp open-loop gain. Subsequently, applications of a higher open-loop gain opamp provides lower THD.

C. Increasing the gain of the integrator, and its associated circuitries

A simple method for increasing the loop gain is by adding another amplifier at the output of the integrator which is shown in Figure 5.

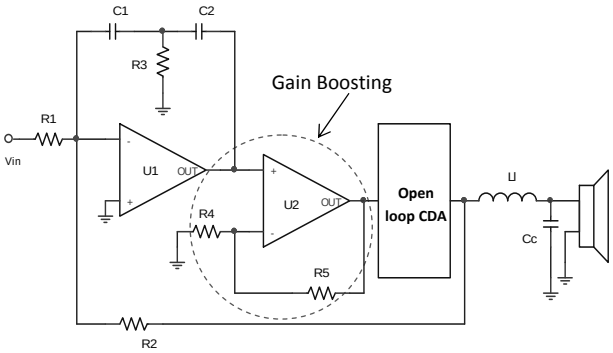

Figure 5: Closed-loop PWM-CDA with again boosting.

In this case, the loop gain increases by the coefficient shown in equation (10).

$$LoopGain = G_A \times (\frac{R_5}{R_4} + 1) \quad (10)$$

Where G_A is the gain loop before applying the gain boosting and $(R_5 / R_4 + 1)$ is the gain of the second amplifier. The frequency response of circuit for a gain boosting of 3 is plotted in Figure 6.

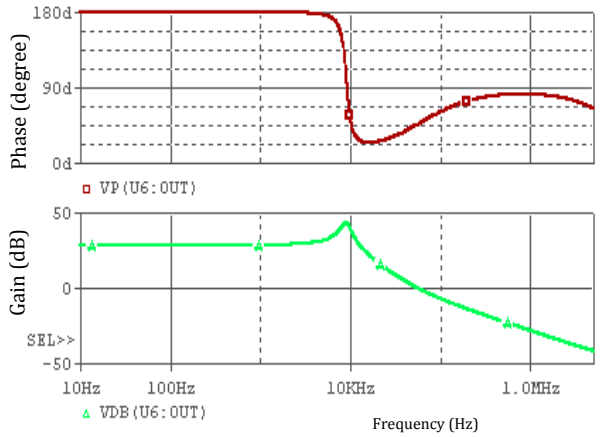

Figure 6: Frequency response of the closed-loop CDA with a gain boosting.

From the frequency response in Figure 6, we note that the gain at the audio frequency range is improved by as much as 17dB. The phase margin at unity gain is also improved by as much as 46°thereby improving the stability of the amplifier. However, this approach will decrease the amount of attenuation on the carrier and as a result larger carrier amplitude will appear at the output of the integrator.

We can increase the gain of the integrator by two cascaded amplifiers with a single pole. We investigate the different design to 2nd-order integrator and depicted in Figure 7.

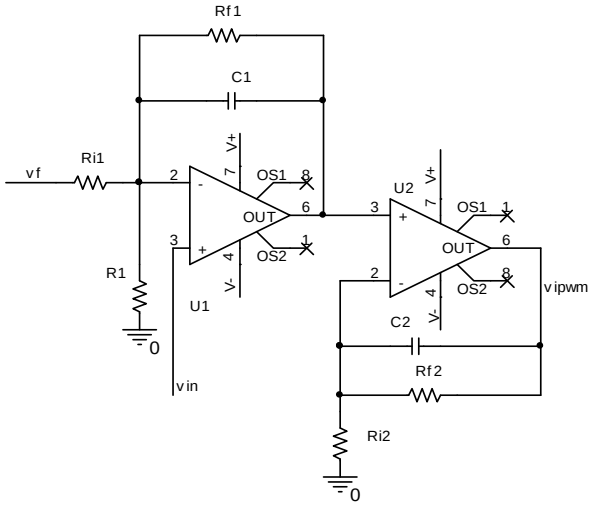

Figure 7: The proposed of a 2nd-order integrator by two cascaded amplifiers with a single pole.

Transfer function for the integrator by two cascaded amplifiers can be derived as follow:

$$G_{\text{int}} = \frac{R_{f1}}{R_{i1}} \cdot \frac{sR_{f2}C_2 + \frac{R_{f2}}{R_{i2}} + 1}{(sC_1R_{f1} + 1)(sC_2R_{f2} + 1)} \qquad (11)$$

Figure 8 shows the gain frequency response of the integrator by two cascaded amplifiers with a single pole based on the RC values as R_{f1}=470kΩ,R_{f2}=300kΩ, R_{i1}=53.2 kΩ, R_{i2}=3 kΩ and C_1=470 pF, C_2=235 pF.

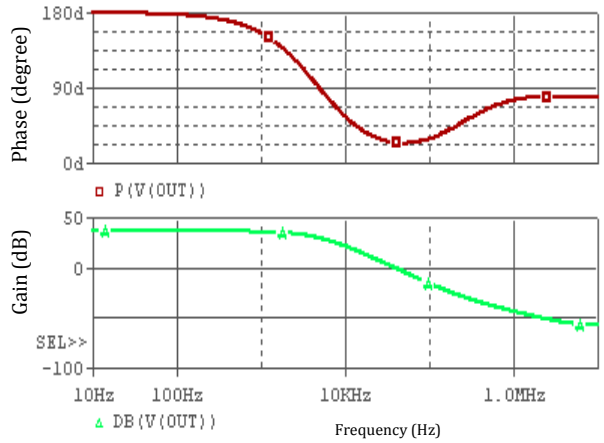

Figure 8: Frequency responses of a 2nd-order integrator by two cascaded amplifiers with a single pole.

Here we see that the integrator by two cascaded amplifiers with a single pole achieves an audio band gain of 46 dB at DC. Subsequently the gain is doubled.

3. Analysis and Comparison of Simulation Results

We have simulated the 2nd-oder closed-loop CDA in Figure 2 for a single amplifier with two poles in the feedback loop and a gain boosting (Figure 5) and two cascaded amplifiers with a single pole in feedback loop (Figure 7).

Figure 9 shows the THD of a single amplifier with two poles (THD2) and the gain boosting (THD3) and at two cascaded amplifiers with a single pole feedback loop CDAs (THD1) based on PSPICE simulation.

In Figure 9, we note that THD improves by as much as 2 times when the2nd-order integrator by two cascaded amplifiers with a single poleis used. For the integrator based on the RC values as R_{f1}=470kΩ, R_{f2}=300kΩ, R_{i1}=53.2kΩ, R_{i2}=3kΩ and C_1=470pF, C_2=235 pF, the THD for input frequency between 1 kHz to 10 kHz is less than 0.5%. The THD of the CDA is improved much better by integrating two cascaded amplifiers with a single pole in comparison to that of the CDA by gain boosting. As expected, the THD increases at higher frequency because the loop gain of the CDA decreases at higher frequency due to the 40dB/dec roll-off at the cut-off frequency. This method can be easily realized since the resistor and capacitors of the integrator are realized externally.

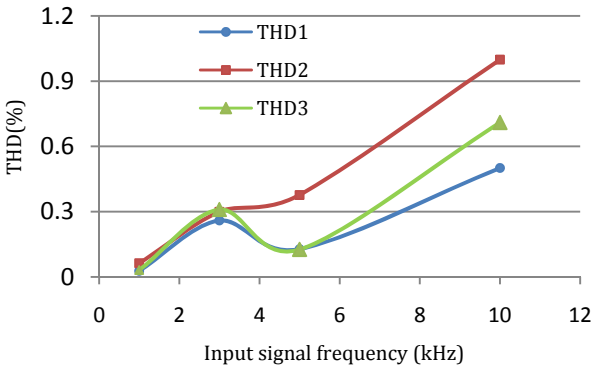

Figure 9: THD against frequency in the single amplifier with two poles, two cascaded amplifiers and a single pole with M=.5.

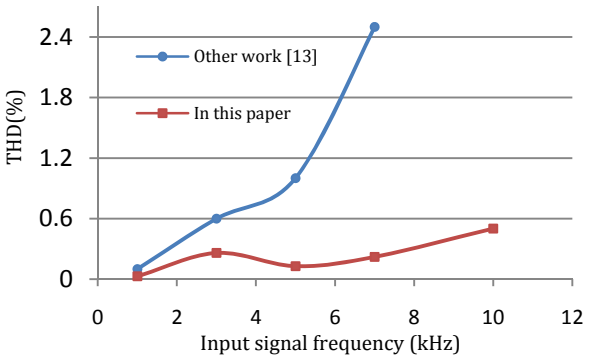

Figure 10: THD vs. frequency.

Figure 10, compares our results for THD against input frequency with other work [13]. The input

frequency in our work ranges from 1 kHz to 10 kHz whereas in [13] it is in the range 1 kHz to 7 kHz.

In Figure 10, we show the THD in this paper compared to [13] improved by as much as 11 times.

4. CONCLUSIONS

We have investigated the parameters affecting THD and THD in a PWM Class D Amplifiers with feedback. We have shown through mathematical analysis and simulation how the THD of a Class D Amplifier with feedback can be improved by increasing the gain of the integrator. We have also shown how the gain of the integrator can be further increased by means of two cascaded amplifiers with a single pole. Simulations show that the THD of a Class D amplifier by gain boosting is improved by as much as 1.4 times. The THD of the Class D amplifier with feedback can be improved by as much as 2 times by means of two cascaded amplifiers with a single pole. When compared to [13], the THD in this paper is improved by as much as 11 times.

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BIOGRAPHIES

Parviz Amiri was born in 1970. He received the B.Sc. degree from University of Mazandaranin 1994, the M.Sc. from Khajeh Nasir Toosi University (KNTU Tehran, Iran) in1997, and his Ph.D. from University of Tarbiat Modares (TMU Tehran, Iran) in 2010, all degrees in Electrical Engineering (Electronics). His main research interest includes electronic circuit design in industries. His primary research interest is in RF and power electronic circuits, with focus on high efficient and high linear power circuit design. He is currently with the Faculty of Electrical and Computer Engineering at Shahid Rajaee Teacher Training University in Tehran, Iran.

Mostafa Kohestani was born in Tehran, Iran, in 1986. He received the M.Sc. degree in electrical engineering from Zarande University of Technology, Saveh, Tehran, in 2009. His current interests are in the development of high-efficiency switching amplifiers.

Mahmood Seifouri received the B.Sc. (Hons) and Ph.D. degrees in electrical and electronic engineering from the University of Wales College of Cardiff, UK, in 1985 and 1989, respectively. After spending two years as a lecturer at Brighton University, UK, Dr. Seifouri moved to Iran University of Science and Technology in 1991. After spending 9 years at IUST, in 2000, he was employed as a Senior Development Engineer at Bookham Technology, UK, where he was primarily involved in research & development projects in the field of optoelectronics. In September 2001, he joined Optometric, CA, USA, as a Senior Development Engineer and continued with his work over there. Since 2006, Dr. Seifouri has been with the Faculty of Electrical and Computer Engineering, Shahid Rajaee Teacher Training University, Tehran, Iran. His research interests include experimental and numerical studies of electromagnetic fields and waves with particular emphasis on the theory, modeling and simulation of optical waveguides, lasers, amplifiers and nano-scale photonic circuits.