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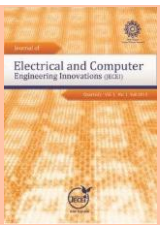

A New Low Power High Reliability Flip-Flop Robust Against Process Variations

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ABSTRACT

Low scaling technology makes a significant reduction in dimension and supply voltage, and leads to new challenges about power consumption such as increasing nodes sensitivity over radiation-induced soft errors in VLSI circuits. In this area, different design methods have been proposed for low power flip-flops and various research studies have been done to reach a suitable hardened flip-flops. In this paper, we combine these two generally separate addressed issues to reach a new low power high reliability flip-flop (LP-HRFF). LP-HRFF operates over 1GHz clock frequency and is structured based on an appropriate combination of dual interlocked storage cell, level converting techniques and clock signal controlled gates. The extensive simulations exhibit LP-HRFF has 0% single event upset rate against single transient events occurred on inputs and internal nodes and show the improvement of power consumption up to 42.8% and power delay product up to 24.6% compared with its counterparts. Furthermore, the simulation results approve the robustness and efficacy of the proposed flip-flop against process variations.

1. INTRODUCTION

Nowadays high reliability and low power considerations are amongst important issues in VLSI design process. Alpha particles from packaging and bonding, neutrons from cosmic rays and radiation-induced transient faults are three important sources of transient faults [1]. A single event upset (SEU) occurs in the case of a transient fault happens in a combinational circuit node and spreads through a storage cell, or on condition that a single event transient (SET) directly strikes to a storage cell and upsets its logical value [2].

Flip-flops are known as an important storage elements distributed in digital designs. To increase the resiliency of flip-flops against soft errors, several techniques have been introduced in previous researches such as dual and triple modular redundancy (TMR) [3], dual interlocked storage cell (DICE) [4], and SEU hardened flip-flop [5]. Some of these techniques consider power consumption improvements in their designs.

On the other hand, different approaches have been proposed in previous studies to decrease power consumption in flip-flop designs. Adaptive coupling technique [6], conditional charging and discharging technique [7], [8] and level converting technique [9] are some of the most recently important methods. Level converting technique is one of the best methods for power consumption reduction in which noncritical path blocks contrary to critical paths blocks utilize low supply voltage to balance between speed and power.

In this paper, we propose a low power-high resilience flip-flop robust against process variation, called LP-HRFF, without any SEU against single event transient and with considerable power optimization compared with recently reported hardened and low power-hardened flip-flops.

The rest of this paper is organized as follows. Section 2 reviews previously mentioned hardened by design (HBD) flip-flops and low power-hardened flip-flops. We introduce the principle of the proposed LP-HRFF operation in Section 3. Section 4 exhibits the simulation results of the proposed flip-flop and proves its superiority through comparative results. We show the robustness and efficacy of the proposed LP-HRFF over process variations in Section 5. Finally, we conclude the paper in Section 6.

2. Brief Review on Previous HBD and Low Power-Hardened Flip-Flops

In this section, we describe some important HBD and low power-hardened flip-flop structures, which are the best, recently reported in more details.

Fig. 1, shows clocked precharge SEU hardened flip-flop (CPSH) [10], which includes an input transfer stage, a soft error robust storage latch and an output stage. A clocked transistor stack in input transfer stage passes data to the latch. In CPSH, soft error robust storage cell has four internal nodes, each node is driven by a couple of NMOS and PMOS transistors. Y_1 and Y_3 nodes store data whilst Y_0 and Y_2 nodes store their complement. Unlike an inverter, the gates of driver transistors are joined to two different nodes. Data is transferred through input stage by turning M_2 and M_3 on when clk is low and clkb is high. Whenever clk becomes high, data is moved in two directions to the latch. Finally, the stored value is appeared on output stage.

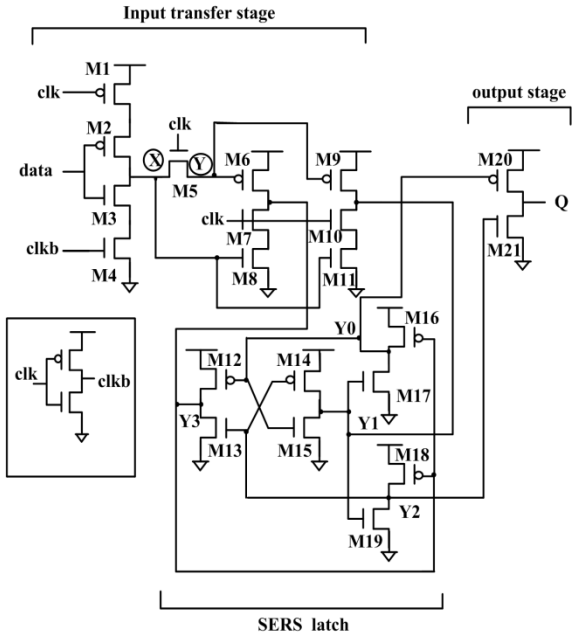

Figure 1: CPSH flip-flop [10].

Fig. 2, shows bistable cross-coupled dual modular redundancy adaptive coupling (BCDMR-AC) flip-flop [3] which includes adaptive coupling flip-flops [6] in a bistable cross coupled dual modular redundancy structure to produce a low power and high reliable flip-flop. An adaptive coupling flip-flop operates with a single-phase clocking scheme using pass transistors and in comparison with conventional master slave latch, it reduces power consumption by eliminating local clock buffers. BCDMR structure consists of two pairs of master-slave latches, two c-elements and one keeper. If one of two latches is flipped by a temporal soft error, the c-element operates and the keeper reserves the previous value and the upset latch recovers when the next clock is injected to the flip-flop.

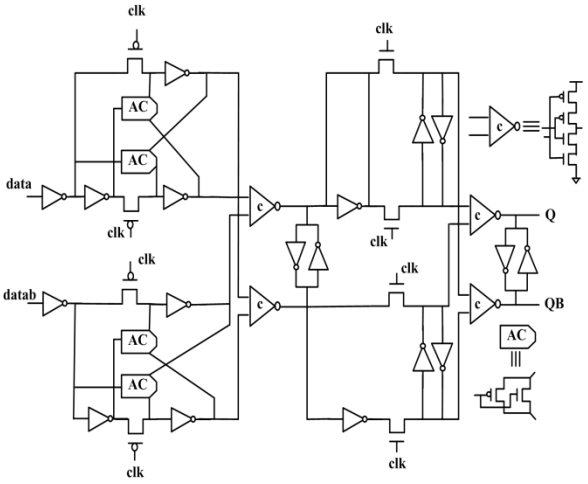

Figure 2: BCDMR-AC flip-flop [3].

True single-phase clock (TSPC)-DICE flip-flop [4], which consists of a TSPC input stage, the SEU hardened DICE latch, and a c-element output stage is shown in Fig. 3. M_{18} is an equalizer transistor, which works in conjunction with input stage to make possible writing operation into the DICE latch when the clock is in rising edge. For a stored data value of 1 in the flip-flop, the voltages at internal nodes A, B, C, and D are 1, 0, 1, and 0 respectively. For a stored data value of 0, the node voltages are the opposite. When clk is low, node X is precharged to the complement of the data while node Y is precharged to 1. Consequently, M_7 and M_8 are off, leaving node B at a logic value is determined by the DICE latch. When clk becomes 1, DICE latch achieves data in two states. If the data is 1 and (clk =1), node X will be 0 and node Y remains at 1, which pulls down node B and turns M_{18} on. A low impedance path through M_{18} then pulls down node D and changes the voltages at nodes A and C from 0 to 1, which is the same as the input data. On the other hand, if the data is 0 and (clk =1), node X will be 1 and node Y is pulled down to 0.

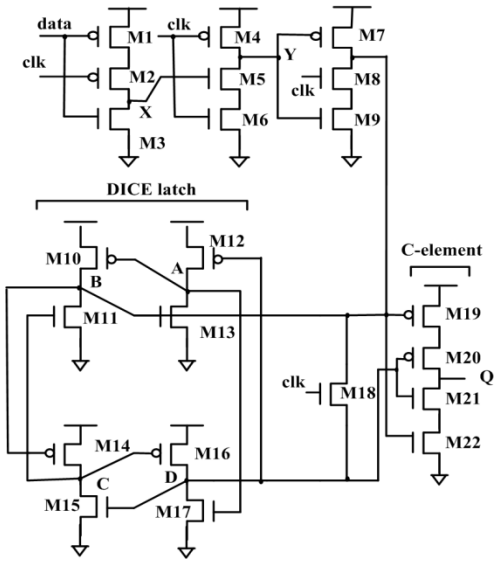

Figure 3: TSPC-DICE flip-flop [4].

Fig. 4, shows a D type SEU hardened edge triggered flip-flop [5], the filp-flop consists of 12T storage cell. When the clk is low, the input clocked stage will be active, if data and output opposite. If clk and Q are low, and if data is high, transistors M_1-M_3 are on and charge node X to V_{DD}. With the rising edge of clk signal, nodes IN_0 and IN_2 discharge to low, resulting high Q. If data is low, transistors M_4-M_6 are on and discharge node X to ground. With the rising edge of clk signal, nodes IN_0 and IN_2 charge to V_{DD}, resulting low logic at the output. Two similar potential nodes IN_0 and IN_2 drive the output c-element buffer.

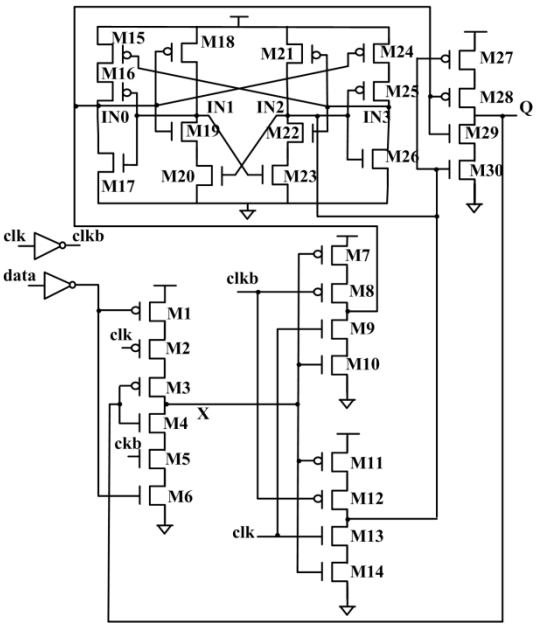

Figure 4: SEU hardened flip-flop [5].

As it can be seen in Fig. 5, Conditional Pass Quatro (CPQ) flip-flop [11] consists of three stages, namely an input transfer unit with a delay element, a soft error robust Quatro latch, and an output stage. The delay element opens a small transparent window between clock (Clk) and its delayed complement (Clkb) signal, to pass the data and its complement to write the data to the Quatro latch. An equalizer transistor M7 works in conjunction with the input stage to enable writing into the Quatro latch at the rising edge of the *Clk* signal. For a stored data value of 1 in the flip-flop, the voltage at internal nodes A, B, C, and D are 0, 1, 0, and 1, respectively. For a stored value of 0, the node voltages are opposite. There are three minimum sized inverter delays between Clk and Clkb signals, generating a narrow time window at the transfer unit to pass logic 1, or 0 data to the output.

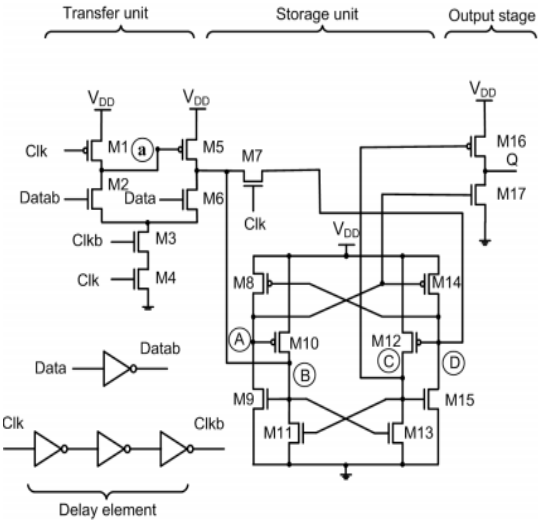

Figure 5: CPQ flip-flop [11].

3. THE PRINCIPLE OF THE PROPOSED LP-HRFF OPERATION

As it can be seen in Fig. 6 (a), the proposed low power and hardened flip-flop, consists of three basic stages which are input low power transfer stage, hardened latch stage and output resilient stage. Input transfer stage includes two transmission gates controlled by clkb and clkbn signals. Fig. 6 (b) demonstrates the logical diagram of the pulse generator that works in a low supply voltage, and Fig. 6 (c) indicates its transistor level circuit design. When data and Q vary, the NOR gate transistors sense the clk transitions and produce clkbn and clkb. When clkb is high, data and its complement enter to the second stage that is a robust DICE latch. DICE storage cell has eight transistors, includes four storage nodes (A, B, C and D) which combat SEU by their feedback loops. The third stage is composed of two c-elements to harden the internal DICE storage nodes against SET and two back-to-back inverters to preserve the flip-flop output.

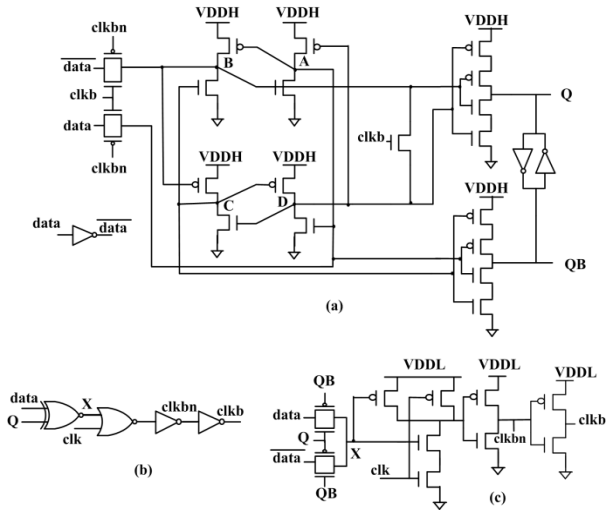

Figure 6: (a) The proposed LP-HRFF, (b) low supply voltage pulse generator circuit in logical level and; (c) in transistor level.

4. The LP-HRFF Simulation Results and Comparison

The testbench of the proposed LP-HRFF loaded by four inverters is shown in Fig.7. The input signals are generated through input buffers to be more realistic and the output load capacitor of flip-flop is 20 fF. The simulation results are provided from Hspice in a PTM 45 nm CMOS technology (PTM is an evolution of previous Berkeley Predictive Technology Model (BPTM) which provides the novel features for robust design exploration toward the 10nm regime)[12], at room temperature (27 ˚C), 1 GHz clock frequency, 1 V for high supply voltage and .8 V for low supply voltage.

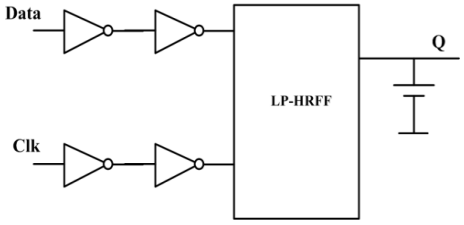

Figure 7: The simulation applied testbench.

A. *Resiliency against soft error*

To investigate the proposed flip-flop resiliency over cosmic radiation and comparison, we suppose a single event transient fault strikes to the most sensitive node. Each fault is modeled by a time varying double exponential current pulse [13]. In this model, current curve I (t) is given by (1).

$$I(t) = I_0\left(\exp\left(-t/\tau_\alpha\right) - \exp\left(-t/\tau_\beta\right)\right) \quad (1)$$

where I_0 is the charge injected current occurred by the particle strike, τ_α is the junction collection time constant and τ_β is a time constant, which identifies initially establishing ion track. To simulate resiliency, we apply a 1 to 0 and a 0 to 1 SET to the sensitive node C (Fig. 6,) of our testbench structure. To model SET, we consider a current source according to equation (1) with τα and τβ respectively equal to 164 ps and 50 ps, such as performed in [14]. Fig. 8 shows the signal waveforms of the proposed flip-flop under SET injections. According to the waveforms, the internal nodes of DICE cell recover both transient faults, thus the output node is totally fault free. The quantity of hardening for the under test flip-flops is reported in Table 1. As shown in the table 1, the proposed flip-flop, BCDMR-AC flip-flop, TSPC-DICE and SEU hardened flip-flop are fully hardened whereas CPSH and CPQ flip flops outputs are upset by 2.6 fc and 4.7 fc critical charges. Moreover, among fully hardened flip-flops, LP-HRFF has an acceptable number of transistors with better performance in comparison with other flip-flops that we will demonstrate it in the next part.

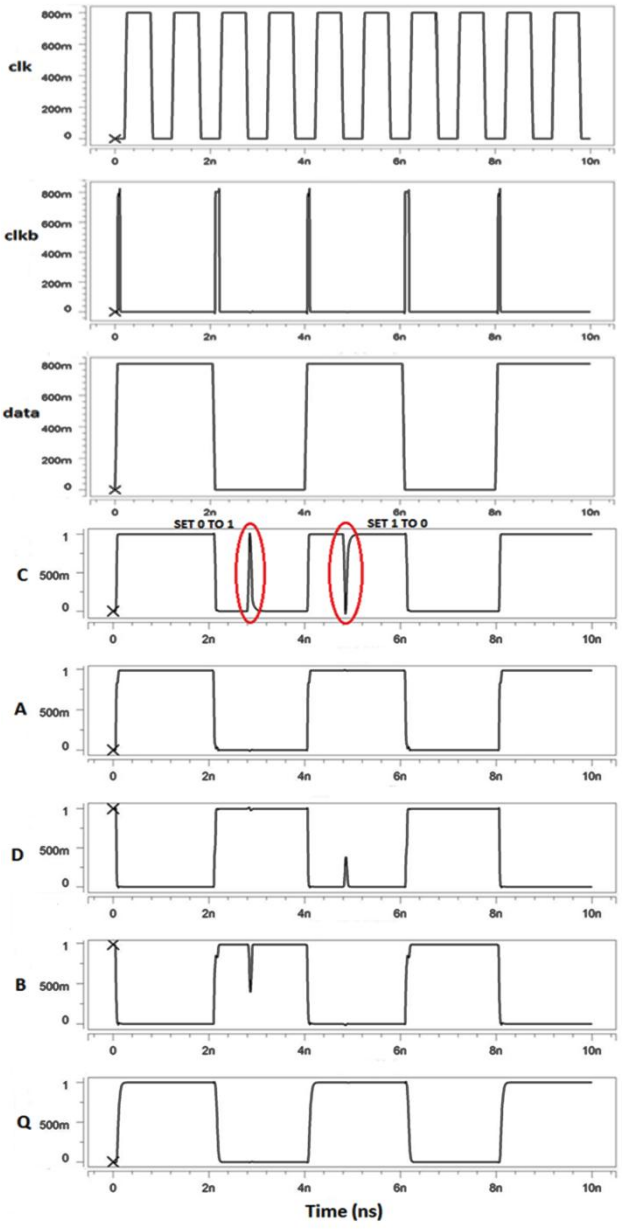

Figure 8: Waveforms of the proposed flip flop and SEU injection at node C.

TABLE 1
THE QUANTITY OF HARDING AND NUMBER OF TRANSISTORS

Types of flip-flop	Proposed flip-flop	BCDMR-ACFF [3]	TSPC-DICE [4]	CPSH [10]	SEU hardened FF[5]	CPQFF [11]
Critical charge for upset	fully hardened	fully hardened	fully hardened	2.6	fully hardened	4.7
Number of transistors	39	70	22	23	34	25

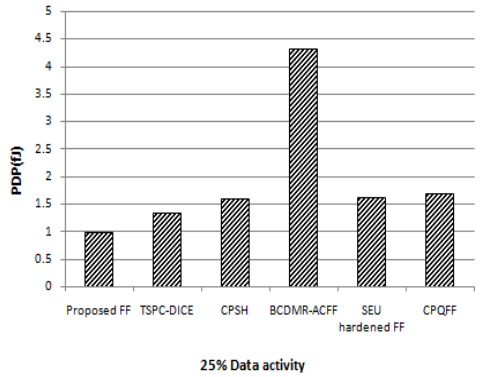

Figure 9: The comparison of power delay product for 25% data switching activity.

B. Delay, Power and PDP merits

To compare the performance of the proposed LP-HRFF with its counterparts, we simulated under consideration that flip-flops are in the testbench structure of Fig. 7 and measured performance merits. Table 2 depicts minimum data to Q delay parameter, power consumption and PDP comparison in 25% data activity. The data to Q delay is obtained by sweeping the low to high and high to low data transition times with respect to the clock edge, minimum data to output delay defines optimum setup time.

As can be seen in the results of Table 2, our proposed flip-flop has the lowest power consumption because of applying level converting technique in its structure and also because of generating the clock pulse by altering input data, which lowers the power consumption of clock production. Fig. 9 shows the comparison of power delay product (PDP) as a trade-off between power and delay of the proposed LP-HRFF and its counterparts. The comparison results show LP-HRFF has 77.2%, 34.6%, 24.6%, 38.7% and 41.3% PDP improvement compared with BCDMR-ACFF, CPSH, TSPC-DICE, SEU hardened flip-flop and CPQFF respectively.

TABLE 2
THE COMPARISON OF DELAY, POWER AND PDP

Types of flip-flop	Proposed flip-flop	BCDMR-ACFF [3]	Tspc-DICE [4]	CPSH [10]	SEU hardened FF[5]	CPQ flip-flop [11]
T_{setup} (ps)	-26.2	41	6.2	12.5	13.9	12.02
Min D to Q delay (ps)	88.4	143.3	68.9	54.8	54.6	56.9
Power (25% activity) (μW)	11.1	30.1	19.5	28.9	29.6	29.5
PDP (25% activity) (fJ)	0.98	4.3	1.3	1.5	1.6	1.7

Fig. 10 compares the power consumptions of under test flip-flops over different data switching activities that approves superiority of the proposed LP-HRFF to BCDMR-ACFF, TSPC-DICE, CPSH and SEU hardened flip-flop up to 50% switching activities.

5. THE ROBUSTNESS OF LP-HRFF AGAINST PROCESS VARIATIONS

Environmental variations including temperature and V_{DD} affect on circuit performance. On the other hand, in CMOS technology processing variations on transistor sizing, the thickness of oxide and V_{th} lead to fast and slow transistors. In the point of design view, a superior circuit design has to provide good results in all process corners. Thus, in this section, we compare our LP-HRFF with its counterparts to approve its robustness against environmental variations and process variations.

To investigate environmental effects, we consider ±10% variation in low and high supply voltages and the range of -40 °C to 85 °C variation on temperature.

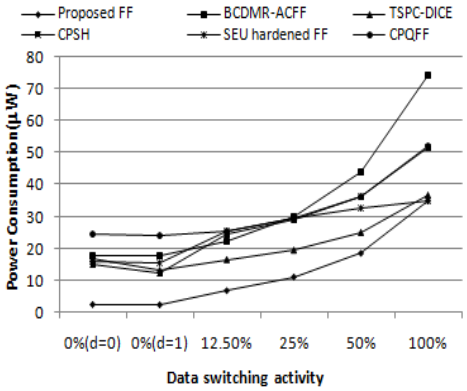

Figure 10: Power consumption versus different data switching activities.

The results which are presented in Fig. 11, demonstrate the power consumption of flip-flops considering power supply variations. We consider from 0.9 V to 1.1 V for high power supply. Low power supply corresponding to high power supply varies from 0.7 V to 0.9 V. The results show the power consumption of our proposed flip-flop is always less than other flip-flops in various supply voltages.

Fig. 12, shows the minimum data to Q delay of LP-HRFF versus temperature in the range of -40°C to 85°C and for three different VDDs including 0.9 V, 1 V and 1.1 V. As shown in Fig. 12, the minimum data to Q delay follows the same decreasing rate in the different supply voltages.

Min data to Q delay is obtained under the supply voltage variation. Then, PDP is obtained from contusion power consumption and Min data to Q delay.

Fig. 13, compares the PDP in various supply voltage values and 25% switching activity for all flip-flops under test and shows LP-HRFF achieves the lowest PDP in different situations.

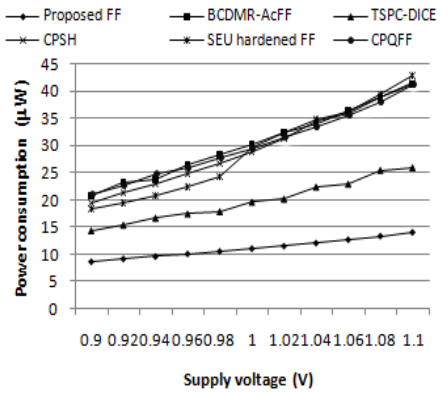

Figure 11: Power consumption versus different supply voltages.

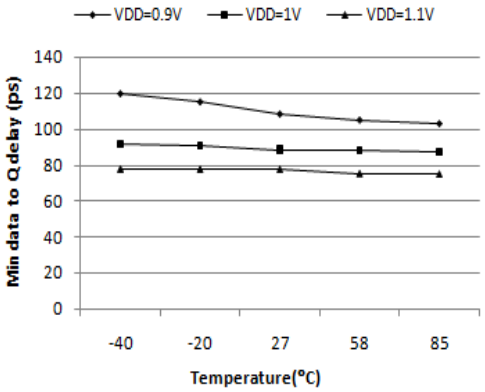

Figure 12: Minimum data-to-Q delay versus temperature in different voltages.

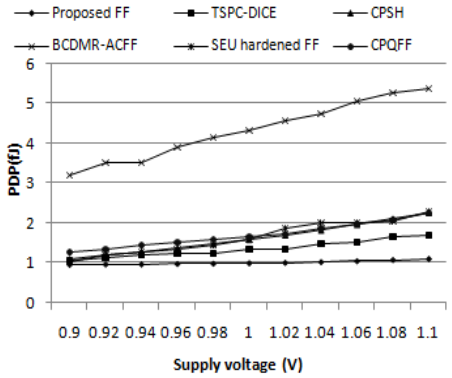

Figure 13: PDP versus different supply voltages.

For similar designed devices, there are various mismatches during the manufacturing of digital integrated circuits. These mismatches occurred as small variations on some design parameters such as length and width of transistors. Analytical investigation of individual variation and their combination effects on the behavior of circuit is almost impossible. The Monte-carlo simulation can consider a large set of circuit instantiates considering randomly varied parameters to analyze the circuit behavior under the combination of different mismatches [15]. To study the effect of length and width variation on the performance of our proposed flip-flop, we consider Monte-carlo analysis with a normal distribution by 10% variation on transistor sizes through 1000 times simulation. Fig. 14, shows the mean value of PDP results for under test flop-flops induced by transistors sizing alterations and approves the robustness of results against process variations. Furthermore, the results confirm that our proposed LP-HRFF has the best power delay product amongst its counterparts.

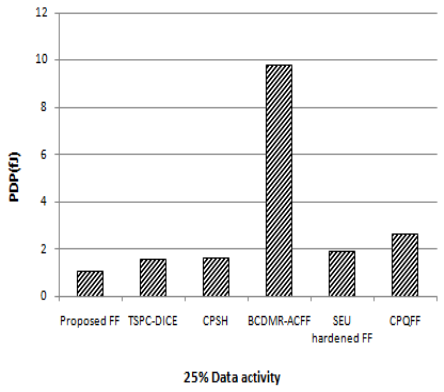

Figure 14: PDP comparison obtained from Monte-carlo analysis.

As we said before, processing variations affect the performance of the circuit.

All of these variations can be got together in the transistor model file which is the basis of the simulator operation. NMOS and PMOS transistors have fast, slow and typical model file in each technology. Fig. 15, shows all process corners for NMOS and PMOS transistors.

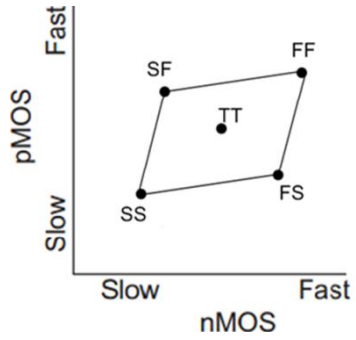

Figure 15: Process corners [16].

In order to explore the efficiency of LP-HRFF, it is essential to measure its power and PDP in process corners.

The power consumption and PDP are calculated at 1 GHZ clock frequency in TT, FF, SS, FS and SF process corners.

Fig. 16, and 17 depict the simulation results of power consumption and PDP respectively in 25% data switching activity. As shown in the Figures 16 and 17, the proposed LP-HRFF has the lowest value in different process corners in all graphs that approve the efficiency of the proposed flip-flop against process corners. Layout of the flip-flops, are drawn based on the design rules for the CMOS technology and shown in Fig. 18.

The layout area of each flip-flop is reported in the Table 3. The results of this table show the proposed LP-HRFF has area improvement in comparison with BCDMR-ACFF. Moreover, between fully hardened other flip-flops, LP-HRFF has an acceptable area with better performance in comparison with other flip-flops.

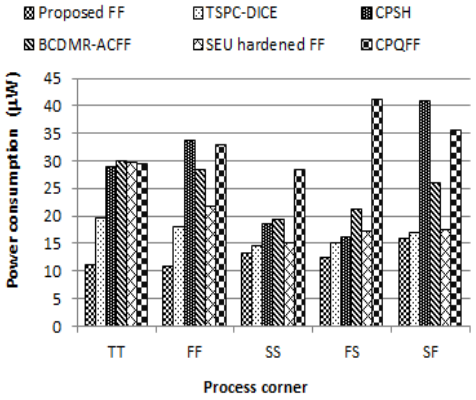

Figure 16: Power consumption comparison at process corners.

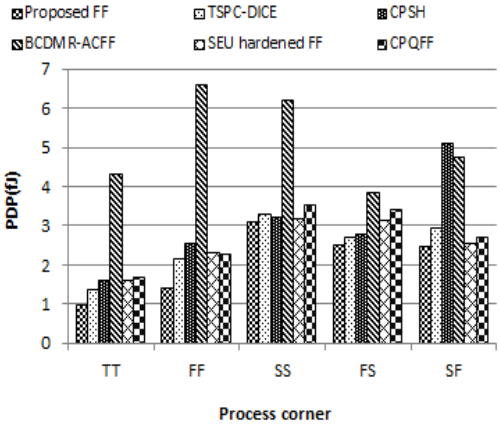

Figure 17: PDP comparison at process corners.

6. Conclusion

In this paper, we proposed a soft error perfect resilience flip-flop, suitable organized based on level converting, input gate controlling techniques, and DICE latch.

The simulation results showed the proposed LP-HRFF is fully hardened against SETs and in comparison with its counterparts, including DICE-TSPC, CPSH, SEU hardened flip-flop, CPQFF and BCDMR-ACFF, reduces power consumption from 42.8% to 63% and improves PDP from 24.6% to 77.2% in 25% data activity.

Moreover, the simulation results demonstrate the proposed flip-flop preserves its robustness and high performance against process variations.

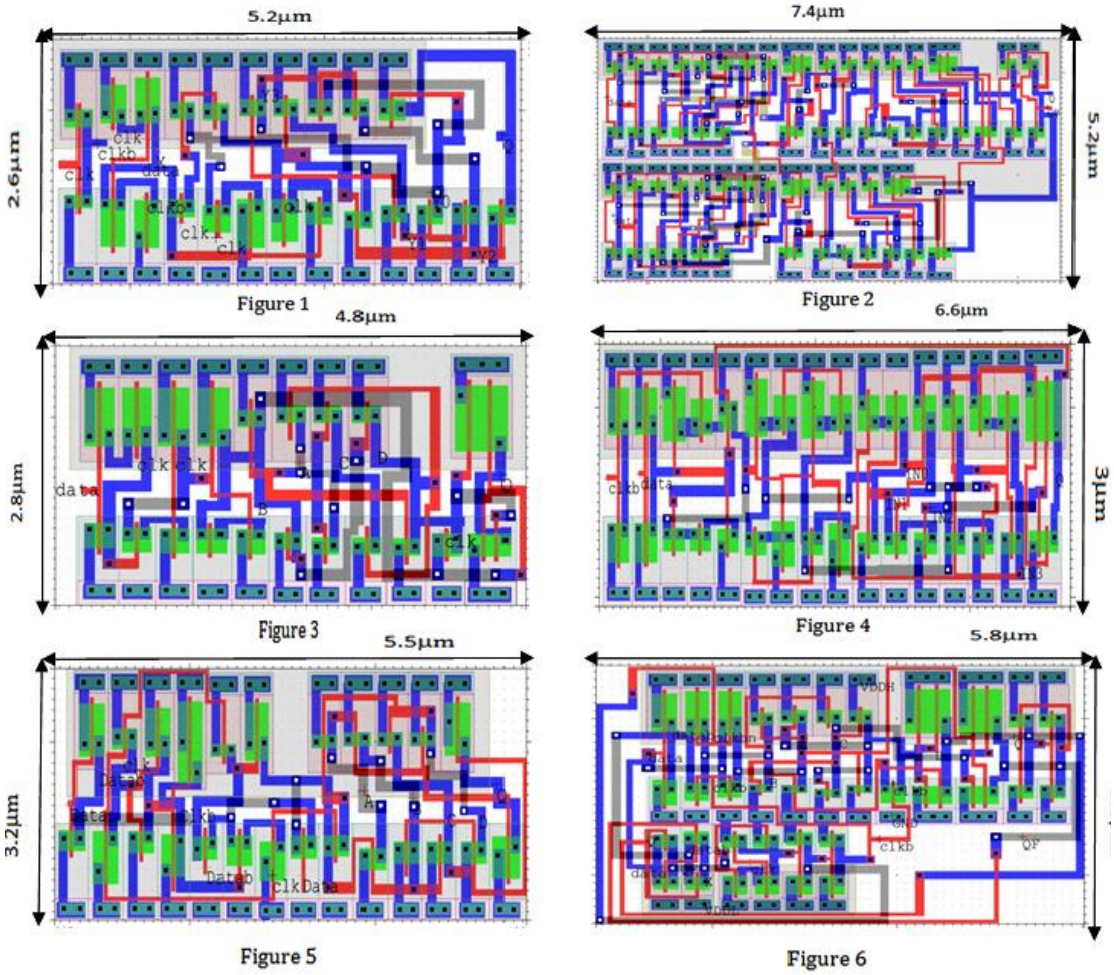

Figure 18: Flip-Flops layouts in CMOS technology.

TABLE 3
FLIP-FLOPS LAYOUT AREA

Types of flip-flop	Proposed flip-flop	BCDMR-ACFF [3]	TSPC-DICE [4]	CPSH [10]	SEU hardened FF[5]	CPQF F [11]
Width	5.8	7.4	4.8	5.2	6.6	5.5
Height	3.6	5.2	2.8	2.6	3	3.2
Layout area (μm^2)	20.8	38.4	13.4	13.5	19.8	17.6

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