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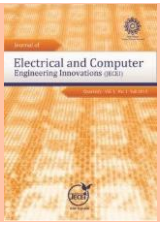

A 12 bit 76MS/s SAR ADC with a Capacitor Merged Technique in 0.18µm CMOS Technology

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ABSTRACT

In this paper, a new high-resolution and high-speed fully differential Successive Approximation Register (SAR) Analog to Digital Converter (ADC) based on capacitor merged technique is presented. The main goal of the proposed idea is to achieve high-resolution and high-speed SAR ADC, simultaneously. It is noteworthy that, exerting the suggested method, the total capacitance and the ratio of the MSB and LSB capacitors are decreased; as a result, the speed and accuracy of the ADC are increased reliably. Therefore, applying the proposed idea, it is reliable that to attain a 12-bit resolution ADC at 76MS/s sampling rate. Furthermore, the power consumption of the proposed ADC is 694µW with the power supply of 1.8 volts correspondingly. The proposed post-layout SAR ADC structure is simulated in all process corner conditions and different temperatures of -50°C to +50°C, and performed using the HSPICE BSIM3 model of a 0.18µm CMOS technology.

1. Introduction

The charge redistribution successive approximation register (SAR) ADC has been a popular candidate among all the different types of ADC due to advantages such as low power consumption, switching feature, no need for precision residue amplification and being more amenable to CMOS process scaling than the other ADC architectures [1, 2, 3, 33]. Switched-capacitor SAR ADCs with high resolution are becoming widely used. Conventionally, a large capacitor array is necessary to keep a low capacitor mismatch, hence improved linearity. However, this demands large input capacitance values and causes considerable reference buffer driving power [4, 10, 11, 23, 34]. To achieve high resolution, a large total capacitance is used to suppress the distortion caused by the capacitor mismatch [2, 9, 11, 14]. However, the large capacitance introduces high power consumption for both ADC input and reference buffers. Several techniques have been proposed for avoiding the use of the large capacitance in C-DACs. Capacitor calibration techniques have been proposed for compensating the capacitor mismatch in the foreground or background [10, 16, 18]. The SAR structure is relatively simple and does not require a high-gain, linear amplifier, and an important characteristic when considering the nanometer scale processes often used for these ADCs [5, 14, 15]. It is also important to consider process node and supply voltage when considering ADC architectures. In addition to scaling well with decreasing process geometry, the SAR architecture is naturally more responsive to low supply voltages than the other medium- or high-resolution Nyquist ADC architectures [5, 6, 11, 19]. Also, a SAR ADC does not require linear signal swing anywhere other than at its input, this is in difference to the other architectures, such as pipeline ADCs, which require high-linearity, high-swing amplifier where the signal range can be truly rail-to-rail. As the supply voltage is reduced, the headroom required for these amplifiers typically remains unchanged; therefore, the available signal swing shrinks and degrades SNR [5, 6, 18]. A SAR ADC can be

implemented in either fully-differential topology. It is clear that, a fully-differential topology has its advantages, namely, better distortion performance, better common-mode noise rejection, and increased output voltage swing [7, 19]. Meanwhile, segmented-capacitor structure is also introduced to alleviate this problem while introducing a non-binary coupling capacitor [12, 13, 16]. This non-binary capacitor causes some bottlenecks on layout and mismatch performance. Thus, it is significant to introduce an improved segmented capacitor array avoiding the non-binary- weighted capacitor [7, 8, 11, 18]. However, the mismatching of binary weighted-capacitor network and the parasitic capacitors on each side of the coupling capacitor have great effect on the achievable resolution which has not yet been analyzed in precise theory [8].

On the other hand, C-2C DAC technique is another choice to achieve high speed and moderate resolution [22, 25]. It is noteworthy that, a C-2C DAC has three major benefits compared to its binary weighted counterpart [29, 34]. Firstly, the DAC size increases linearly with the resolution. Secondly, the capacitive input loading is fixed, usually a few unit capacitors, and independent of the resolution on the first order, as a result the bandwidth is larger. Thirdly, the loading at each middle node inside the DAC is fixed, and making the DAC faster and the switch design easier as well [22, 24, 25, 26, 34]. Therefore, SAR ADCs with C-2C DAC have the potential to achieve wider bandwidths and higher speeds though occupying less area. Conversely, the parasitic capacitance problem in the C-2C DAC causes a severe accuracy limitation and it is hard to achieve high resolutions with this topology [25, 26, 29, 34].

This paper focuses on how a differential SAR ADC can be designed to achieve high- resolution, high-speed and very low power in the 0.18µm CMOS process without using any calibration technique. In order to enhance the resolution and reduce the number of unit capacitors in the conventional capacitance DAC, and to increase the speed of the system simultaneously, a novel capacitor merged technique is presented in this paper. The proposed paper is organized as follows. In Section 2 the proposed fully differential SAR ADC is discussed. Section 3 describes the circuit implementation. Post-layout simulation results are presented in Section 4, and finally, section 5 concludes the paper.

2. The Proposed Fully Differential SAR ADC

The main building blocks of a typical fully differential SAR ADC structure is shown in Figure 1.

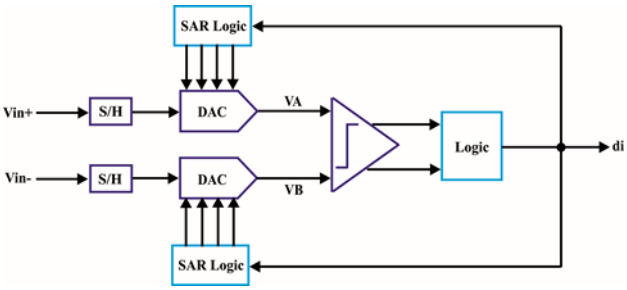

Figure 1: A general block diagram of the fully differential SAR ADC.

Generally, the SAR ADC based on capacitor DAC contains the comparator, the SAR registers and the digital to analog converter basically. The SAR architecture uses powerful binary search algorithms with DAC capacitor array and SAR registers approximating the input signals, while the comparator takes decisions on the approximated inputs. The decision made is used to approximate inputs further, and this process continues until the entire digital code is obtained. The SAR ADC operation is serial by nature, and it requires at least 'n' clock cycles to produce an output, where 'n' represents the number of bits of resolution of the ADC [3, 14, 16, 18, 30, 31, 33]. The proposed fully differential SAR ADC architecture is shown in Figure 2.

The main purposes of the proposed idea are to achieve a high-resolution and high- speed SAR ADC simultaneously. For this case, a new capacitor merged technique is applied in this paper, which the first 7bits (LSB bits) and the last 5bits (MSB bits) are employed C-2C and Binary-Weighted Capacitive DAC technique, respectively. It is noticeable that, applying this technique the total capacitance and the ratio of the MSB and LSB capacitors are decreased extremely, as a result the speed and the accuracy of the system are increased as well. Meanwhile, the effect of the parasitic capacitors in the internal nodes of C-2C DAC are negligible, because as it is clear in Figure 2 the C-2C DAC technique is applied just on LSB bits. On the other hand, since both 5 MSB and 7 LSB bits are connected to each other through the coupling capacitor, in order to improve the accuracy of the system and decrease the mismatch effect of the both sides of two DAC arrays, the size of the coupling capacitor (Cc) is considered 2C reliably.

The conversion process is basically divided into two phases. During the first (sampling) phase, the bottom plates of the capacitors are connected to the corresponding positive or negative input signal (Vin+ or Vin-) while the inputs of the comparator are connected to the common–mode voltage (Vcm).

Therefore, the capacitors are charged with the input signal.

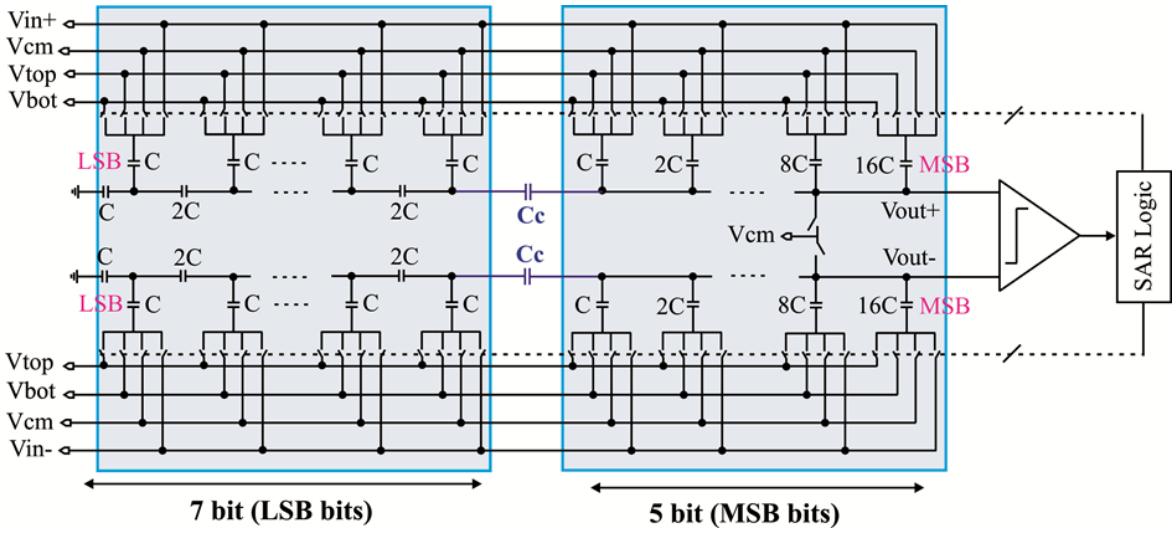

Figure 2: The proposed fully differential SAR ADC architecture.

On the other hand, after the sampling phase, in the first conversion cycle the bottom plates of the capacitors are disconnected from input signals and connected to the Vcm, in order to determine the reference voltage of each capacitor block, the sign of the sampled input voltage is decided, also the inputs of the comparator are disconnected from Vcm. In the next conversion cycles, the bottom plates of the capacitors are connected to either of the maximum or minimum reference voltages (Vtop or Vbot) or Vcm, according to the binary word from the control logic which performs a successive approximation binary search. As a result of charge conversion at each of comparator input nodes, their voltage would be the output of the DAC minus the corresponding input signal. Reliably, 4-bit numeral example is presented in order to clarify the operation of the proposed ADC as well. The voltage sources of the ADC are supposed to as follows; Vin+=2.4V, Vin-=1.6V, Vtop=2.5V, Vbot=1.5V, Vcm=2V and Vcmin=2V. Where Vin+ and Vin-, and Vtop and Vbot are the positive and negative input voltages, and maximum and minimum reference voltages respectively. Also, Vcm and Vcmin are the common-mode voltage. During the sample mode, the inputs are being sampled on all the capacitors and during the hold mode, all the switches are connected to Vcmin which are depicted in Figure 3 and Figure 4 correspondingly. The charges sampled in the capacitors during the sample mode have to be equal to the charges held on the capacitors during the hold mode owing to the law of charge conservation, and the value of the first bit is "1" as clearly exposed in (1). Meanwhile, through the bit cycling action, the comparator compares V_A and V_B. If V_A is bigger than V_B, the comparator outputs a decision bit 1. Otherwise, the comparator outputs a decision bit -1. Generally, as Figure 5 shows starting with the most significant bit, if the decision is 1, the capacitors labe-

-led 2C will switch to Vtop and Vbot at the positive and negative sides of the DAC respectively, and the rest of the capacitors are connected to Vcmin at the both sides of the DAC which the value of the second bit is "1" equally represented in (2) as well. Also, the next conversion of the 4-bit SAR ADC are illustrated in (3) and Figure 6, clearly. As a result, VB is increased by the first binary weight, and VA is reduced by the first binary weight in the first cycle.

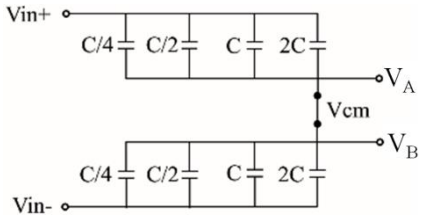

Figure 3: During the sample mode of 4bit SAR ADC.

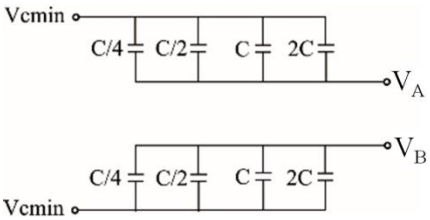

Figure 4: During the hold mode of 4bit SAR ADC.

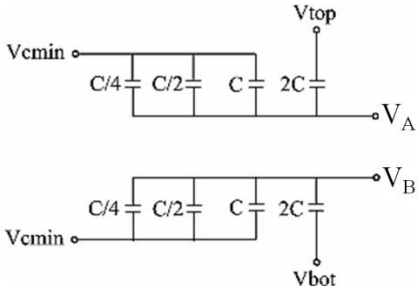

Figure 5: During the bit cycling action of 4bit SAR ADC.

$$
\left.\begin{aligned}
&[(\mathrm{V_{top}}-\mathrm{V_A})-(\mathrm{V_{in+}}-\mathrm{V_{cm}})].(2+1+1/2)\mathrm{C}=0\\
&\Rightarrow -(\underbrace{\mathrm{V_A}-\mathrm{V_{cm}}}_{\delta_{v+}})(15/4)\mathrm{C}-(\mathrm{V_{in+}}-\mathrm{V_{cmin}}).(15/4)\mathrm{C}=0\\
&\Rightarrow \delta_{v+}=-(\mathrm{V_{in+}}-\mathrm{V_{cmin}})\\
&\Rightarrow \delta_{v-}=-(\mathrm{V_{in-}}-\mathrm{V_{cmin}})\\
&\Rightarrow \delta_{v}=\delta_{v+}-\delta_{v-}=-(\mathrm{V_{in+}}-\mathrm{V_{in-}})\\
&\Rightarrow \delta_{v}=\delta_{v+}-\delta_{v-}=-(2.6-1.6)=-0.8 \Rrightarrow \mathbf{Bit1}=\mathbf{1}
\end{aligned}\right\} \quad (1)
$$

$$
\left.\begin{aligned}
&[(V_{top}-V_A)-(V_{in+}-V_{cm})].2C+[(V_{cmin}-V_A)-(V_{in+}-V_{cm})].(1+1/2+1/4)C=0\\
&\Rightarrow 2V_{top}-2V_A-2V_{in+}+2V_{cm}+\left(\frac{7}{4}\right).V_{cm}-\left(\frac{7}{4}\right).V_A-\left(\frac{7}{4}\right).V_{in+}+\left(\frac{7}{4}\right).V_{cmin}=0\\
&\Rightarrow -\left(\underbrace{V_A-V_{cm}}_{\delta_{v+}}\right).\left(\frac{15}{4}\right)C-\left(\frac{15}{4}\right).V_{in+}+\left(\frac{7}{4}\right).V_{cmin}+2.V_{top}=0\\
&\Rightarrow \delta_{v+}=-V_{in+}+\left(\frac{8}{15}\right).V_{top}+\left(\frac{7}{15}\right).V_{cm}\\
&\Rightarrow \delta_{v-}=-V_{in-}+\left(\frac{8}{15}\right).V_{bot}+\left(\frac{7}{15}\right).V_{cm}\\
&\Rightarrow \delta_{v}=\delta_{v+}-\delta_{v-}=-[(V_{in+}-V_{in-})+(8/15).(V_{top}-V_{bot}]\\
&\Rightarrow \delta_{v}=\delta_{v+}-\delta_{v-}=-(-0.8+0.53)=-0.267 \Rrightarrow \mathbf{Bit2}=\mathbf{1}
\end{aligned}\right\} \quad (2)
$$

$$
\left.\begin{aligned}
&[(\mathrm{V_{top}}-\mathrm{V_A})-(\mathrm{V_{in+}}-\mathrm{V_{cm}})].(3.5)\mathrm{C}+[(\mathrm{_{cmin}}-\mathrm{V_A})-(\mathrm{V_{in+}}-\mathrm{V_{cm}})].(1/4)\mathrm{C}=0\\
&\Rightarrow 3\mathrm{V_{top}}-3\mathrm{V_A}-3\mathrm{V_{in+}}+3\mathrm{V_{cm}}+\left(\frac{3}{4}\right).\mathrm{V_{cm}}-\left(\frac{3}{4}\right).\mathrm{V_A}-\left(\frac{3}{4}\right).\mathrm{V_{in+}}+\left(\frac{3}{4}\right).\mathrm{V_{cm}}=0\\
&\Rightarrow -\left(\underbrace{\mathrm{V_A}-\mathrm{V_{cm}}}_{\delta_{v+}}\right).\left(\frac{15}{4}\right)\mathrm{C}-\left(\frac{15}{4}\right).\mathrm{V_{in+}}+\left(\frac{3}{4}\right).\mathrm{V_{cmin}}+3\mathrm{V_{top}}=0\\
&\Rightarrow \delta_{v+}=-\mathrm{V_{in+}}+\left(\frac{12}{15}\right).\mathrm{V_{top}}+\left(\frac{3}{15}\right).\mathrm{V_{cm}}\\
&\Rightarrow \delta_{v-}=-\mathrm{V_{in-}}+\left(\frac{12}{15}\right).\mathrm{V_{bot}}+\left(\frac{3}{15}\right).\mathrm{V_{cm}}\\
&\Rightarrow \delta_{v}=\delta_{v+}-\delta_{v-}=-[(\mathrm{V_{in+}}-\mathrm{V_{in-}})+(12/15).(\mathrm{V_{top}}-\mathrm{V_{bot}}]\\
&\Rightarrow \delta_{v}=\delta_{v+}-\delta_{v-}=-(-0.8+0.8)=0 \Rrightarrow \mathbf{Bit3}=?
\end{aligned}\right\} \quad (3)
$$

$$
\begin{aligned}
&[(V_{top}-V_A)-(V_{in+}-V_{cm})].(3)C+[(V_{cmin}-V_A)-(V_{in+}-V_{cm})].(3/4)C=0\\
&\Rightarrow -\left(\underbrace{V_A-V_{cm}}_{\delta_{v+}}\right).\left(\frac{15}{4}\right)C-\left(\frac{15}{4}\right).V_{in+}+\left(\frac{1}{4}\right).V_{cmin}+\left(\frac{7}{4}\right).V_{top}=0\\
&\Rightarrow \delta_{v+}=-V_{in+}+\left(\frac{14}{15}\right).V_{top}+\left(\frac{1}{15}\right).V_{cm}\\
&\Rightarrow \delta_{v-}=-V_{in-}+\left(\frac{14}{15}\right).V_{bot}+\left(\frac{1}{15}\right).V_{cm}\\
&\Rightarrow \delta_v=\delta_{v+}-\delta_{v-}=-[(V_{in+}-V_{in-})+(14/15).(V_{top}-V_{bot}]\\
&\Rightarrow \delta_v=\delta_{v+}-\delta_{v-}=-(-0.8+0.93)=+0.13 \Rrightarrow \mathbf{Bit4=0}
\end{aligned}
\tag{4}
$$

$$
\begin{aligned}
&[(V_{top}-V_A)-(V_{in+}-V_{cm})].(3)C+[(V_{bot}-V_A)-(V_{in+}-V_{cm})].(1/2)C+\\
&[(V_{cm}-V_A)-(V_{in+}-V_{cm})].(1/4)C=0\\
&\Rightarrow -\left(\underbrace{V_A-V_{cm}}_{\delta_{v+}}\right).\left(\frac{15}{4}\right)C-\left(\frac{15}{4}\right).V_{in+}+\left(\frac{1}{4}\right).V_{cmin}+3.V_{top}+\left(\frac{1}{2}\right).V_{bot}=0\\
&\Rightarrow \delta_{v+}=-V_{in+}+\left(\frac{12}{15}\right).V_{top}+\left(\frac{4}{30}\right).V_{bot}+\left(\frac{1}{15}\right).V_{cm}\\
&\Rightarrow \delta_{v-}=-V_{in-}+\left(\frac{12}{15}\right).V_{bot}+\left(\frac{4}{30}\right).V_{top}+\left(\frac{1}{15}\right).V_{cm}\\
&\Rightarrow \delta_v=\delta_{v+}-\delta_{v-}=-[(V_{in+}-V_{in-})+(12/15).(V_{top}-V_{bot}]+\left(\frac{4}{30}\right).(V_{bot}-V_{bot})\\
&\Rightarrow \delta_v=\delta_{v+}-\delta_{v-}=-(-0.8+0.8-0.13)=-0.13 \Rrightarrow \mathbf{Bit4=1}
\end{aligned}
\tag{5}
$$

It is noteworthy that in (3), the value of the third bit is undefined (neither "1" nor "0"), because the output voltage difference (δ_v) is 0 volts. For this case, in order to clear the value of the fourth bit, first time value of the third bit is supposed to be "1" which is shown in Figure 7, as it is clear in (4), in this time the value of the fourth bit is achieved "0" as well . Otherwise, if the value of the third bit is supposed to be "0" which is shown in Figure 8, the value of the fourth bit is attained as "1" that is exposed in (5) conspicuously.

3. Circuit Implementation

A. Digital to Analog Converter (DAC)

The DAC producing the analog voltage is one of the most significant sub-blocks which dominate the statistic linearity [3,9]. Basically, for a high resolution SAR ADC, high linearity capacitor array is necessary to assure that the switching voltage is binary weighting [16]. It is noticeably that, for each additional bit, the numbers of the capacitors rise exponentially and the area of capacitor array increases and hence the capacitance will become larger. Also, it will increase the switching power, capacitor switching time and input capacitive loading [3, 14, 16, 18, and 31]. To avoid these problems a novel merged capacitor DAC is presented in this paper. Figure 9 indicates the proposed fully differential 12 bit DAC structure. As it is clear in Figure 9, in the proposed idea, the 5 MSB and 7 LSB bits are implemented with Binary-Weighted Capacitive and C-2C DAC technique respectively. The key motivations of this idea are reduced the total capacitive and increased the speed of the DAC as well. In the proposed structure, in order to reduce the total capacitance and to increase the speed, just 7 LSB bits are implemented with the C-2C DAC technique, because as discussed above, C-2C DAC is not the good choice for high-resolution circuits.

It is notable that, a 7-bit conventional binary-weighted capacitor DAC requires 128 unit capacitors, which is a large sum that is difficult to accomplish with

high yield at this nascent stage of process development. While, a 7-bit C-2C DAC only requires 20 unit capacitors which is a quantity easier to fabricate with high yield, and the value of the unit capacitor (C) is considered 62.5fF. In the proposed DAC structure, another considerable significant point is the coupling capacitor size. Since both 5 MSB and 7 LSB bits are connected to each other through the coupling capacitor. To improve the accuracy of the system and decrease the mismatch effect of both sides of two DAC arrays, the size of the coupling capacitor (Cc) is chosen 2C. Likewise, the common-centroid layout technique is utilized. Meanwhile, to ensure that all unit capacitors in the capacitor array have the same structure a dummy capacitor ring is also used on the edges of the capacitor array around them. So, by applying this method it is credible that to achieve high resolution and high speed ADC properly.

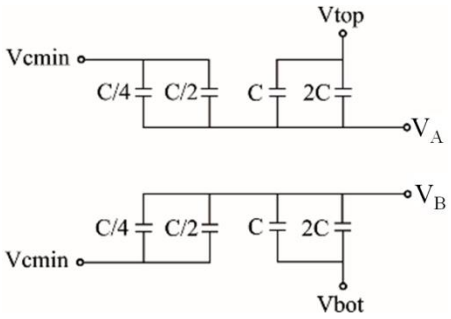

Figure 6: During the bit cycling action of 3bit SAR ADC.

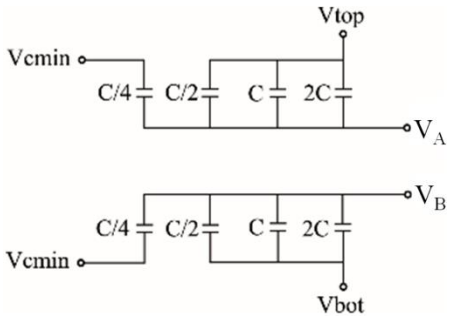

Figure 7: During the bit cycling action of 4bit SAR ADC.

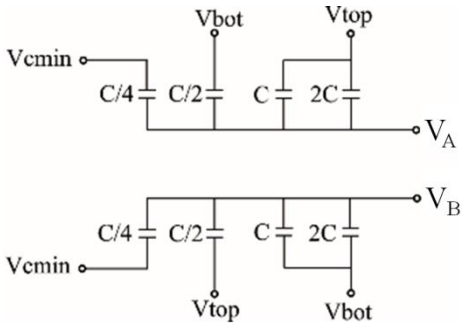

Figure 8: During the bit cycling action of 4bit SAR ADC.

B. Comparator

The schematic of the proposed comparator circuit is illustrated in Figure 10. This comparator is composed of one pre-amplifier stage and latch stage. Fundamentally, in a switched-capacitor latch comparator, other than thermal noise, the main sources of errors are comparator offset, clock feedthrough, and kick-back noise [20, 28, 30]. In a SAR ADC, the comparator offset, normally constant, can be tolerated, since it results in an offset in the ADC I/O transfer curve that can easily be tolerated [30]. However, the other two errors must be minimized. It is clear that clock feedthrough and kick-back noise are generated at the edge of the comparator clock and the edge of the comparator input signal, respectively [21, 27, 28, 30, 31]. A basic solution is to use a preamplifier that reduces the input- referred effects of these errors. However, this noticeably increases the comparator power consumption [20, 32]. Generally, the pre-amplifier is used to amplify the input signal and block the kickback noise [28, 31]. Although the output signal of the pre-amplifier is larger than the input signal, it is not large enough to drive the digital circuitry, due to that a latch stage is required to create the full range signal at the output nodes of the comparator basically [20, 28-32]. The input signals (Vin+, Vin-) are applied to the gate terminals of the M1 and M2.

Then, the amplified signals of AA and BB nodes are employed to the gate terminals of the M7 and M8 correspondingly to generate full range signals at the output nodes (out+, out-) as well. Meanwhile, M3 - M4 and M5-M6 are utilized positive and negative feedback respectively. Also, the transistors M9-M12 play function of the latch stage to produce full range signal. Finally, M13, M14 and the reset switch are used to short the output nodes to speed up the next comparison of the comparator. It is conspicuous that, the transistors M13 and M14 are utilized to short the output nodes (out+, out-) with low distortion and low clock skew as well, instead of using one switch between the output nodes. For this case, the inverse reset clock (Resetcb) is applied to the gate terminals of M13 and M14. Meanwhile, M0 and M01 are the current sources of the proposed comparator structure.

4. Simulation Results

In this section, the simulation results of the proposed fully differential SAR ADC are presented.

The output FFT spectrum of the proposed ADC is represented in Figure 11, as it is clear in the mentioned figure, the output THD is less than -72dB by applying a 38.38MHz sinusoidal input frequency at 76MS/s sampling rate as well.

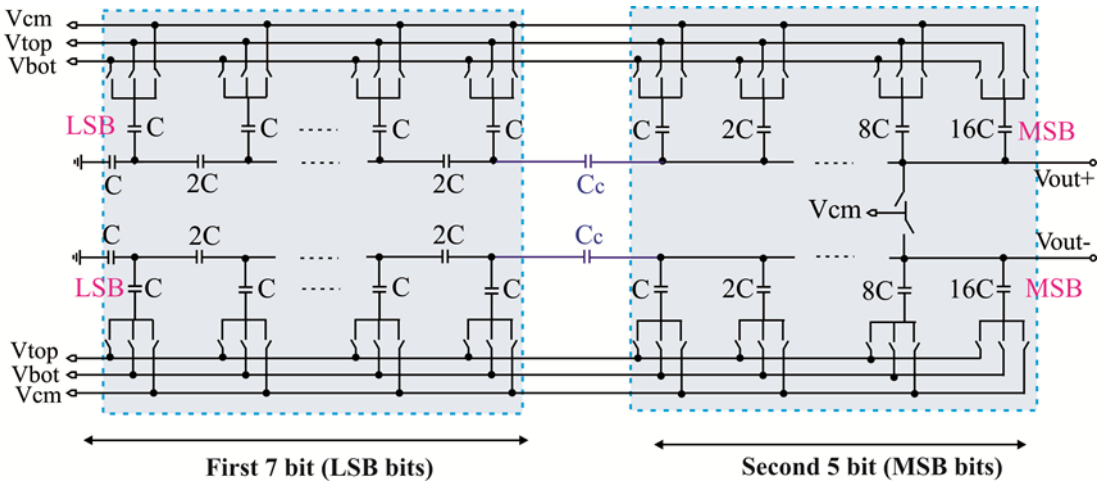

Figure 9: A 12 fully differential capacitor DAC.

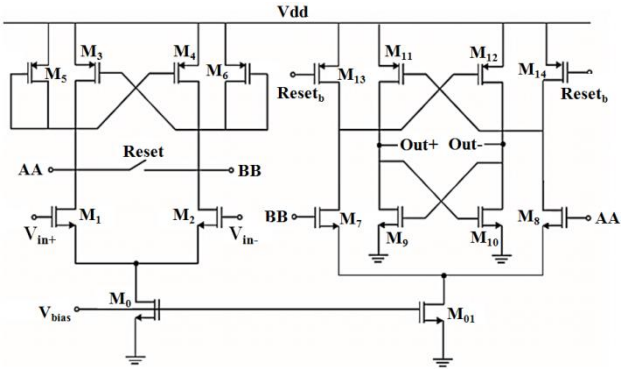

Figure 10: The proposed comparator structure.

Meanwhile, Figure12 shows the Multi tone output FFT spectrum of the proposed ADC in f_{in}=18.76MHz, 19MHz, 19.38MHz, and 19.68MHz at f_S=76MS/s. Post-layout simulation results of the proposed ADC are stated in Figures 13 and 14, respectively. The temperature dependency of the SNDR and SFDR are depicted in Figure 15, while the SNDR and SFDR variations between -50°C to 50°C were less than 1.2dB and 2.1dB correspondingly. Meanwhile, 500 times Monte-Carlo simulation results of the behavioral model of the suggested design are shown in Figure 16 (parasitic capacitance included). Capacitor mismatch is $\partial_{mismatch} = 1.5\%$, also both reference noise and comparator noise errors are $\partial_{noise} = 0.25V$. As it is clear in figure 16, labeled (A) and (B), show the SNDR and SFDR of the proposed ADC respectively. It can be seen that the worst and the best SNDR and SFDR are about 64.4dB and 73.3dB, 76.1dB and 87.2dB respectively. Figure 17 labeled (C) and (D) summarizes the simulation results of the SNDR and SFDR versus different process corners with a Nyquist rate (38.42MHz) input, at the sampling rate 76MS/s, it validate that the SNDR and SFDR of the proposed architecture are no less than 67dB and 78dB in all process corners as well. Finally, the layout of the proposed 12 bit SAR ADC is indicated in figure 18.

The total power consumption of the suggested ADC is 694µW with the power supply of 1.8 volts. Also, the figure-of-merit (FOM) parameter used to a standard the ADC is shown in (6).

$$FOM = \frac{Ptotal}{2^{ENOB} * fS} \quad (6)$$

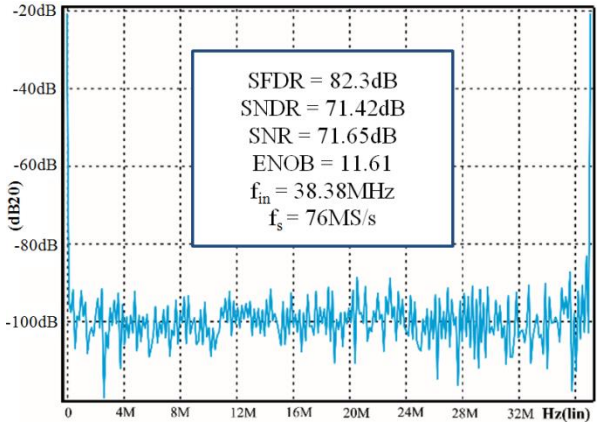

Figure 11: The output FFT spectrum of the proposed ADC in f_{in}=38.38MHz at f_S=76MS/s.

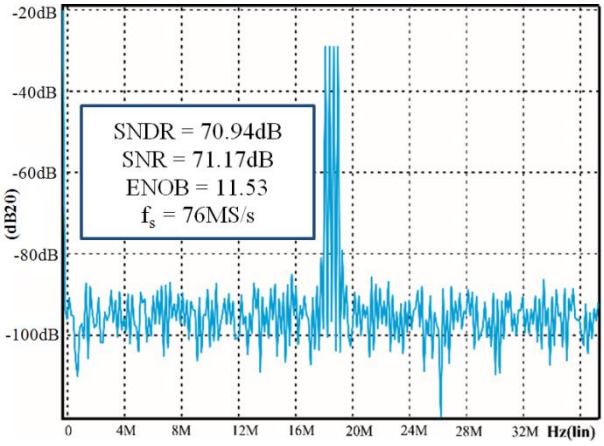

Figure 12: Multi tone output FFT spectrum of the proposed ADC in f_{in}=18.76MHz, 19MHz, 19.38MHz, and 19.68MHz at f_S=76MS/s.

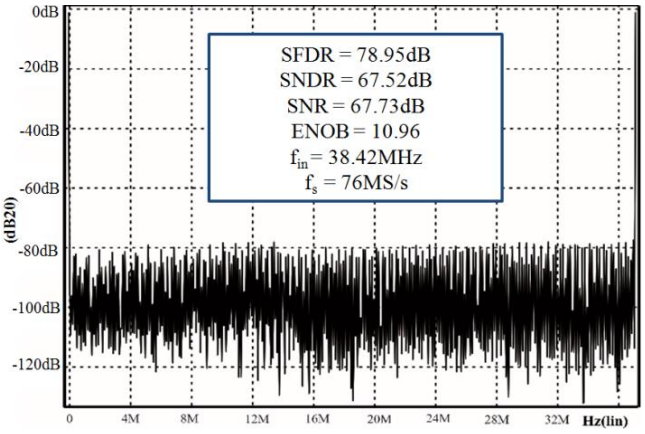

Figure 13: The post-layout simulation result output FFT spectrum of the proposed ADC with a Nyquist rate (38.42MHz) input at f_S=76MS/s.

where Ptotal, ENOB, and fS are the total power consumption, the effective number of bits, and the Nyquist sampling frequency, respectively. The FOM calculated using (6) is 2.88fJ per conversion step. Post-layout simulations are performed for all corner conditions using the BSIM3 model of a 0.18µm CMOS process with the power supply of 1.8 volts.

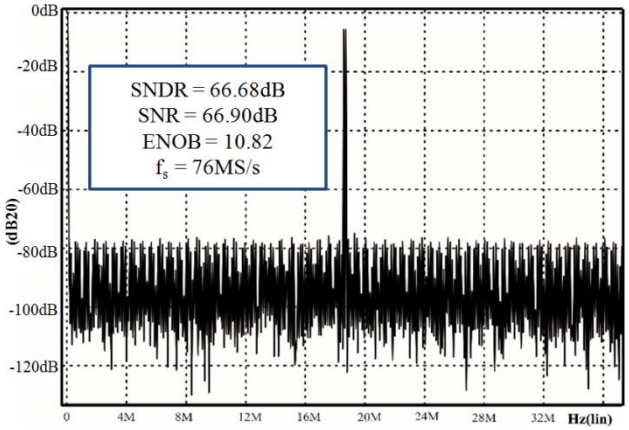

Figure 14: The post-layout double tone simulation result output FFT spectrum of the proposed ADC in f_{in}=19.15MHz and 19.19MHz at f_S=76MS/s.

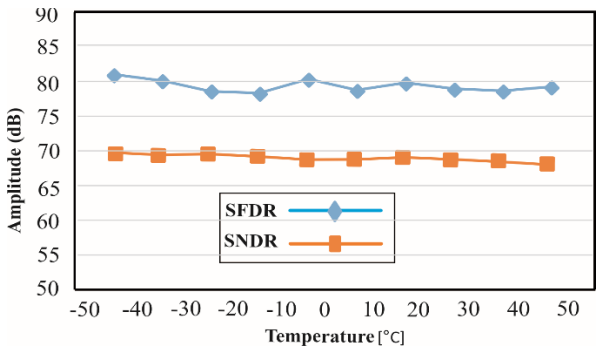

Figure 15: Post-layout simulation results of SNDR and SFDR versus temperature with a Nyquist rate (38.42MHz) input at f_S=76MS/s.

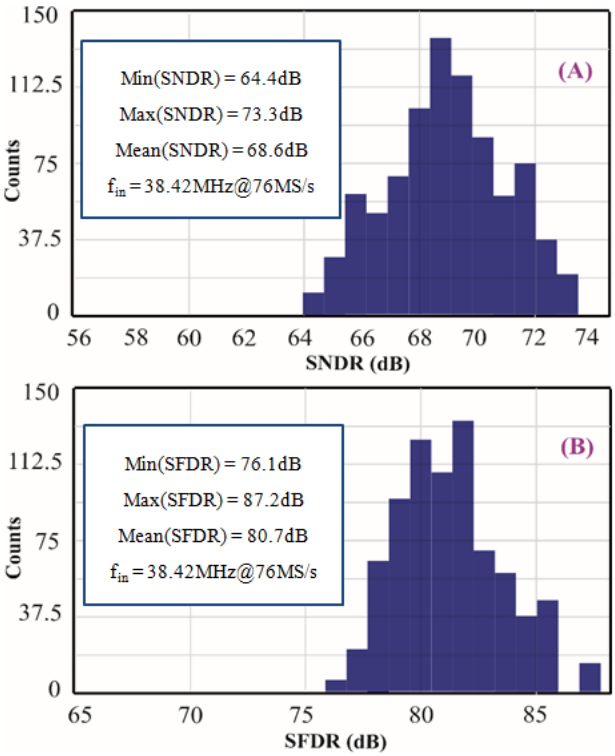

Figure 16: 500 Monte-Carlo SNDR (labeled (A)) and SFDR (labeled (B)) simulation results of the proposed ADC in f_{in}=38.42MHz at f_S=76MS/s.

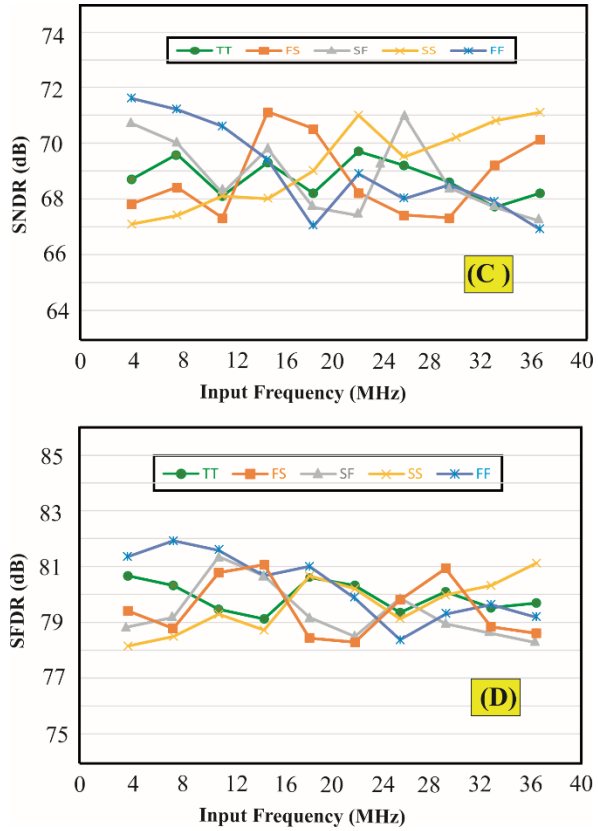

Figure 17: All process corners (TT, FS, SF, SS and FF) SNDR (labeled (C)) and SFDR (labeled (D)) simulation results of the proposed ADC in f_{in}=38.42MHz at f_S=76MS/s.

5. Conclusion

In this paper, a new fully differential SAR-ADC based on capacitor merged technique was presented. The main purpose of the proposed idea is achieving high-resolution and high-speed SAR ADC. By exerting the suggested method, the total capacitance and the ratio of the MSB and LSB capacitor was decreased, as a result, the speed and accuracy of the ADC were reliably increased. Therefore, applying the proposed idea, it is reliable that to attain a 12-bit resolution SAR ADC at 76MS/s (sampling rate). Furthermore, at the 1.8V supply voltage and 76MS/s sampling rate with a Nyquist input frequency, the ADC achieves an SNDR and SFDR of 67.52dB and 78.95dB, respectively.

The power consumption of the proposed ADC is 694µW with the power supply of 1.8 volts. In addition, the resultant FOM of the proposed ADC is 2.88fJ per conversion step. Finally, Table 1 compares the specifications of the proposed SAR ADC with the other similar works. Post-layout simulation results was performed using the HSPICE BSIM3 model of a 0.18µm CMOS technology, as shown in Fig. 18.

Table 1
Comparison Table

Ref.	[5]	[12]	[13]	This work
Technology (µm)	0.18	0.18	0.18	0.18
Resolution (bits)	12	12	12	12
Sampling Rate (MS/s)	5	0.2	0.5	76
Supply Voltage (V)	1.8	2.8	1.4	1.8
Power Consumption (µW)	490	1160	91	694
FOM(fJ/Conv-Step)	57.2	-	-	2.88

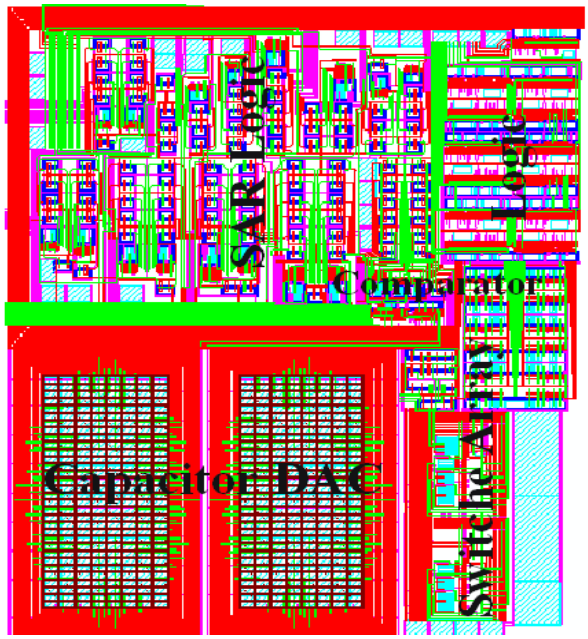

Figure 18: The layout of the proposed SAR AD.

References

[1] S. Liu, Y. Shen, and Z. Zhu, "A 12-bit 10 MS/s SAR ADC with high linearity and energy-efficient switching," *IEEE Transactions on Circuits and Systems*, vol. 63, no. 10, pp. 1616 – 1627, 2016.

[2] C. Liu, M. Huang, and Y. H. Tu, "A 12 bit 100 MS/s SAR-assisted digital-slope ADC," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2941-2950, 2016.

[3] Kh. Hadidi, "Data converter course notes," Urmia University, Urmia, Iran, 2005.

[4] Y. Chung, M. Wu, and H. Li, "A 12-bit 8.47-fJ/conversion-step capacitor-swapping SAR ADC in 110-nm CMOS," *IEEE Transactions on Circuits and Systems*, vol. 62, no. 1, pp. 10-18, 2015.

[5] Y. Chung, M. Wu, and H. Li, "A 14b 80 MS/s SAR ADC with 73.6 dB SNDR in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3059-3066, 2013.

[6] Y. Song, Z. Xue, Y. Shiquan Fan, and L. Geng, "A 0.6-V 10-bit 200-kS/s fully differential SAR ADC with incremental converting algorithm for energy efficient applications," *IEEE Transactions on Circuits and System*, vol. 63, no. 4, pp. 449-458, 2016.

[7] Y. Tao and Y. Lian, "A 0.8-V, 1-MS/s, 10-bit SAR ADC for multi-channel neural recording," *IEEE Transactions on Circuits and Systems*, vol. 62, no. 2, pp. 366-375, 2015.

[8] S. Lei, D. Qinyuan, L. Chuangchuan, and Q. Gaoshuai, "Analysis on capacitor mismatch and parasitic capacitors effect of improved segmented-capacitor array in SAR ADC," in *Proc. Third International Symposium on Intelligent Information Technology Application*, vol. 2, pp. 280-283, Shanghai, China, 2009.

[9] J. Wen, P. Hung Chang, J. Huang, and W. Lai, "Chip design of a 12-bit 5MS/s fully differential SAR ADC with resistor- capacitor array DAC technique for wireless application," in *Proc. IEEE International Conference on Signal Processing, Communications and Computing* (ICSPCC), pp. 1-4, Ningbo, China, 2015.

[10] W. Lai, J. Huang, C. Hsieh, and F. Kao, "An 8-bit 2 MS/s successive approximation register analog-to-digital converter for bioinformatics and computational biology Application," IEEE 12th International Conference on Networking, Sensing and Control (ICNSC), pp. 576-579, Taipei, Taiwan, 2015.

[11] W. Lai, J. Huang, T. Ye, and C.W. Shih "Integrated successive approximation register analog-to-digital converter for healthcare systems applications," in *Proc. 12th IEEE International Conference on Solid-State and Integrated Circuit Technology* (ICSICT), pp. 1-3, Guilin, China, 2014.

[12] W. Lai, J. Huang, and W. Lin "1MS/s low power successive approximations register ADC for 67-fJ/conversion-step," in *Proc. 2012 IEEE Asia Pacific Conference on Circuits and Systems*, pp. 260-263, Kaohsiung, Taiwan, 2012.

[13] P. Lee, J. Lin, and C. Hsieh, "A 0.4 V 1.94 fJ/conversion-step 10 bit 750 kS/s SAR ADC with input-range-adaptive switching," *IEEE Transactions on Circuits and Systems*, vol. 63, no. 12, pp. 2149-2157, 2016.

[14] M. Kim, Y. Kim, Y. Kwak, and G. Ahn, "A 12-bit 200-kS/s SAR ADC with hybrid RC DAC," in *Proc. 2014 IEEE Asia Pacific Conference on Circuits and Systems* (APCCAS), pp. 185-188, Ishigaki, Japan, 2014.

[15] S. Wong, U. Chio, Y. Zhu, S. Sin, S. Pan U, and R. Paulo Martins, "A 2.3 mW 10-bit 170 MS/s two-step binary-search assisted time-interleaved SAR ADC," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 8, pp. 1783-1794, 2014.

[16] M. Yoshioka, K. Ishikawa, T. Takayama, and S. Tsukamoto "A 10-b 50-MS/s 820µW SAR ADC with on-chip digital calibration," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 6, pp. 410-416, 2010.

[17] Y. Chung, C. Yen, and M. Hsuan Wu, "A 24µW 12-bit 1-MS/s SAR ADC with two-step decision DAC switching in 110-nm CMOS,"

IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 11, pp. 3334-3344, 2016.

[18] M. Yee Ng, "0.18um low voltage 12-bit successive-approximation-register analog-to-digital converter (SAR ADC)," in *Proc. 3rd Asia Symposium on Quality Electronic Design (ASQED)*, pp. 277-281, Kuala Lumpur, Malaysia, 2011.

[19] W. Tseng, W. Lee, C. Huang, and P. Chiu, "A 12-bit 104 MS/s SAR ADC in 28 nm CMOS for Digitally-Assisted Wireless Transmitters," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2222- 2231, 2016.

[20] S. Kazeminia and S. Mahdavi, "A 800MS/s, 150μV input-referred offset single-stage latched comparator," in *Proc. 23rd International Conference Mixed Design of Integrated Circuits and Systems*, pp. 119-123, Lodz, Poland, 2016.

[21] S. Kazeminia, S. Mahdavi, and R. Gholamnejad, "Bulk controlled offset cancellation mechanism for single-stage latched comparator," in *Proc. 23rd International Conference Mixed Design of Integrated Circuits and Systems*, pp. 174-178, Lodz, Poland, 2016.

[22] W. Xiong, Y. Guo, U. Zschieschang, H. Klauk, and B. Murmann, "A 3-V, 6-bit C-2C digital-to-analog converter using complementary organic thin-film transistors on glass," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 7, pp. 1380-1388, 2010.

[23] Kh. Hadidi, V. S. Tso, and G. C. Temes, "An 8-b 1.3-MHz successive approximation A/D Converter," *IEEE J. Solid-State Circuits*, vol. 25, no. 3, pp. 880-885, June 1990.

[24] L. Cong, "Pseudo C-2C ladder-based data converter technique," *IEEE Trans. Circuits Syst. II, Analog Digital Signal Processing*, vol. 48, no. 10, pp. 927-929, 2001.

[25] Y. M. Liao and T. C. Lee, "A 6-b 1.3Gs/s A/D converter with C-2C switch-capacitor technique," in *Proc. IEEE Int. Symp. on VLSI-DAT*, pp. 1-4. Hsinchu, Taiwan, 2006.

[26] H. Kim, Y. Min, Y. Kim, and S. Kim, "A low power consumption 10-bit rail-to-rail SAR ADC using a C-2C capacitor array," in *Proc. IEEE Int. Conf. on EDSSC*, pp. 1-4, Hong Kong, China, 2009.

[27] S. Kazeminia, S. Mahdavi, and Kh. Hadidi, "Digitally-assisted offset cancellation technique for open loop residue amplifiers in high-resolution and high-speed ADCs," in *Proc. 23rd International Conference Mixed Design of Integrated Circuits and Systems*, pp. 197-202, Lodz, Poland, 2016.

[28] D. S. Khosrov, "A new offset cancelled latch comparator for high-speed, low-power ADCs," in *Proc. IEEE Asia Pacific Conference on Circuits and Systems, APCCAS*, pp. 13-16, Kuala Lumpur, Malaysia, Dec., 2010.

[29] S. W. Lee, H. J. Chung, and C.-H. Han, "C-2C digital-to-analogue converter on insulator," *IEEE Electron. Lett.*, vol. 35, no. 15, pp. 1242-1243, 1999.

[30] M. Taherzadeh-Sani, R. Lotfi, and F. Nabki, "A 10-bit 110 kS/s 1.16 \mu\hbox {W} SA-ADC with a hybrid differential/single-ended DAC in 180-nm CMOS for multichannel biomedical applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 8, pp. 584-588, 2014.

[31] W. Lai, J. Huang, and C. Hsieh, "A 10-bit 20 MS/s successive approximation register analog-to-digital converter using single-sided DAC switching method for control application," in *Proc. CACS International Automatic Control Conference (CACS 2014)*, pp. 29-33, Kaohsiung, Taiwan, 2014.

[32] S. Aghaie, J. Mueller, R. Wunderlich, and S. Heinen, "Design of a low-power calibrate-able charge-redistribution SAR ADC", 10th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), pp. 1-4 Grenoble, France, 2014.

[33] R. Rajendran, P.V. Ramakrishna, "A design of 6-bit 125-MS/s SAR ADC in 0.13-μm MM/RF CMOS process", in *Proc. International Symposium on Electronic System Design (ISED)*, pp. 23-27, Kolkata, India, 2012.

[34] S. P. Singh, A. Prabhakar, and A. B. Bhattcharyya, "C-2C ladder-based D/A converters for PCM codecs," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 6, pp.1197-1200, 1987.

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