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Table of Contents

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Research paper

Low Delay Time All Optical NAND, XNOR and OR Logic Gates Based on 2D Photonic Crystal Structure

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Abstract

Background and Objectives: Recently, photonic crystals have been considered as the basic structures for the realization of various optical devices for high speed optical communication.
Methods: In this research, two dimensional photonic crystals are used for designing all optical logic gates. A photonic crystal structure with a triangular lattice is proposed for making NAND, XNOR, and OR optical logic gates. Using the structure as the intended logic gate is possible without the need to change the structure through the use of the phase difference at the inputs. Line and point defects have been used to propagate light from inputs to output. The logical values "0" and "1", are defined based on the amount of transferred optical power to the output.
Results: The simple structure and the use of line and point defects, instead of ring resonators, reduce the complexity of the design and its use in optical logic integrated circuits. Another advantage of proposed structure, in comparison to the previous structures is the reduction in delay time that increases its speed. The maximum delay time of the proposed optical NAND, XNOR, and OR gates is about 0.1ps.
Conclusion: In this study, one structure is suggested for realizing NAND, XNOR, and OR logic gates. This structure has a small size and low delay time, and is suitable for use in optical integrated circuits.

Introduction

So far, electronic logic gates based on transistors have been used to design logic circuits, which require advanced technology to increase their speed. To increase the speed of these circuits, the dimensions of the transistors must be reduced. Reducing the size of transistors also depends on the advancement of technology in the manufacture of electronic devices. Due to the excessive reduction of the dimensions of the transistors, it seems that further reduction will have many problems [1][2]. Photonic crystals are flexible structures and most circuits that ever designed in electronics can be implemented based on photonic crystals. Therefore, these structures can be used to design integrated optical circuits. Integrated optical circuits are the underlying of reaching high speed optical computers. You can also use a variety of materials and their combinations at different wavelengths to design them. The main challenge in using these structures is their manufacturing technology, which is not currently widely available. But researchers are optimistic that in the future they will be able to build these structures and in practice be able to move towards building optical integrated circuits. Using photonic crystals as a basic structure for designing analog and digital optical devices, has attracted many researchers to the optic areas [3]. Photonic crystals are alternating structures in which this alternation can occur in 1, 2, or 3 dimensions [4]-[5]. Two-dimensional (2D) photonic crystals are used extensively in designing optical devices due to their flexibility. These structures alternate in two dimensions and are homogeneous in the third dimension. The

alternating characteristic of the structure, makes it impossible for wavelengths of lights to propagate through the photonic crystal structure. This wavelength range is called the photonic band gap (PBG) and is a continuous range. This PBG can be obtained by band structure calculations [6]-[7]. In order to transfer light through specific paths, it is necessary to make changes to the paths and to eliminate their alternating characteristic. These changes are called defects. Defect paths transfer light waves from input sources to output routes. This characteristic is used to connect the inputs and the outputs of optical devices. Defects in photonic crystals can be in the form of line or point. These pathways are used as waveguides, because light waves can be directed in these directions [8][9]. Many attempts have been made to realize photonic crystal based logic gates. The design of AND, XOR, and OR logic gates are simpler than other gates. The design of NOR, NAND, and XNOR gates is more difficult due to the fact that when the input is "0", the output should be a logic "1". An additional input, called “the bias”, is also required. In fact, the bias input is an additional source that is used to generate power at the output, when the main inputs are zero (based on the accuracy table) [10][17]. With regard to the design of the NAND and the XNOR optical logic gates, some work has been performed; in most of this work, a ring resonator has been used. This has caused an increase in the size of the circuit and the coupling light in them increases the delay-time and reduces the speed of the gates. The increase in the size of a structure is an important issue. Its reduction and its simplicity make the use of the circuit in integrated optical circuits possible [18]-[36]. In reference 15, a NAND gate is designed using photonic crystals. Although a square lattice is used in this gate, but in the proposed structure, a ring resonator is used, which reduces the speed of the gate. Also, the dimensions of the structure have been slightly enlarged due to the use of resonators. Reference 21 presents a structure for designing an OR gate based on photonic crystals. This structure is designed only for one gate and the use of three resonator rings in this structure has increased the size of the circuit and also reduced the gate speed. Also in this gate, inputs and outputs are considered on one side of the structure, which will be problematic for use in integrated optical circuits. In reference 28, a NAND gate is designed based on a photonic crystal. In this structure, a square lattice is used. The use of two ring resonators increases the size of the circuit and also increases the gate delay. Also, the large displacement of dielectric rods in this structure will make it difficult to build.

In reference 29, a NAND gate is designed that photonic crystal with a square lattice has been used. In this structure, a ring resonator is used, which increases the delay and thus reduces the gate speed. Also in this gate, the output in logic "0" state has a high optical power and the distance between two logic values is close to each other. A small distance between two logical values increases the bit detection error at the output. In addition, the size of the structure is relatively large. In reference 30, the NAND and XNOR gates are designed using photonic crystals. In this structure, because line defects are used and the structure does not have a ring resonator, it has a good speed. But because the length of this structure is a little long, the delay has been slightly increased. Also the size of the circuit is also relatively large. One of the other problems that are seen in most optical logic gates is the proximity of optical power to the two logic states. In other words, optical power is high at a logic "0" and low at a logic "1", and this can increase the probability of error in the output. Therefore, a criterion for the evaluation of the function of the logic gates is this difference. In this study, one structure is suggested for realizing three logic gates (NAND, XNOR, and OR). For using this structure as the intended gate, a phase difference is created. One of the input ports is used as the bias input. When the inputs are equal to zero, this input supplies power to the output and keeps it at a logic "1" (used in the NAND and XNOR gates). Plane Wave Expansion (PWE) method is used to analyze the band structure and calculate PBG, and Finite Difference Time Domain (FDTD) method is used for time calculations of light wave propagation from waveguide paths.

In the design of the logic gates, increasing the output power at the "1" state and reducing it at the "0" state is emphasized. Furthermore, the simplicity of this structure and making use of simple defects is another characteristic of these gates which makes it possible to use them in integrated optical circuits. In addition, not using ring resonators in the design reduces the delay-time significantly in a manner which leads to the formation of high-speed gates. The method of presentation in this study is that after the introduction, the NAND, XNOR, and OR logic gates are briefly introduced. The initial structure for realizing these optical logic gates are presented in the next section. After this section, the realization of the NAND, XNOR, and OR optical logic gates are presented (in three sub-sections separately). Finally, conclusion is presented.

Introduction to NAND, XNOR, and OR Logic Gates

NAND, XNOR, and OR logic gates have two inputs and an output. According to the logical values of the inputs, the output of the gates is determined. Figure 1 shows the circuit symbol of these logic gates. The logic value of the outputs of the logic gates are shown in Table 1. The presented tables are known as accuracy tables.

According to Table 1, the output of the NAND gate is a "1" when at least one of the inputs is a "0". The XNOR logic gate has an output of "1" when the inputs are equal. Finally, the output of the OR logic gate is a "1" when at least one of the inputs is a "1".

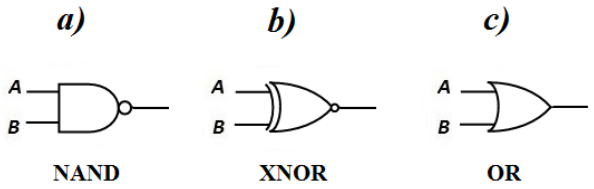

Fig. 1: Circuit schematic for the logic gates in a) NAND, b) XNOR, and c) OR

Table 1: Accuracy table of logic gates in Figure 1

INPUT A	B	NAND Gate	XNOR Gate	OR Gate
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	1	1

Initial Structure for Realizing Logic Gates

In order to obtain the intended logic gates, first, a two dimensional photonic crystal structure is considered. This structure includes a hexagonal lattice with dielectric rods in the air. The refractive index of the rods is 3 (n=3); these rods are placed next to one another in two dimensions and the background material is assumed to be air. In photonic crystals, the working wavelength should be in the PBG range. The PBG range is also a continuous range. That is, a photonic crystal structure can be used in a range of wavelengths. Also, in addition to the material of the rods, the PBG range depends on the material of the substrate as well as the lattice constant of the structure. Therefore, if the refractive index of the material changes slightly, the working wavelength can be adjusted by changing the lattice constant. $Ga_xIn_{1-x}P$ can be used as a material with a refractive index of 3 in the considered wavelength.

The lattice constant in this structure is a=0.64µm and the radius of the rods is selected to be r=0.18a. The number of rods is considered to be 19×19. That is, the number of rods that are placed next to each other in the air background, includes 19 cylindrical rods in the x direction and 19 rods in the y direction.

Figure 2 shows the structure of the original photonic crystal without defects. This structure is used to calculate the band structure. This structure creates a PBG, which does not allow the wavelength of this band to pass through the structure.

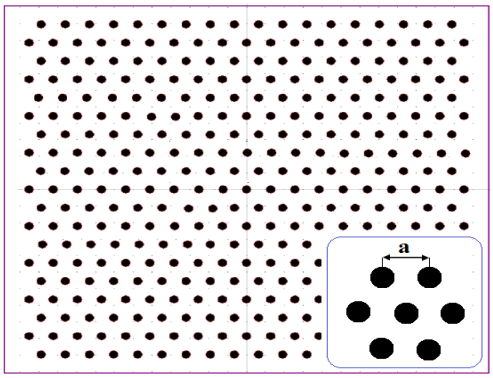

Fig. 2: Photonic crystal structure

For obtaining not-transmittable wavelengths in the structure, band structure calculations are used.

For this purpose, RSOFT software, which is very suitable software for simulating photonic crystal structures, has been used. This software greatly reduces time calculations.

The results of the band structure are shown in Fig. 3. The proposed structure creates a PBG for TM mode. Therefore, the band structure simulation is calculated for this mode.

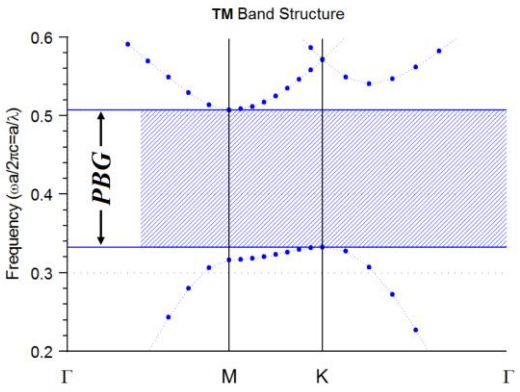

Fig. 3: Band structure of the proposed structure.

Figure 3 shows the PBG range for the intended structure by using band structure calculations. As observable in the normalized wavelength $(\frac{a}{\lambda})$ interval, in the range between 0.33 and 0.51, light is not transmittable in the structure, and these wavelengths are reflected on hitting the structure. The wavelength equivalent with this interval falls in the range from 1.25µm to 1.94µm.

At other wavelengths, light is transmitted in the structure, and cannot be guided in the intended paths of the structure. Hence, in order to transfer light in specific paths in the structure, light-source wavelengths should be in the PBG range. Here, the wavelength considered for the light source is 1.55µm, that is in the PBG range. This wavelength is the third communications window.

Realizing the NAND, XNOR, and OR Optical Gates

In order to create optical gates using the proposed structure, three input paths and one output path have been provisioned. The paths for the passage of light is created by using line and point defects in such a way that all the three paths intersect in one location. Point defects are used at the intersection of the three paths. Point defects include four defects that are a result of the change in the rod radius.

The radius of the three rods a, b, and c are halved and the radius of rod d is multiplied by 1.2. This structure is used for the three NAND, XNOR, and OR optical gates. Line and point defects are shown in Fig. 5, 6 and 7.

When the structure is used as NAND and XNOR gates, one of the input ports is chosen as the bias for supplying power to the outputs when the inputs are "0". To use the proposed structure as an OR gate, two ports are used as input and the third port is not used.

To achieve the desired outputs according to the accuracy table, and the interaction of the waves propagated in the input paths, phase difference has been used for some inputs and bias input relative to each other.

A. Nand optical logic gate

In order to use, the proposed structure as a NAND optical gate, A and B inputs, and the bias source are selected as shown in Fig. 4a. Input B has a phase difference of 110° and the bias source has a phase difference of 75° with respect to input A.

The results of the simulation of the NAND optical gate are shown in Fig. 4b. This diagram shows the normalized output optical power. The results show that under the condition A=B=0, the output is equal to 0.83. This power is supplied by the bias source.

When A=0 and B=1, the optical output power is 0.85; when A=1 and B=0, the output is 0.88.

The phase differences and the point defects are selected in such a way that when the output is in the "1" logic state, the light waves come together at the defects in such a way that they interfere with the bias source and the value of output power is similar in all the three cases. In these three cases, considering that the outputs are high, they can be considered a logic "1". When the inputs A=B=1, the power transmitted to the output is very low (about 0.12), which can be considered a logic "0". In the optical gate described, the interval between the two logic states of "0" and "1" is 0.71. This difference reduces the error in determining a high or a low logic level at the output. Furthermore, Figure 4b shows that the delay time in output response to the input is approximately 0.1ps. Considering the fluctuations in the output when the inputs become active, the time required for the output to become stable is about 0.4ps. One of the reasons for the reduction of delay time relative to previous works is the small size of the structures and the nonuse of the ring resonators.

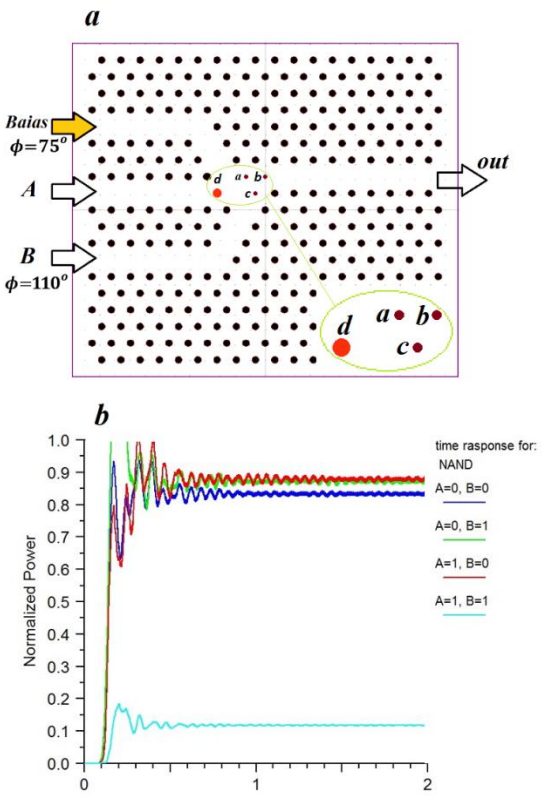

Fig. 4: a) Optical NAND structure and b) Normalized output power.

B. XNOR Optical Logic Gate

Using the suggested structure as an XNOR optical gate is possible without changing the structure and only through the change of phase difference in the inputs. To achieve this, the phase difference of the bias source with respect to the two main inputs A and B is considered to be 65°. Fig. 5a shows the placement of the inputs and the bias source for use as an XNOR optical logic gate. Fig. 5b shows the normalized output power for various inputs to the optical XNOR gate. According to the figure, the output is high (a logic "1") when the inputs A and B are equal; when the inputs are not equal, however, the output has little power (a logic "0"). This is similar to the XNOR gate. The results of the simulation show that the normalized output power is about 0.61, when the inputs A=B=0. This amount of optical power is equivalent to logic "1". Also, the output power is about 0.64 (a logic "1") when A=B=1.

The output power, when A=0 and B=1, and A=1 and B=0 are 0.06 and 0.12, respectively which are equivalent to logic "0". Considering these values, the interval between the two logic states of "0" and "1" is 0.49. In the XNOR optical gate, the input bias is active, and when the inputs are off, it supplies power to the output.

When both inputs are on, the paths taken by the light waves from the sources and the phase difference of the bias source are chosen such that the point defects and the light interferences cause the power transferred to the output to be equal to the "1" logic state.

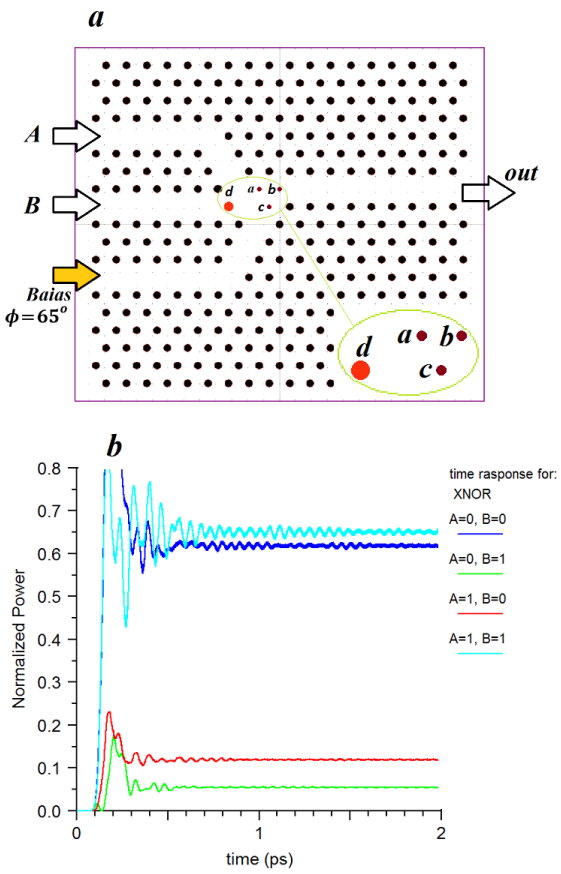

Fig. 5: a) Optical XNOR structure and b) Normalized output power.

When the inputs are not equal, the interference between the active input and the bias source is such that the transmission output power in both cases is low.

The time required for the output responding to the input source is almost 0.1ps, and the time required for the output to become stable is about 0.3ps. This low delay time, as well as the small size of the proposed structure, makes this optical gate suitable for use in high speed optical integrated circuits.

C. OR Optical Logic Gate

The proposed structure can also be used as an OR gate as well. For access this gate, two sources are selected for the inputs and there is no need for a bias source. Considering the results obtained from the optical NAND gate, if the phases of the upper and the lower sources (as shown in Figure 6a) are selected to be 75° and 110°, respectively, the structure functions as an OR gate. The selection of the inputs A and B is shown in Figure 6a. It is clear that, if both inputs are turned off, the power emitted to the output is zero. The output powers for the other three cases are shown in Figure 6b. These values are calculated and found to be normalized.

The diagram obtained shows that in the condition that one of the inputs is switched on, the power emitted to the output is considerable (a logic "1"). For the condition in which A=0 and B=1, the value of normalized power at the output is 0.61, whereas in the condition A=1 and B=0, the value is equal to 0.83. When A=B=1, the normalized power at the output is 0.85. Considering that the output power at a logic "0" is equal to zero and the least power at a logic "1" is 0.61, the output power interval is 0.61 in the worst case.

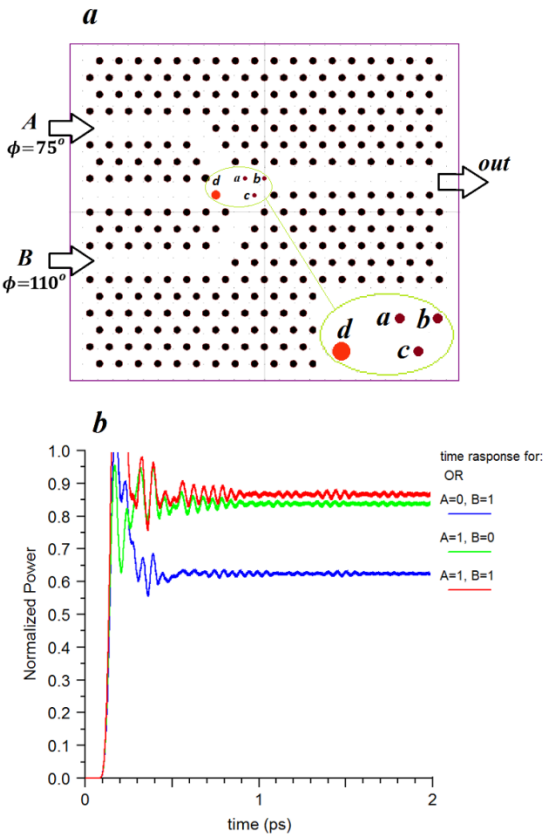

Fig. 6: a) Optical OR structure and b) Normalized output power.

The time diagram shows that the delay time of the optical gate is about 0.1ps and the time required for the output to become stable is about 0.4ps.

Comparing the three optical logic gates (NAND, XNOR, and OR) shows that the time required for the output to become stable in the XNOR gate is about 0.3ps and in the NAND and the OR gates, the time is about 0.4ps. Considering that this time is very short, the suggested optical gates can be used as high-speed optical gates.

Table 2 shows the simulation results for all three logic gates, NAND, XNOR and OR. This table shows the values of the normalized output power for each gate, as well as its equivalent value.

According to Table 2, it is clear, that the output power of each gate is low in the "0" logic state. Also in "1" logic

state, the power is high. These values indicate that the designed gates have a reasonable logical distance and the detection error at the output will be reduced.

The detection error at the output depends on the distance between the two logic values "0" and "1". The smaller distance between the two logic values"0" and "1", will cause the correct detection for the logical values at the output. In this case, the error detection for bits will be reduced.

Table 2: Normalized output optical power for NAND, XNOR, and OR optical logic gates

INPUT A	INPUT B	NAND Output (logic)	XNOR Output (logic)	OR Output (logic)
0	0	0.83 (1)	0.61 (1)	0.00 (0)
0	1	0.88 (1)	0.06 (0)	0.61 (1)
1	0	0.88 (1)	0.12 (0)	0.83 (1)
1	1	0.12 (0)	0.64 (1)	0.85 (1)

The value of Contrast Ratio (CR), which represents the distance between the two logical values "1" and "0", is calculated as the relation CR= 10log(P_1/P_0). Where P_1 and P_0 are the power transmissions to the output in the "1" and "0" logic state, respectively. According to Table 2, this value is equal to CR= 8.4dB for NAND gate and CR= 7.1dB for XNOR gate. Also for the OR gate, since the amount of power in the "0" logic state is zero, the value will be high, for all OR structures.

Due to the fact, that the output of the "NAND" and "XNOR" gates, for zero inputs must be "1", the design of this gate is more difficult than other gates and requires an additional input. Therefore, the design of these gates is usually accompanied by an increase in size. In this paper, a simple structure with small dimensions is used to design these gates.

The results obtained for the NAND, XNOR and OR logic gates are shown in Fig. 4-6. Diagrams b in these figures show the normalized transfer power at the output. These figures show that the designed logic gates have high output power in "1" logic state and low power in "0" logic state. Therefore, it can be said that in this structure, the bit detection error in the output is reduced. Also, due to the low delay in light emission from input to output, the designed gates have a high speed and can be used in high speed optical circuits. To study the effect of wavelength changes, the above structures can be simulated for different wavelengths. However, since the desirable structure for all three gates has the same paths, one of the modes when the structure is used as an OR gate is re-simulated for 1.5um and 1.6um wavelengths and the results obtained are shown in Fig. 7 and 8.

Figure 7 shows the transmission power at the output of the OR gate for the 1.5µm wavelength.

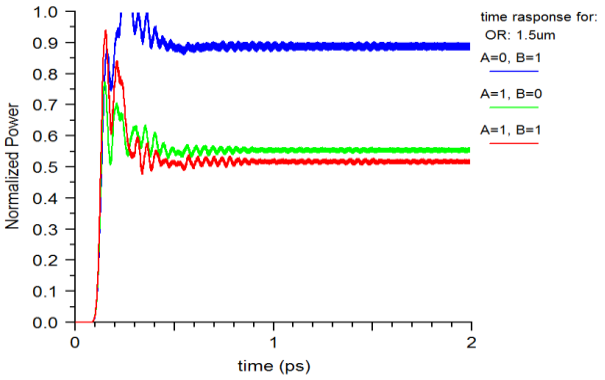

Fig. 7: Normalized output power for OR gate at $\lambda = 1.5\mu m$.

As it is shown in Fig. 7, in cases where the output is in the "1" logic state, one of the outputs is slightly increased but the other two outputs are greatly reduced so that the normalized value is approximately 0.5 and this value is low for logical "1" state.

Now the same OR gate structure is simulated for the 1.6µm wavelength and the normalized power results at the output are shown in Figure 8.

According to Figure 8, it can be seen that the amount of output power for input A=1, B=0 has not changed much and the output power for input A=B=1 has increased significantly. But in the case of A=0, B=1, the amount of output power is reduced to about 0.4 normalized, and this value is very small for logical "1" state. On the other hand, in a logic gate, the proximity of the logic "1" values in different modes is an advantage, because bit detection sensors for different logic "1" values may cause problem.

It should be noted that the proposed NAND and XNOR gates have less losses in this wave length and have better performance considering that designed to propagate light at a wavelength of 1.55µm.

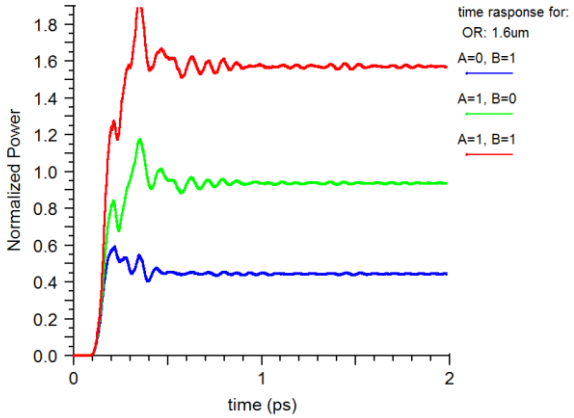

Fig. 8: Normalized output power for OR gate at $\lambda = 1.6\mu m$.

Results and Discussion

In this paper, one structure is suggested for realizing three logic gates. To compare the proposed gates with

the recently designed gates, Table 3 is given. Table 3 shows the simulation results for the designed gates, for the output parameters. These parameters are: structure size (number of rods in horizontal and vertical directions), delay time (the time when the input effect appears on the output) and Contrast Ratio. Table 3 shows that the proposed structure has a smaller size than other references, and therefore, is expected to have less delay time. The CR parameter is also increased. The reason for increasing CR in the proposed structure is the large output power distance for the two logic values.

Table 3: Comparison table of the proposed gate with a number of similar references

Reference	Gates	Size (Number of Rods)	t_{delay}	CR(dB)
[21]	OR	24×31	-	7.27
[29]	NOR	37×27	-	3.5
	NAND			3.4
[34]	XNOR	46×45	0.5ps	6.3
	NAND			3.74
[35]	XNOR	20×41	-	7.2
	NAND			7.4
This work	XNOR	19×19	0.1ps	7.1
	NAND			8.4

Conclusion

In this research, a fixed photonic crystal structure with small dimensions is used as the three optical logic gates. Values of output optical power are determined based on the interference of light waves in the defect paths created. The "0" and "1" logical values are defined based on the value of optical power. The results show that the logic gates have an output power close to zero at a logic "0" and close to the input power source at a logic "1". The difference between a "0" and a "1" is relatively large, which is considered one of the advantages of these gates. Furthermore, considering the short delay time of this structure, the designed gates have high speed.

Author Contributions

M.R. Malmir designed and simulated and carried out the data analysis, and F. Parandin collected the data and interpreted the results and wrote the manuscript.

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Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

Abbreviations

There is no abbreviation.

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Research paper

A Novel Method Design Multiplexer Quaternary with CNTFET

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Abstract

Background and Objectives: In recent decades, due to the effect of the short channel, the use of CMOS transistors in the nanoscale has become a major concern. One option to deal with this issue is the use of nano-transistors.

Methods: Using nano-transistors and multi-valued logic (MVL) can reduce the level of chips and connections and have a direct impact on power consumption. The present study reports the design of a new method of Multiplexers (MUXs) based on quaternary logic and transistors of carbon nanotubes (CNTFET) and having a new look at the layout and use of MUXs.

Results: The use of special rotary functions and unary operators in Quaternary logic in the design of MUXs reduced the number of CNTFETs from 27% to 54%. Also, the use of MUXs in the Adder structure resulted in a 54% reduction in Power Delay Product (PDP) and a 17.5% to 85.6% reduction in CNTFET counts.

Conclusion: The simulated results display a significant improvement in the fabrication of Adders, average power consumption, speed, and PDP compared to the current best-performing techniques in the literature. The proposed operators and circuits were evaluated under various operating conditions. The results show the stability of the proposed circuits.

Introduction

Advances in science and technology have considerably increased human need for information, rapid processing, and storage. As a result, scientists face the challenge of fabricating compact integrated circuits that can simultaneously reduce energy consumption and boost the speed of systems. With the advent of complementary metal-oxide-semiconductor (CMOS) technology, technological advancements provided CMOS transistors with further challenges such as short channel effects, leakage current, increased power consumption, and high sensitivity to orbital parameters, which incentivize scientists to take advantage of new technologies at the nanoscale [1], [2]. The remarkable similarity between carbon Nanotube field transistors (CNTFETs) and Metal Oxide Semiconductor Field Effect Transistor (MOSFETs) has been the subject of intense research. CNTFETs enjoy high carrier mobility, low power consumption, lower latency, and smaller intrinsic capacitors, resulting in the acceleration of these elements. Due to the identical mobility of electrons and holes, P and N types of these transistors are similar in terms of channel length. One of the unique features of CNTFETs is the variation of the threshold voltage caused by changing the channel length [3]. Using these transistors along with multi-value logic (MVL) has thus greatly reduced the volume of integrated circuits. MVL circuits do not share common problems of binary circuits such as the high number of connections and higher power consumption [4]. Accordingly, they reduce the intricacy of the circuits and chip surface and allow implementing the rational and mathematical functions at a higher rate and fewer computations [5]. Multi-valued logic is divided into Ternary, Quaternary, and

Pentanary groups, with the Ternary having been more extensively researched than the other two. Among the highest and the lowest levels in MVL circuits, Quaternary logic can be the right option in designing microprocessors. Different circuits have been designed using CNTFETs and MVL logic. Ternary and quaternary circuits work directly with ternary and quaternary logic [6], [7]. The circuits work by converting Ternary and Quaternary to binary and vice versa [8], [9], and by MUXs [10], [11]. Because most computational operations are performed by adding an operator, in this study, different adder blocks were designed using MUXs and circuits with quaternary logic. New insights into MUXs and circuits dramatically reduced the number of transistors, average power consumption, propagation delay, and PDP compared with previous results [6], [12]-[16]. The remainder of the paper is organized as follows. Next Section describes the basic principle. Next Section includes the proposed circuit design. Next Section presents the simulated results and comparison. Finally, Section presents the conclusions.

Principles

A. Carbon Nano Tube Field Effect Transistor (CNTFET)

Nanotubes are graphite plates with a tubular form and hexagonal structure. The nanotube plates can be conductive or semiconductor depending on their rotational axis. Carbon nanotubes are composed of tubular graphite plates that are based on the chirality vector C= $m\alpha_1 + m\alpha_2$, where α_1 and α_2 are the unit vectors of the graphite plate and the chirality (m, n) determines how the CNTs twist. SWCNTs can be conductors or semiconductors. If m and n are equal (m = n) or their product is a multiple of 3 (m·n = 3i), then the nanotube will exhibit metal conductivity. Otherwise, the produced nanotube will exhibit a semi-conductive property [17]. Fig. 1 shows the structure of the CNTFET structure. The appropriate threshold voltage for CNTFETs can be obtained using an appropriate CNT diameter. The CNTFET threshold voltage is inversely related to the nanotube diameter as follows [12].

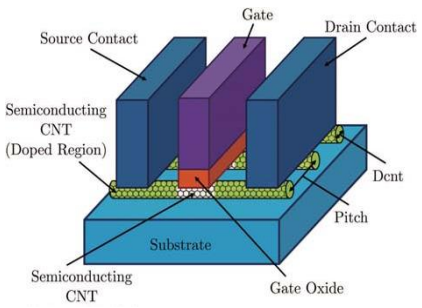

Fig. 1: The structure of the CNTFET.

$$V_{th} \approx \frac{E_g}{2.e} = \frac{\sqrt{3}}{3}\frac{a.V_\pi}{e.DCNT} \approx \frac{0.43}{DCNT(nm)} \quad (1)$$

$$DCNT = \frac{a.\sqrt{m^2+n^2+m.n}}{\pi} = 0.078\sqrt{m^2+n^2+m.n} \quad (2)$$

where α is the distance between two adjacent carbon atoms ($a \cong 0.248$), Vπ is the bond energy between the two carbon atoms (Vπ = 0.033), e is the unit electron charge, and DCNT is the diameter of the carbon nanotube. Therefore, using a CNTFET transistor with appropriate nanotube diameters, different threshold voltages, which are the basis for evaluating various logical levels, can be created. The relations between chirality, CNT diameter, and threshold voltage are shown in Table 1.

Table 1: The relations between chirality, CNT diameter, and threshold voltage

(n, m)	Diameter (CNTs)	Threshold voltage (N-NTFET)	Threshold voltage (P-CNTFET)
(19,0)	1.487 nm	0.289 V	-0.289 V
(17.0)	1.330 nm	0.328 V	-0.328 V
(16,0)	1.253 nm	0.348 V	-0.348 V
(14,0)	1.100 nm	0.398 V	-0.398 V
(13,0)	1.018 nm	0.428 V	-0.428 V
(11,0)	0.861 nm	0.506 V	-0.506 V
(10,0)	0.783 nm	0.559 V	-0.559 V

B. Quaternary Logic

The Quaternary logic consists of four voltage levels, as shown in Table 2 [18]. Logical functions are also introduced based on quaternary logic such as QNAND, QNOR, QNOT, and other special functions [12], [14].

Table 2: Corresponding voltages with logic values

Scale	Logic	Voltage(v)
GND	'0'	0
Vdd/3	'1'	0.3
2Vdd/3	'2'	0.6
Vdd	'3'	0.9

Multi-value functions have various functions due to the type of particular attitude assigned to them; e.g. the inverter has several functions such as Intermediate Quaternary Invert (IQI), Negative Quaternary Invert (NQI), Positive Quaternary Invert (PQI), and Standard Quaternary Standard Invert (SQI) [5], [18].

$$QNOT(a) = 3 - a \quad (3)$$

$$QNAND(a,b) = \overline{MIN(a,b)} = \begin{cases} 3-a & if \quad a \le b \\ 3-b & otherwise \end{cases} \quad (4)$$

$$QNOR(a,b) = \overline{MAX(a,b)} = \begin{cases} 3-a & if \quad a \ge b \\ 3-b & otherwise \end{cases} \quad (5)$$

The accuracy table of inverter functions is presented in Table 3.

Table 3: The truth table of quaternary inverter

IN	NQI	PQI	IQI	SQI
0	3	3	3	3
1	0	3	3	2
2	0	3	0	1
3	0	0	0	0

Equation (3) equal to the SQI function, which its accuracy is shown in Table 3.

C. Efficient CNTFET-based circuits for unary operators

In the design of multiplexer-based circuits, special functions and Unary functions are used. These functions are shown in Table 4 and the sample circuits that include these functions are shown in Fig. 2.

AP is equivalent to PQI function, AN is equivalent to NQI function, and AI is equivalent to IQI function. Different circuit operators are defined according to design requirements in this paper [8], [14], [17]. Here, A1, A2, and A3 are rotational quaternary logic operators that represent the beginning of function with the level according to their index. For example, operator A1 starts at level 1 and A2 begins at level 2.

These operators were constructed by varying the voltage levels of the chirality vector according to the status of A and its dependent operators. Fig. 2 illustrates this procedure. MUX 4*1 was applied to construct operators A1, A2, and A3. The voltage levels L1 (0.3v) and L2 (0.6v) were generated by the voltage divider. In Fig. 2 (g), operators S1 and S2 are used to control multiplexer outputs.

For example, in operator A1, when A goes through its corresponding levels 0, 1, 2, and 3, respectively, voltage levels (A) of transistors T4, T5, T6, and T7 are switched on, while levels 1, 2, 3, and 0 are switched on as its output. This is also the case for operators A2 and A3, which produce different levels of output proportional to the input A [14].

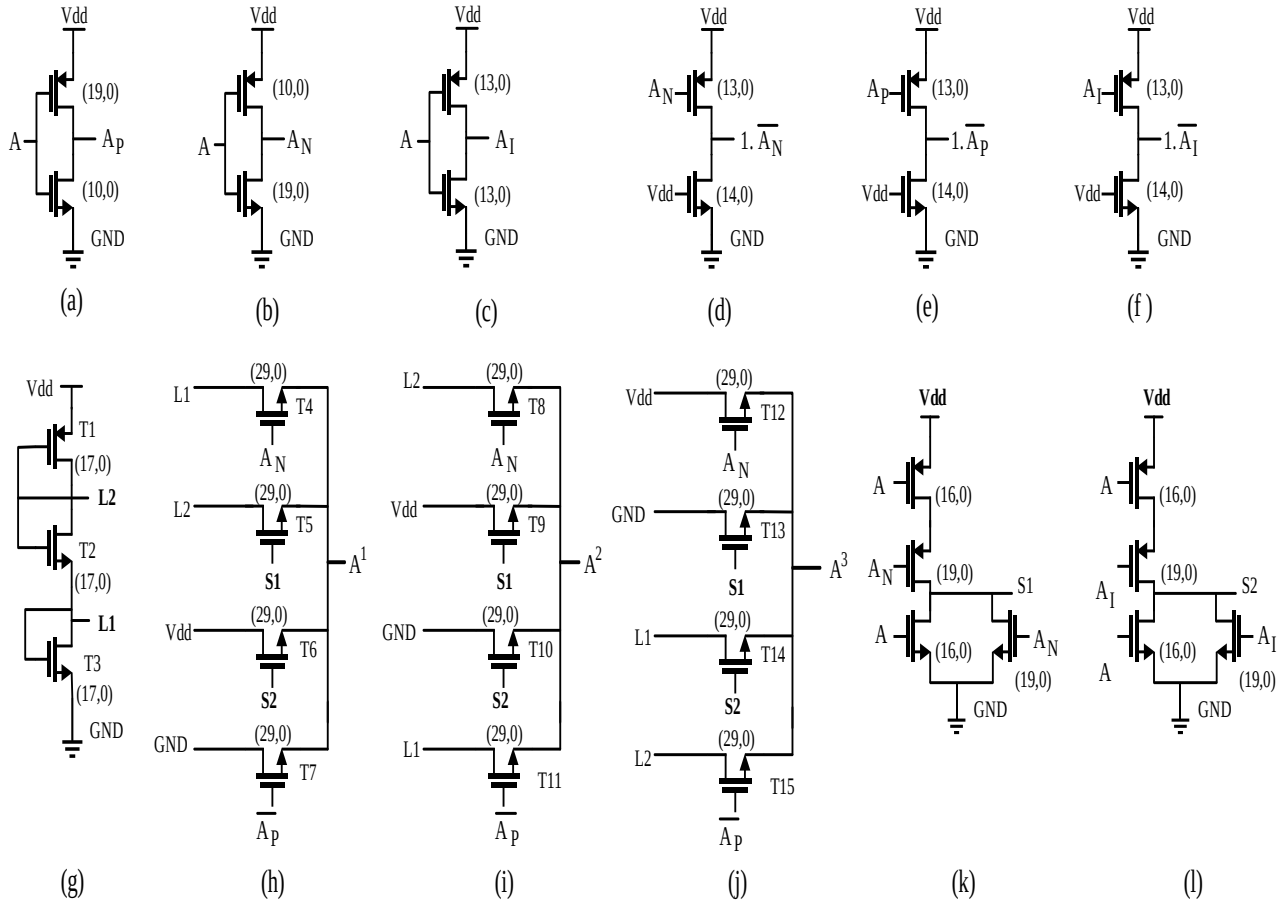

Fig. 2: CNTFET circuits for unary operators: (a) A_P (b) A_N (c) A_I (d) $1.\overline{A_N}$ (e) $1.\overline{A_P}$ (f) $1.\overline{A_I}$ (g) voltage divider (h) A^1 (i) A^2 (j) A^3 (k) S1 (l) S2.

Table 4: Truth table of unary operator

A	A_P	A_N	A_I	A^1	A^2	A^3	$1.\overline{A_P}$	$1.\overline{A_N}$	$1.\overline{A_I}$	$S1$	$S2$
0	3	3	3	1	2	3	0	0	0	0	0
1	3	0	3	2	3	0	0	1	0	3	0
2	3	0	0	3	0	1	0	1	1	0	3
3	0	0	0	0	1	2	1	1	1	0	0

Proposed Circuits

Normally, multiplexers are circuits that connect multiple information inputs to an output according to different choices. In this section, we propose different models of MUXs (i.e., 8*4, and 12*4), depending on their application in the adder circuit.

A. Proposed Quaternary Multiplexer

One of the most common methods of designing multiplexers is shown in Fig. 3. In this method, according to the voltage levels of the selector signal, one of the inputs is connected to the output. In the above circuit, in addition to the selector signal B, the input signal has also quaternary values. In this case, if B = 0, 1, 2, and 3, the inputs D1, D2, D3, and D4 are transferred to the output, respectively. In this design, the signal B1 has an output when the voltage level of the signal B has reached 1 logic (0.3 v) and the output of the signal B2 is activated in B = 2. A total of 30 CNTFETs are used in the Multiplexer shown in Fig. 3.

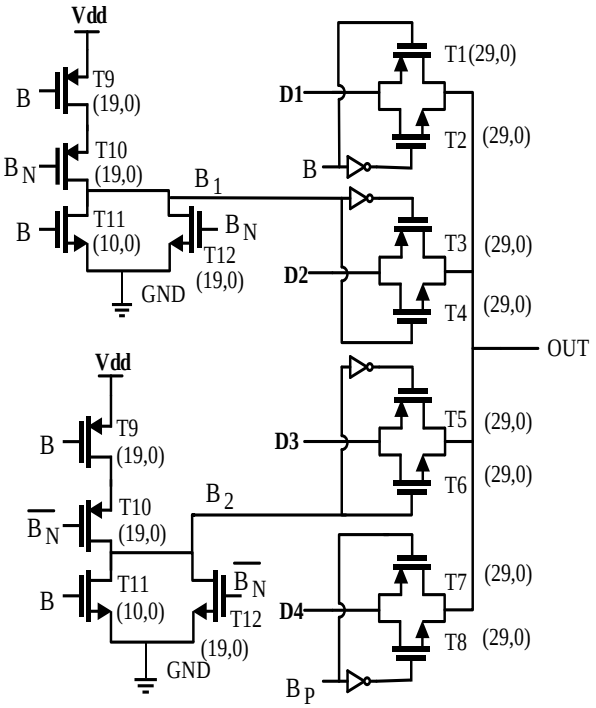

Fig. 3: Structure of MUX 4*1 using the proposed design.

One of the applications of these multiplexers is in the design of Adder circuits.

Table 5 shows the accuracy of a half adder and Fig. 4 shows the application of a MUX 4*1 in the construction of a half adder.

Table 5: The truth table for quaternary half adder [13]

	Product						Carry				
A						A					
B	0	1	2	3		B	0	1	2	3	
0	0	1	2	3	A	0	0	0	0	0	0
1	1	2	3	0	A^1	1	0	0	0	1	$1.\overline{A_P}$
2	2	3	0	1	A^2	2	0	0	1	1	$1.\overline{A_I}$
3	3	0	1	2	A^3	3	0	1	1	1	$1.\overline{A_N}$

According to Table 5, the value of sum and carry are obtained as:

$$\begin{aligned} Sum &= B_0(A_0 + A_1 + A_2 + A_3) + B_1(A_1 + A_2 + A_3 + A_0) \\ &+ B_2(A_2 + A_3 + A_0 + A_1) + B_3(A_3 + A_2 + A_1 + A_0) \end{aligned}$$

$$\begin{aligned} Carry &= B_0(0) + B_1(1.A_3) + B_2((1.A_2) + (1.A_3)) \\ &+ B_3((1.A_1) + (1.A_2) + (1.A_3)) \end{aligned} \quad (6)$$

where A_0, A_1, A_2, and A_3 are equal to levels A = 0, 1, 2, and 3, respectively. This also applies to B and its various levels. The sum and carry are rewritten as relationships in (7).

$$Sum = B_0(A) + B_1(A^1) + B_2(A^2) + B_3(A^3)$$

$$Carry = B_0(0) + B_1(1.\overline{A_P}) + B_2(1.\overline{A_I}) + B_3(1.\overline{A_N}) \quad (7)$$

Based on (7), it is possible to design Sum and Carry using two MUX 4*1. This can be seen in Fig. 4. In this combination.

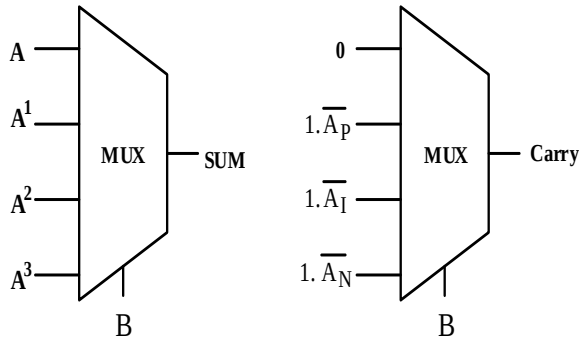

Fig. 4:. Proposed Design QHA.

B acts as a selector in MUX units. Also, by selecting one of the B levels in the Sum operator, one of the inputs A, A^1, A^2, and A^3 is considered as output. Moreover, in the Carry operator, B is selected among the operators $1.\overline{A_P}$, $1.\overline{A_I}$, $1.\overline{A_N}$ and 0 is the output.

Two half adders can be used to design the full adder. The full adder block consists of two inputs A and B, one input carry (Cin), and two outputs including Sum and output carry (Cout). According to Table 5, the maximum carry produced is 0 and 1, so Cin can be a maximum of 1. Table 6 shows the accuracy of the performance of a full adder and Fig. 5 presents its structure with the basic blocks of MUX 4*1. Fig. 5 presents a full adder block for each output Sum and Carry, including two blocks MUX 4*1 and one block MUX 2*1. The structure of the first full adder proposed in this article is shown in Fig. 6. Selector signals C and B are shifted together at the beginning and end of the adder block. Each Sum and Carry output consists of 8*4 and 4*1 MUXs, of which the MUX 4*1s is less used than the base full adder mode. In the MUX 8*4 structure, Cin is used as the selector, for example, by selecting C = 0, operator A, A^1, A^2, and A^3 are transferred to the outputs while selecting C=1, operators A^1, A^2, A^3, and A are transferred to the outputs.

Table 6: The truth table of a proposed quaternary full adder with unary

Cin	B	A	Sum	Cout
0	0	A	A	0
0	1	A	A^1	$1.\overline{A_P}$
0	2	A	A^2	$1.\overline{A_I}$
0	3	A	A^3	$1.\overline{A_N}$
1	0	A	A^1	$1.\overline{A_P}$
1	1	A	A^2	$1.\overline{A_I}$
1	2	A	A^3	$1.\overline{A_N}$
1	3	A	A	1

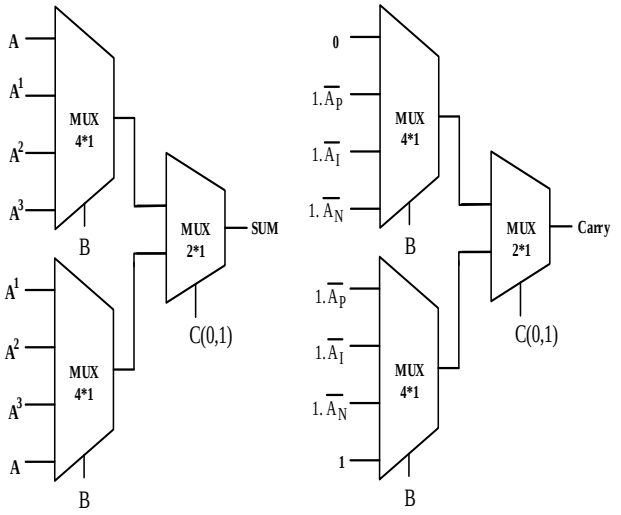

Fig. 5: Structure of the base quaternary FA [3].

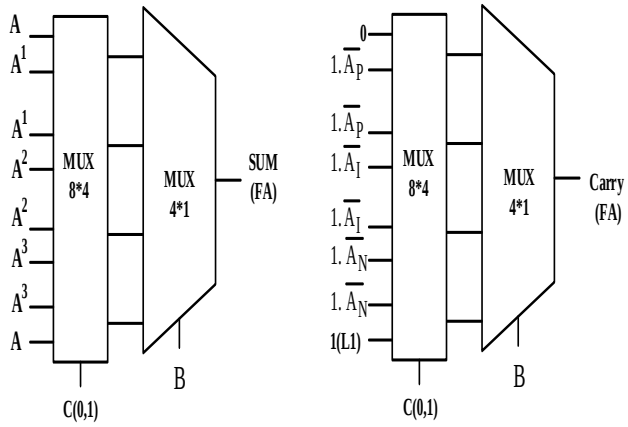

Fig. 6: The structure of the proposed QFA1.

As mentioned earlier, in normal mode, the highest carry will be 1 and can move to the next block in addition to the action. In the worst case, the Cout of a sum block can be the sum of 3 digits each with a value of 3. In this case, the maximum output Cout can be a value of 2 that can move to the next block. Table 7 presents the obtained results.

To build a full adder based on Table 7 and with a basic multiplexer structure, 3 MUX 4*1 and 1 MUX 3*1 are required for each Sum and Carry output. The second full adder proposed in this article and with the idea expressed in the first full adder (Fig. 6) requires a MUX 12*4 and a MUX 4*1 to build each of the Sum and Carry blocks. In the new structure, 4 MUX 4*1s are less used than the base full adder mode. presents the structure of the second proposed full adder. In the MUX 12*4 structure, Cin is used as the selector; for example, by selecting C = 0, inputs A, A1, A2, and A3 appear at the outputs. In this way, 4 inputs are transferred to 4 outputs for each selection. Table 8 and Fig. 8 display the

accuracy table and structure of the CE operator, respectively.

Table 7: QFA2 truth table

Cin	B	A	Sum	Cout
0	0	A	A	0
0	1	A	A^1	$1.\overline{A_P}$
0	2	A	A^2	$1.\overline{A_I}$
0	3	A	A^3	$1.\overline{A_N}$
1	0	A	A^1	$1.\overline{A_P}$
1	1	A	A^2	$1.\overline{A_I}$
1	2	A	A^3	$1.\overline{A_N}$
1	3	A	A	1
2	0	A	A^2	$1.\overline{A_I}$
2	1	A	A^3	$1.\overline{A_N}$
2	2	A	A	1
2	3	A	A^1	CE

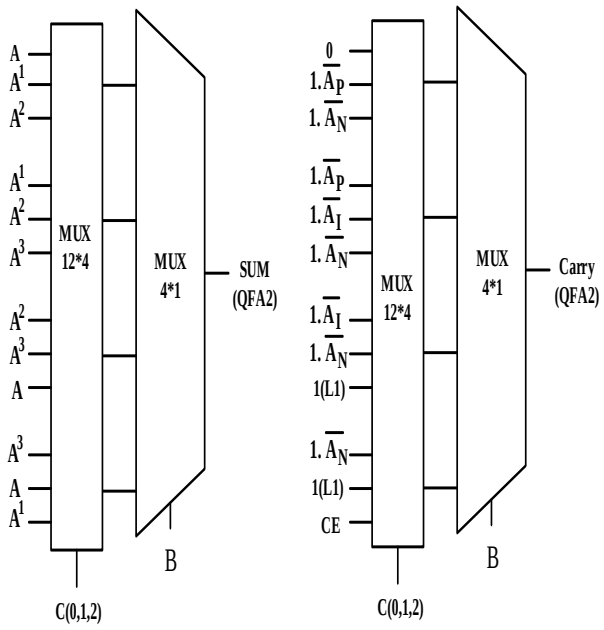

Fig. 7: The structure of the proposed QFA2.

Table 8: The truth table of the CE operator

Cin	B	A	Sum	Cout
2	3	0	1	1
2	3	1	2	1
2	3	2	3	1
2	3	3	0	2

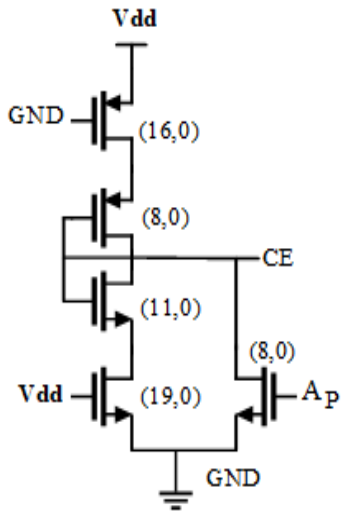

Fig. 9: Unary operator CE structure.

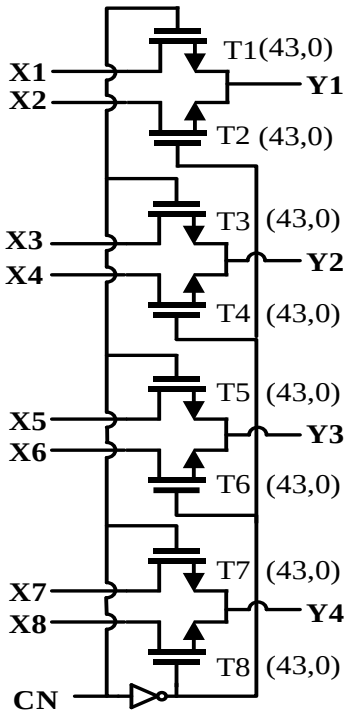

Fig. 10: Structure of the MUX8*4 used in the proposed QFA1.

B. Proposed Structure Multiplexer

As mentioned in the previous section, in the proposed full adder, MUX 8*4 or MUX 12*4 were used to reduce their dimensions. The structure of these multiplexers is shown in Fig. 10 and 10. In the structure of these multiplexers, the Pass Transistor Logic method was used. Fig. 10 shows the structure of the MUX 8*4. In this MUX, if C = 0, transistors T1, T3, T5, and T7 turn on and inputs X1, X3, X5, X7 are transferred to the outputs. Also, if C = 1, transistors T2, T4, T6, and T8 turn on and the inputs X2, X4, X6, X8 are transferred to the output. A total of 10

CNTFETs were used for constructing the MUX 8*4. In the construction of the base full adder (

Fig. 5, 4 MUX 4*1 and 2 MUX 2*1, as well as 132 CNTFETs, were used. Regarding the structure of the first full adder proposed, two MUX 8*4 and two MUX 4*1 were used. Totally, 96 CNTFETs were used, indicating a 27% reduction.

C. Proposed Structure Multiplexer

As mentioned in the previous section, in the proposed full adder, MUX 8*4 or MUX 12*4 were used to reduce their dimensions. The structure of these multiplexers is shown in Fig. 10 and 10. In the structure of these multiplexers, the Pass Transistor Logic method was used. Fig. 10 shows the structure of the MUX 8*4. In this MUX, if C = 0, transistors T1, T3, T5, and T7 turn on and inputs X1, X3, X5, X7 are transferred to the outputs. Also, if C = 1, transistors T2, T4, T6, and T8 turn on and the inputs X2, X4, X6, X8 are transferred to the output. A total of 10 CNTFETs were used for constructing the MUX 8*4.

In the construction of the base full adder (Fig. 5), 4 MUX 4*1 and 2 MUX 2*1, as well as 132 CNTFETs, were used. Regarding the structure of the first full adder proposed, two MUX 8*4 and two MUX 4*1 were used. Totally, 96 CNTFETs were used, indicating a 27% reduction.

Fig. 13 shows the MUX 12*4 structure used in the proposed second full adder. This MUX has 20 CNTFETs. In MUX 12*4, if the signal C is selected 0, 1, or 2, then three groups of transistors (T1, T4, T7, T10), (T2, T5, T8, T11), or (T3, T6, T9, T12) are turned on to transmit input data to outputs.

In the base full adder, according to Table 7 and Fig. 5, 6 MUX 4*1 and two MUX 3*1 are required. A total of 224 CNTFEs were used to build multiplexers. In the design of the proposed second full adder (Fig. 5), 104 CNTFETs are used, which reduced the number of transistors by 53.6%.

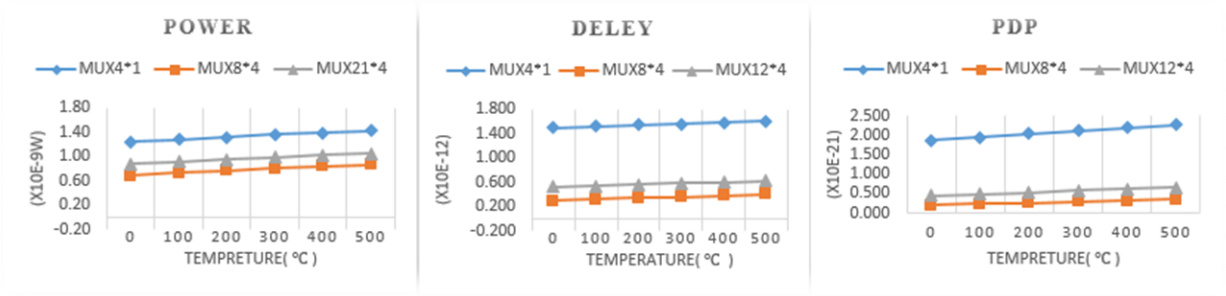

Fig. 11: Evaluation of the proposed MUX for different temperatures.

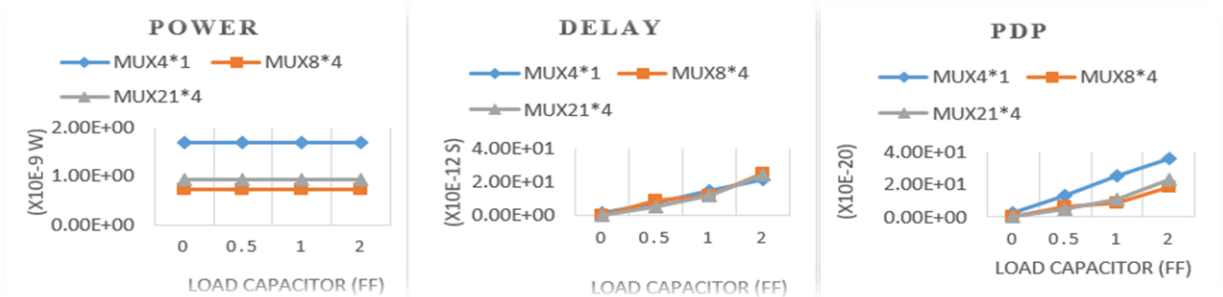

Fig. 12: Evaluation of the proposed MUX for different load capacitors.

Results and Discussion

The simulation was run using Hspice software and 32 nm technology with a standard model proposed at Stanford University [18], [21].

In designing the circuits of Fig. 3, 6, and 7, nanotubes were considered to be between 4 and 8 such that MUX circuits were designed to have the best flow drive, a good fan-out with 8 tubes, and a control circuit with 4 tubes.

Fig. 11 and 12 present the accuracy and performance of the circuits designed at different temperatures and under different loads, respectively.

According to Fig. 11, variations of the power consumption are approximately 4 e-11w and the delay changes are approximately 2 e-14s to per 100°C. The proposed full adders were simulated using a 0.9-volt power supply.

The performance of evaluation criteria including delay propagation, average power consumption, and PDP, the number of transistors used, and the number of used power supplies are shown in Table 9. In this evaluation, the worst-case propagation delay includes the longest signal path and the maximum delay.

Table 9 compares all proposed full adders without load and in the presence of 0.7 and 2 fF capacitor loads. The results show a significant decrease in the number of transistors used, PDP, average power consumption, and propagation delay. The results of the first design [14] with no load were better than those of the proposed design.

However, [14] uses 3 power supplies while we employed just one power supply. As shown in the first proposed full adder, the number of transistors used indicates a 32% to 88% reduction compared to other designs.

Also, the proposed PDP design indicates a 50% to 100% reduction compared to other designs. Energy consumption in [20] with 0.7 FF capacitor load was better than the second proposal.

However, [20] uses 3 power supplies while we use only one power supply. As shown in the results of the second proposed full adder, 81.3% increase the propagation speed compared to [20] and in PDP 29% decrease compared to [19].

Finally, in the second full adder proposal, the number of transistors used indicates a 17.5% to 85.6% reduction compared to other designs and in 2fF capacitor load the resulting PDP decreased by 28% to 99% compared to other designs.

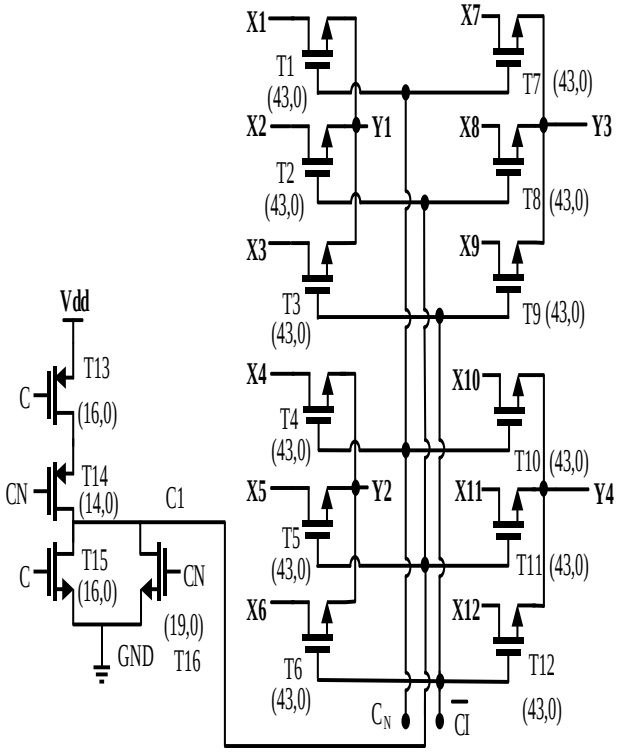

Fig. 13: The structure of MUX 12*4 used in the proposed QFA2.

Conclusion

Applying MVL logic with CNTFET transistors speeds up computational circuits and decreases the chip size. In this paper, the new method Multiplexers Quaternary logic is designed.

The results showed that the use of these multiplexers in the design of full adders reduced the number of transistors used by 27% to 54% compared to base full adders.

Also, the other results showed a reduction in average energy consumption (by a minimum of 20% and a maximum of 99.5%) and PDP (29.25% to 98.94%).

These results may be of promising value for benefiting from nanotechnology. Finally, according to the results of the application of quaternary multiplexers in the construction of adders, it is possible to suggest the construction of processor circuits and fast and low-consumption arithmetic circuits based on nano transistors and multiplexers.

Also Multi-value multiplexer technology can be used to design telecommunication transmission lines and data networks for new generations of mobile phones.

Author Contributions

S.Rahmati and E. Farshidi conceptualized the research. S.Rahmati designed the experiments and collected the data. S.Rahmati carried out the data analysis. E. Farshidi and J.Ganje validated the results. S.Rahmati wrote the manuscript. E. Farshidi and J.Ganje reviewed and edited the manuscript.

Table 9: Comparison of quaternary full adder performance

C-Load= 0e-15fF	Power (uw)	Delay (ps)	PDP (e-16J)	Transistor count	Power Supply count
Proposed 1 (FA)	0.7064	48.33	0.3414	93	1
Proposed 2 (FA)	0.7115	53.6	0.3713	113	1
Design 1 [14]	0.212	46.71	0.099	137	3
Design 2 [14]	0.884	43.88	0.387	157	1
[12]	2.467	71.72	1.178	195	1
[6]	75.34	112.7	84.95	163	1
Design 1 [15]	137.5	114.7	157.5	788	3
Design 2 [15]	57.73	71.54	41.25	154	1
		C-Load= 2e-15fF			
Proposed 1 (FA)	0.9745	95.5	0.9306	93	1
Proposed 2 (FA)	1.216	109.67	1.33	113	1
Design 1 [14]	0.453	407.2	1.844	137	3
Design 2 [14]	1.161	665.0	7.721	157	1
[12]	2.657	107.9	2.871	195	1
[7]	102.4	122.3	125.3	163	1
		C-Load= 0.7e-15fF			
Proposed 2 (FA)	0.986	42.53	0.4193	113	1
[19]	1.73	38.13	0.6596	212	1

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Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

Abbreviations

MVL	Multi-Valued Logic
MUX	Multiplexer
PDP	Power Delay Product
CMOS	Complementary Metal-Oxide-Semiconductor
CNTFET	Carbon NanoTube Field Effect Transistors
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IQI	Intermediate Quaternary Invert
NQI	Negative Quaternary Invert
PQI	Positive Quaternary Invert
SQI	Standard Quaternary Standard Invert
QHA	Quaternary Half Adder
QFA	Quaternary Full Adder

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Research paper

Utilization of CHB Multilevel Inverter for Harmonic Reduction in Fuzzy Logic Controlled Multiphase LIM Drives

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Abstract

Background and Objectives: Despite superior privileges that multiphase motors offer in comparison with their three-phase counterparts, in the field of multiphase linear induction motors (LIMs) few studies have been reported until now. To combine the advantages of both multiphase motors and linear induction motors, this paper concentrates on multiphase LIM drives considering the end effects.

Methods: The main contributions of this paper can be divided into two major categories. First, a comparative study has been conducted about the dynamic performance of Fuzzy Logic Controller (FLC) and Genetic-PI controller for a seven-phase LIM drive; and second, because of the superior performance of the FLC method revealed from the results, the harmonic pollution of the FLC based LIM drive has been studied in the case of supplying through a five-level Cascaded H-bridge (CHB) VSI and then compared with the traditional two-level VSI fed one.

Results: The five-level CHB-VSI has utilized a multiband hysteresis modulation scheme and the two-level VSI has used the traditional three-level hysteresis modulation strategy. Note that for harmonic distortion assessment both harmonic and interharmonic components are considered in THD calculations.

Conclusion: The results validate the effectiveness of the proposed FLC for seven-phase LIM drive supplied with five-level CHB-VSI and guarantee for perfect control characteristics, lower maximum starting current, and significant harmonic and interharmonic reduction.

Introduction

From the beginning of this century, multiphase motor drives have attracted worldwide attention due to the significant advantages they have in comparison with three-phase motors [1]. The predominant benefits of using multiphase machines are greater torque density, increase in efficiency, lower torque pulsation, higher fault tolerance, and lower required rating per inverter leg (which results in simpler and more reliable power electronics devices) [2]. Furthermore, multiphase motors possess additional degrees of freedom by which more than one motor can be independently controlled through a single Voltage Source Inverter (VSI) [2]-[4]. For this purpose, the stator windings of the motors must have an appropriate connection style [2]-[4]. The dominant advantage of this concept is that the number of inverter legs decreases.

Although this idea is appropriate for all types of multiphase AC machines, until now, the most research interests in the area of multiphase machines are

concentrated on AC rotational machines [1]-[12]. Consequently, in this paper, an attempt is made to provide a survey in control of multiphase LIMs with more than three phases.

Additionally, Linear Induction Motors (LIMs) are extensively utilized in industrial applications and high-speed transportation systems because of the significant privileges they offer. Nevertheless, accurate modeling of these machines is more complicated than the rotational induction ones due to the end effects [13]-[16].

A famous per-phase model of the LIM was proposed by Duncan [17]. This model was extracted by appropriate modification of the traditional rotary induction machine model. To reflect the end effects, the magnetizing branch was suitably modified [17]. Despite the usefulness and simplicity of this model, it was not directly applicable to drive applications. In [18] using Duncan's equivalent circuit model and regarding the end effect phenomena, the dynamic model of the three-phase LIM was suggested. Nevertheless, the end effect has been just regarded in the direct-axis equivalent circuit. The quadrature-axis equivalent circuit of the motor has been considered the same as a RIM with no end effect. However, it is explicit that for precise modeling of a LIM, both direct and quadrature axes must be affected by the end effect. Six years later, the second author of [18] introduced another dynamic model for three-phase LIM including the end effect in both direct and quadrature axes of the model [19]. In [20], regarding the end effect phenomena, the dynamic model of multiphase LIM has been derived for more than three phases. This model has been extracted by choosing an arbitrary rotating reference-frame and utilizing Park's transformation. On the other hand, among various control techniques accomplished on the LIM, Indirect Field Oriented Control (IFOC) method is an approved control strategy abundantly utilized for LIM drive applications [19]-[23]. The principal concept behind IFOC of a LIM is based on the alliance of the secondary flux vector with the direct-axis, which leads to the decoupling of flux and thrust [19]-[23]. To achieve this, the component of secondary flux along the quadrature-axis must be set to zero. Furthermore, the component of secondary flux along the direct-axis must be fixed on the nominal secondary flux value.

Moreover, in the past decade, multi-level inverters (MLIs) have been extensively utilized due to their particular privileges in power quality improvement [24]-[25]. The principal preferences of MLIs are lower voltage stress (dv/dt) on power electronic switches and reduced voltage harmonics of the VSI.

Therefore, it would be an interesting idea to use multilevel inverters for supplying LIM drives. An investigation of various topologies and control methods for multilevel inverters is presented in [24]-[25]. Cascaded H-bridge (CHB) inverter is a well-known multilevel structure utilized in high-power Medium-Voltage (MV) drives. The CHB inverter, in comparison with other multilevel inverters, has a simpler and modular topology. In recent years, CHB-VSIs have been extensively utilized in electrical motor drive applications due to their prominent benefits in the reduction of harmonic contents and power quality enhancement [26]-[29]. A multiband hysteresis switching scheme for current control of CHB-VSIs has been suggested in [30]. Implementation of current control using the hysteresis method is simple and has a fast dynamic response [30]. Also, it shows suitable robustness performance. Moreover, to calculate the hysteresis bandwidth with respect to the CHB switching frequency, a frequency-domain strategy has been proposed [30]. As a result, the CHB multilevel inverter has been selected in this paper for supplying the multiphase LIM drive. According to above mentioned, the principal scope of this paper is to investigate the harmonic reduction of Fuzzy Logic Controlled (FLC) multiphase LIM drive fed through a five-level CHB-VSI in comparison with the traditional two-level VSI. The remainder of this paper is organized as follows. In the next section, the dynamic model for the n-phase LIM is presented considering the end effect phenomena in the magnetizing branch inductance. Then, the indirect field-oriented control of n-phase LIM regarding the end effect is demonstrated. Next, the CHB-VSI with multiband hysteresis switching scheme is illustrated. After that, the calculation of the Total Harmonic Distortion (THD) factor considering harmonic and interharmonic components will be discussed. The overall control system, the Genetic-PI based controller, and the fuzzy logic controller will be introduced in the next sections, respectively. Subsequently, the simulation results are provided for a seven-phase LIM drive. Finally, the conclusions are given.

Dynamic Modeling of The LIM Considering The End Effect

The per-phase model of a LIM developed by Duncan is depicted in Fig. 1.

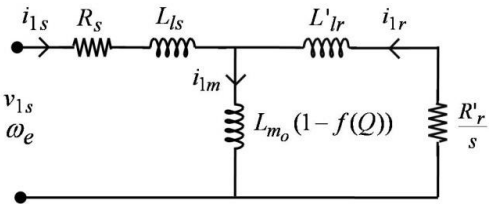

Fig. 1: The per-phase equivalent circuit model of LIM.

To take into account the end effect, a dimensionless factor Q and a function $f(Q)$ are defined as follows [17], [31]:

$$Q \cong \frac{D.R'_r}{L'_r.v_r} \quad (1)$$

$$f(Q) = \frac{\left(1-e^{-Q}\right)}{Q} \quad (2)$$

where D and v_r are the LIM length and speed, respectively. L'_r and R'_r are the self-inductance and resistance of the secondary, respectively.

Accordingly, the magnetizing branch is changed to $L_{m_0}(1-f(Q))$, in which L_{m_0} is the magnetizing inductance when the LIM speed is equal to zero [17].

By applying the Park's transformation to Duncan's model, the dynamic model of an n-phase LIM can be extracted as follows [20]:

Primary voltage equations:

$$\begin{aligned} v_{qs} &= R_s i_{qs} + \omega\lambda_{ds} + p\lambda_{qs} \\ v_{ds} &= R_s i_{ds} - \omega\lambda_{qs} + p\lambda_{ds} \\ v_{x1s} &= R_s i_{x1s} + p\lambda_{x1s} \\ v_{y1s} &= R_s i_{y1s} + p\lambda_{y1s} \\ &\vdots \\ v_{0s} &= R_s i_{0s} + p\lambda_{0s} \end{aligned} \quad (3)$$

Secondary voltage equations:

$$\begin{aligned} v_{qr} &= R'_r i_{qr} + (\omega-\omega_r)\lambda_{dr} + p\lambda_{qr} = 0 \\ v_{dr} &= R'_r i_{dr} - (\omega-\omega_r)\lambda_{qr} + p\lambda_{dr} = 0 \\ v_{x1r} &= R'_r i_{x1r} + p\lambda_{x1r} = 0 \\ v_{y1r} &= R'_r i_{y1r} + p\lambda_{y1r} = 0 \\ &\vdots \\ v_{0r} &= R'_r i_{0r} + p\lambda_{0r} = 0 \end{aligned} \quad (4)$$

Primary flux linkage equations:

$$\begin{aligned} \lambda_{qs} &= L_{ls} i_{qs} + L_m\{1-f(Q)\}(i_{qs}+i_{qr}) \\ \lambda_{ds} &= L_{ls} i_{ds} + L_m\{1-f(Q)\}(i_{ds}+i_{dr}) \\ \lambda_{x1s} &= L_{ls} i_{x1s} \\ \lambda_{y1s} &= L_{ls} i_{y1s} \\ &\vdots \\ \lambda_{0s} &= L_{ls} i_{0s} \end{aligned} \quad (5)$$

Secondary flux linkage equations:

$$\begin{aligned} \lambda_{qr} &= L'_{lr} i_{qr} + L_m\{1-f(Q)\}(i_{qs}+i_{qr}) \\ \lambda_{dr} &= L'_{lr} i_{dr} + L_m\{1-f(Q)\}(i_{ds}+i_{dr}) \\ \lambda_{x1r} &= L'_{lr} i_{x1r} \\ \lambda_{y1r} &= L'_{lr} i_{y1r} \\ &\vdots \\ \lambda_{0r} &= L'_{lr} i_{0r} \end{aligned} \quad (6)$$

where $p \equiv d/dt$ and ω_r denotes the secondary angular speed. Also, ω-ω_r represents the slip angular frequency ($\omega - \omega_r \equiv \omega_{sl}$).

The LIM thrust can be expressed as [20]:

$$F = \frac{n}{2}\frac{\pi}{\tau}\left(\lambda_{qr} i_{dr} - \lambda_{dr} i_{qr}\right) \quad (7)$$

in which τ represents the motor pole pitch.

Indirect Field-Oriented Control of LIM Considering End Effects

The main idea behind the IFOC of a LIM is based on aligning the reference frame to the secondary flux vector, which results in the decoupling of flux and thrust. Consequently, the component of secondary flux along the quadrature-axis must be set to zero. In other words, the secondary flux vector should be aligned with the direct-axis and its value must be fixed on the nominal secondary flux value. It follows that [20]:

$$\lambda_{qr} = 0 \quad \text{and} \quad \frac{d\lambda_{qr}}{dt} = 0 \quad (8)$$

Supposing $v_{qr} = v_{dr} = 0$, the slip angular frequency ($\omega_{sl} \equiv \omega_e - \omega_r$) will be calculated using (4) and (6) and by omitting the i_{qr} as:

$$\omega_{sl} = R'_r \left[\frac{1-f(Q)}{\frac{L'_{lr}}{L_m} + (1-f(Q))}\right] \times \frac{i_{qs}}{\lambda_{dr}} \quad (9)$$

Using (4) and (6) and by omitting i_{dr}, the direct-axis secondary flux (λ_{dr}) will be calculated:

$$\lambda_{dr} = \frac{L_m(1-f(Q))}{1 + \left\{\frac{L'_{lr} + L_m(1-f(Q))}{R'_r}\right\} p} \times i_{ds} \quad (10)$$

It is notable that supposing $v_r \approx 0$ and $f(Q) \approx 0$, will result in $\omega_{sl} \approx R'_r L_m i_{qs} / (L'_r \lambda_{dr})$ and $\lambda_{dr} \approx L_m i_{ds} / \left(1 + \left(L'_r / R'_r\right) p\right)$ (where $L'_r = L'_{lr} + L_m$), which are in accordance with rotary induction motors. The LIM thrust could be written as [20]:

$$F = \frac{n}{2}\frac{\pi}{\tau}\frac{L_m(1-f(Q))}{L'_{lr} + L_m(1-f(Q))}\lambda_{dr} i_{qs} \quad (11)$$

Cascaded H-Bridge Multilevel Inverter With Multiband Hysteresis Switching Scheme

In Fig. 2, the basic structure of a single-phase five-level CHB-VSI is illustrated with two cascaded H-Bridge (HB) cells. Each of the semiconductor switching devices S_{11}, S_{12}, …, S_{22} represents an IGBT with back-to-back diode. The CHB-VSI output voltage can be written as $V_c = u(t) \times V_{dc}$, in which $u(t)$ is the output logic signal including five different levels. In Fig. 3 the flowchart of five-band hysteresis switching scheme is represented. In this figure, the current error is defines as $C_e = i_s - i_s^*$, in

which i_s and i_s^* represent the actual and reference phase currents, respectively. Also, h denotes the hysteresis band. The modulation scheme produces five voltage levels, i.e. u = -1, -1/2, 0, +1/2, +1.

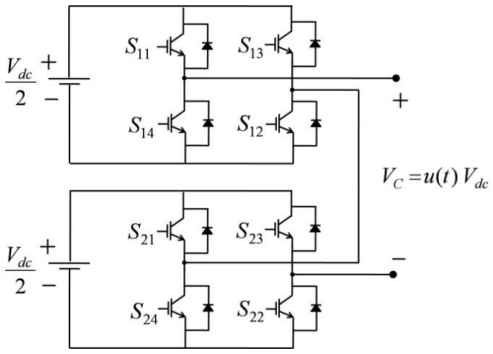

Fig. 2: Five-level CHB-VSI.

For an n-phase voltage source inverter with n-phase balanced load, the instantaneous values of phase-to-neutral voltages (V_1 , …, V_n) can be written as a function of DC bus voltage V_{dc} and logic variables (u_1, …, u_n) as:

$$\begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_{n-1} \\ v_n \end{bmatrix} = \frac{V_{dc}}{n} \begin{bmatrix} n-1 & -1 & -1 & \cdots & -1 \\ -1 & n-1 & -1 & \cdots & -1 \\ -1 & -1 & \ddots & \cdots & -1 \\ \vdots & \vdots & \cdots & \vdots & \vdots \\ -1 & -1 & \cdots & n-1 & -1 \\ -1 & -1 & \cdots & -1 & n-1 \end{bmatrix}_{n\times n} \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ \vdots \\ u_{n-1} \\ u_n \end{bmatrix} \quad (12)$$

For a five-level CHB-VSI, each logic variable (u_1,… , u_n) has five levels of output, i.e. u_i = -1, -1/2, 0, +1/2, +1, according to the five-band hysteresis switching flowchart.

Harmonic and Interharmonic Distortion

Generally, power quality evaluations are performed on periodic voltages and current waveforms. The defined criteria are usually expressed with regard to the harmonic and fundamental components of the waveforms. Unfortunately, currents waveforms in many industrial loads are not periodic. For instance, the current waveform generated by the hysteresis modulation possesses (except the fundamental sinusoidal component), random and stochastic components that are irregular and non-periodic. Consequently, the custom power quality criteria which are defined based on the periodicity of the signals, could not be utilized. Nevertheless, in the past decade, considerable research has been concentrated on solving this issue [32]. Analyzing non-periodic loads is mostly based on the time windows utilized for extracting statistical data to achieve an overall characteristic. The IEC 61000-4-30 recommends a window width of about 200ms, which corresponds to 10 cycles on 50 Hz systems and 12 cycles on 60 Hz systems [32].

According to the IEC 61000-4-30, considering a 200ms time window is appropriate [32]. This window width is 10 cycles on 50 Hz systems and 12 cycles on 60 Hz systems. The stochastic nature of controller operation dictates that the hysteresis modulation will result in harmonic, interharmonic, and subharmonic distortion. Unlike harmonics which are located on multiples of the fundamental frequency, interharmonics and subharmonics take place at non-integer multiples of the fundamental frequency.

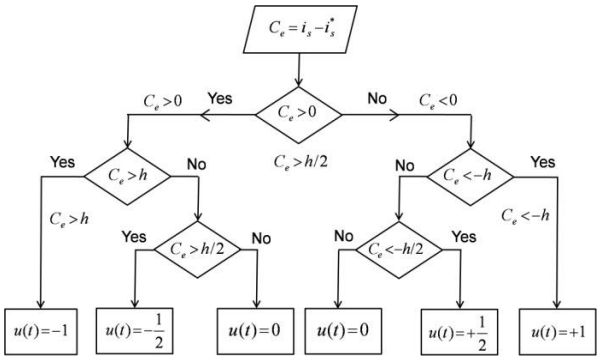

Fig. 3: Flowchart of the five-band hysteresis modulation.

Interharmonics and subharmonics take place at non-integer multiples above or below the fundamental frequency, respectively. To avoid complexity, in the remainder of this work, interharmonics and subharmonics are classified into a single group, called interharmonic distortion.

It is notable that for calculating the Total Harmonic Distortion (*THD*), when interharmonics exist, two components should be considered [32]:

$$THD = \sqrt{TDHD^2 + TIHD^2} \quad (13)$$

TDHD and *TIHD* denote the total discrete harmonic distortion and the total interharmonic distortion, respectively. For a current signal, *TDHD* and *TIHD* are written as [32]:

$$TDHD_I = \frac{\sqrt{\sum_{m=2}^{m_{max}} I_m^2}}{I_1} \quad (14)$$

$$TIHD_I = \frac{\sqrt{\sum_{m=0}^{m_{max}-1} IRSS_{m,m+1}^2}}{I_1} \quad (15)$$

where m is the harmonic order and m_{max} represents the maximum harmonic order. I_1 is the fundamental value of current waveforms. *IRSS* is the root sum squared value of the current interharmonics which are located between two consecutive harmonics m and m+1 [32]. If the LIM drive operates at a frequency of f_1, by considering a

frequency resolution of Δ*f*, the *IRSS* can be determined as [32]:

$$IRSS_{m,m+1}=\sqrt{\sum_{f=f_1\cdot m+\Delta f}^{f_1\cdot(m+1)-\Delta f} IRSS_{m,m+1}^{2}} \quad (16)$$

Consequently, for a current waveform including harmonics and interharmonics, the equivalent *THD* index ($THD_{e\text{-}I}$) is defined as [32]:

$$THD_{e-I}=\frac{\sqrt{\sum_{m\neq 1}^{m_{max}} I_m^{\,2}+\sum_{m=0}^{m_{max}-1}\sum_{f=f_1\cdot m+\Delta f}^{f_1\cdot(m+1)-\Delta f} I_m^{\,2}}}{I_1} \quad (17)$$

where I_m denotes the rms values of the current harmonics and interharmonics. For voltage waveforms, the equivalent *THD* index ($THD_{e\text{-}V}$) can be calculated in the same way.

Control System

The total IFOC diagram of the n-phase LIM drive is demonstrated in Fig. 4. The LIM is fed through CHB-VSI based multiband hysteresis switching strategy. The end effect is regarded in the LIM model and the controller. A current control loop and a speed control loop are included in the LIM drive. In this work, both genetic-PI based controller and fuzzy Logic Controller are utilized as regulators in the speed control loop.

In this work, both genetic-PI based controller and fuzzy Logic Controller are utilized as regulators in the speed control loop.

The command quadrature-axis primary current (i_{qs}^*) is produced by the speed controller. Also, the command direct-axis primary current (i_{ds}^*) is produced according to the nominal direct-axis secondary flux (λ_{dr}^*) and the LIM speed. Moreover, the gains K_1 and K_2 are calculated from (9) and (10). Note that K_1 and K_2 are dependent on $f(Q)$ and thus dependant on the LIM speed [33]. The command currents (i_{1s}^*, i_{2s}^*, …, i_{ns}^*) are produced using i_{qs}^* and i_{ds}^* and by applying inverse Park's transformation. The current controller produces the firing pulses for the CHB-VSI switches. For reducing the harmonic and interharmonic distortion of the multiphase LIM drive, a five-level CHB-VSI (with two HB cells) has been unutilized and compared with the conventional two-level VSI.

The current controller produces the firing pulses for the CHB-VSI switches. For reducing the harmonic and interharmonic distortion of the multiphase LIM drive, a five-level CHB-VSI (with two HB cells) has been unutilized and compared with the conventional two-level VSI.

Genetic-PI Based Controller [34]

Genetic Algorithm (GA) is a well-known optimization method, inspired by the populations evolve in nature. In this paper, GA has been utilized for optimizing the PI gains of the speed controller.

For GA implementation, the roulette-wheel selection function has been used. Moreover, the two-point crossover with a probability of 0.80 is chosen.

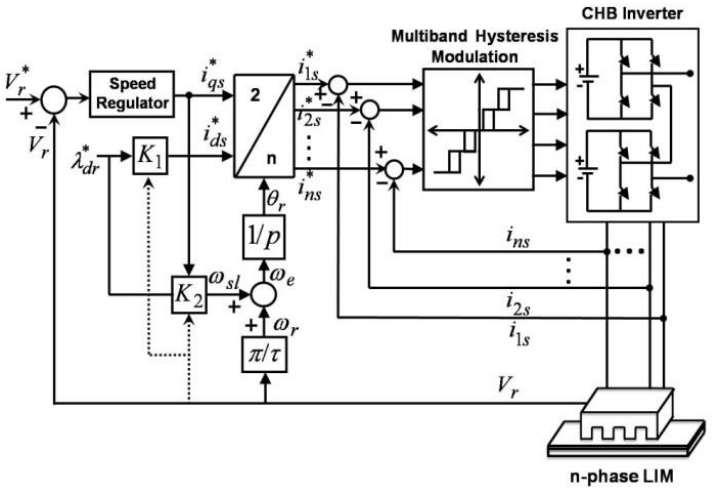

Fig. 4: Block diagram of the proposed IFOC scheme for n-phase LIM.

To avoid local minimum answers, the adaptive feasible mutation has been selected. Furthermore, the population size is considered 200 chromosomes for each generation.

The objective function, which must be minimized, is the sum of different functions. In this paper, rise time, settling time, maximum overshoot, steady-state error, and load change error are taken into account in the objective function, as follows [34]:

$$F_{obj}=k_1.F_{obj_1}+k_2.F_{obj_2}+k_3.F_{obj_3}+k_4.F_{obj_4}+k_5.F_{obj_5} \quad (18)$$

where $F_{obj_1}=\frac{T_r}{M_T}+P$

$F_{obj_2}=\frac{T_S}{M_T}+P$ $\quad$ $F_{obj_3}=\frac{M_p}{M_E}+P$

$$F_{obj_4}=\frac{|E_{SS}|}{M_E}+P \qquad F_{obj_5}=\frac{|F_L|}{M_L}+L \tag{19}$$

k_1 to k_5 are the importance coefficients and are chosen as: $k_1=k_2=k_3=k_4=k_5=1$. E_{SS}, M_P, T_r, and T_S denote the steady-state error, the overshoot, the rise time, and the settling time, respectively. The constants M_T, M_E, and M_L are scaling factors. In this research, these constants are considered as $M_T = t_{final}$, $M_E = y_d$, $M_L = 1$ (t_{final} and y_d denote the total time and the desired LIM speed, respectively). P and L are penalty factors that must be set to zero in case of a stable speed response. Moreover, to minimize the effect of load variations on the speed response, the load change error is also considered to the objective function as $F_L=y_{(t_{final})}(full-load)-y_{(t_{final})}(no-load)$. For small load change errors, penalty factor L is set to zero and for high error values, it is considered 8. If the LIM speed becomes unstable or deficient, the parameters are selected according to Table 1 [34].

Finally, as the main goal of this paper is controlling the LIM drive in the whole speed range, the final objective function optimized by GA is considered as:

$$F_{obj_{Total}}=F_{obj}(V_r=V_{rated})+F_{obj}(V_r=\frac{V_{\max}}{2}) \tag{20}$$

In the Appendix, the optimized PI controller gains obtained from GA are given. Moreover, the best objective functions in each generation, during the GA optimization process, are captured and demonstrated in the Appendix.

Table 1: Parameters of the objective function in deficient and unstable conditions [34]

	E_{ss}	T_S	T_r	M_P	P
Deficient condition	$y_d-y_{(t_{final})}$	M_T	M_T	0	7
Unstable condition	y_d	M_T	T_r	y_d	10

Fuzzy Logic Controller (FLC)

In Fig. 5, the total IFOC diagram of the multiphase LIM drive with FLC is demonstrated. The linguistic variables of FLC are selected according to the LIM model [23]. The speed error $\Delta V_r(n)$ and the change of speed error $\Delta e(n)$ are considered as the inputs of the FLC. The output variable is the command LIM force ($F_e^*(n)$).

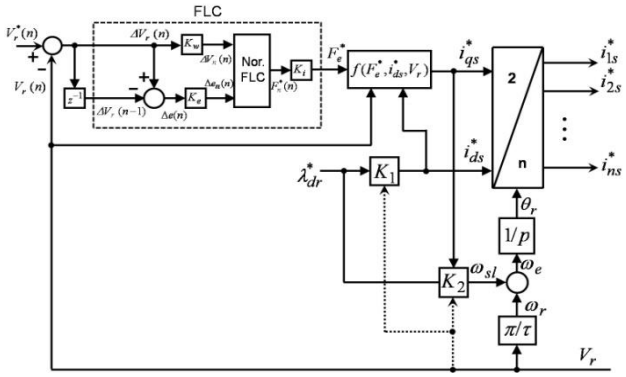

Fig. 5: Block diagram of the proposed FLC for IFOC of n-phase LIM.

Correspondingly, the command quadrature-axis current (i_{qs}^*) will be produced using (11). In the next step, the scaling factors K_ω, K_e, and K_i are chosen by trial-and-error to get optimal drive performance.

For FLC implementation, the Mamdani-type fuzzy inference approach and the center of gravity defuzzification method are used [23].

The FLC rules, used in this work, are as follows [23]:

If ΔV_n is PH (Positive High), then F_e^* is PH.

If ΔV_n is ZE (Zero) and Δe is PO (Positive), then F_e^* is PL.

If ΔV_n is ZE and Δe is NE (Negative), then F_e^* is NC (No Change).

If ΔV_n is ZE and Δe is ZE, then F_e^* is NC.

If ΔV_n is NL (Negative Low), then F_e^* is NL.

If ΔV_n is NH (Negative High), then F_e^* is NH.

The membership functions of FLC are illustrated in Fig. 6.

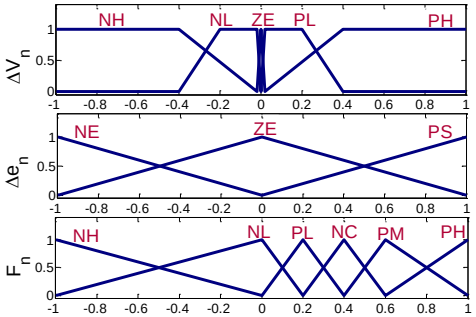

Fig. 6: Fuzzy logic membership functions; speed error ΔV_n, speed error change Δe_n, command LIM thrust $F_{en}^*(n)$.

Results and Discussion

To investigate the functionality of the proposed FLC of LIM drive with the end effect considerations, different tests have been performed at various operating points. The validity of the suggested LIM model combined with the relevant controller is evaluated by simulating a seven-phase LIM drive. The seven-phase LIM is fed through a five-level CHB-VSI with a five-band hysteresis switching technique. The performance validation of the FL controller and Genetic-PI Based controller have been evaluated and compared with each other. The speed and current responses have been monitored under various operating situations such as abrupt changes in reference speed, step changes in load, and also at various reference speeds and loads. The simulation of the complete drive has been executed utilizing Matlab/Simulink software with the parameters expressed in the Appendix. Furthermore, the power quality improvement of the seven-phase LIM drive supplied with five-level CHB-VSI is studied and compared with the traditional two-level VSI. For this purpose, the THD index has been evaluated for both inverter topologies considering both harmonics and interharmonics. Some of the achieved results are presented in the following paragraphs.

In the CHB-VSI, a net dc-link voltage of $V_{dc}=90V$ is considered for each HB cell. Also, a hysteresis band of $h\approx 0.1A$ is applied.

The FL controller gains are chosen to achieve the best transients and dynamic responses considering the requirement of stability. The command speed and dynamic speed response of the LIM drive for Genetic-PI and FL controllers are demonstrated in Figs. 7 (a)-(b), respectively. First, the LIM is driven at 0.5 m/sec command speed and with no external force. At t=3 sec, the command speed is suddenly increased from 0.5 to 1.5 m/sec. At t=6 sec, a 100 N external force is applied to the LIM. At t=9 sec, the command speed is suddenly decreased from 1.5 to 1 m/sec while keeping constant the external force at 100 N. The external force applied to the motor primary is decreased at t=12 sec from 100 N to 50 N. Despite optimum adjusting of PI constants utilizing GA, the FLC showed better performance from the viewpoint of dynamic response time, overshoot, and adaptability to external force changes.

Figs. 8 (a)-(b) illustrate the corresponding LIM primary phase currents for PI and FL controllers, respectively. From these figures, the maximum starting current for PI and fuzzy are equal to 6.64 A and 3.96 A, respectively. As a result, it is clear that FLC has lower starting current in comparison with PI controller, which increases the motor ability and decrease the inverter rating.

Furthermore, a quantitative comparison of some dynamic response parameters for the aforementioned control methods is illustrated in Table 2 for a command speed of 1.5 m/sec.

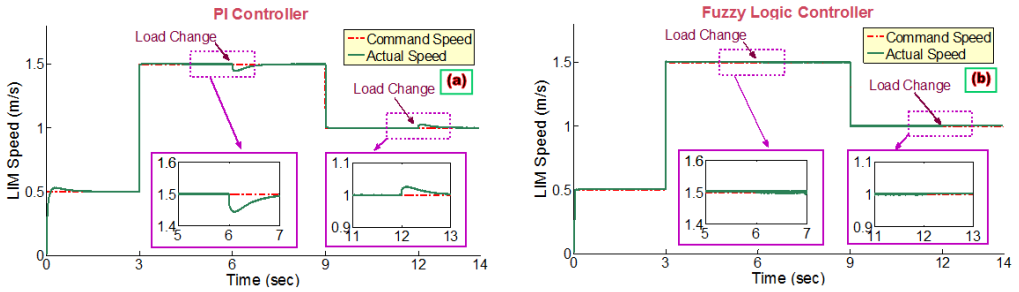

Fig. 7: Command speed and actual speed of the LIM drive; (a) Genetic-PI controller and (b) Fuzzy logic controller.

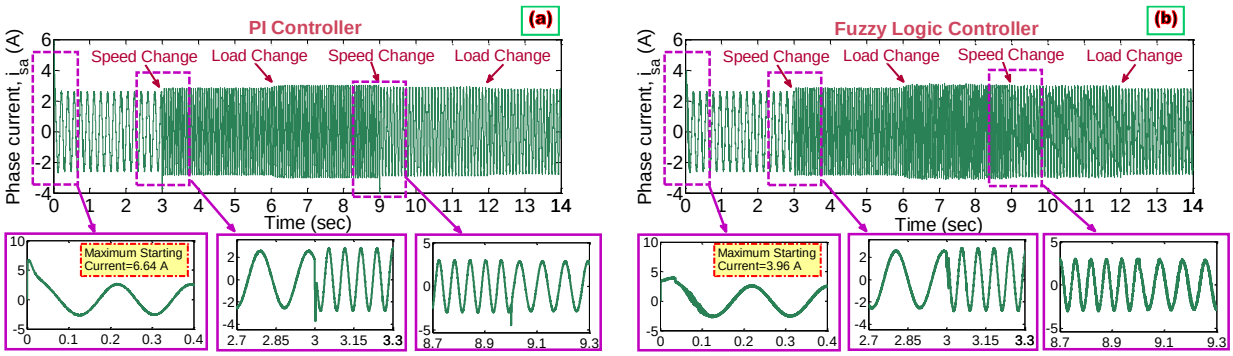

Fig. 8: Primary current of the LIM drive; (a) Genetic-PI controller and (b) Fuzzy Logic controller.

According to the results, it is obvious that in the FLC of multilevel LIM drive, the actual LIM speed tracks the command speed under various loading conditions. Moreover, it offers more accurate dynamic responses,

which makes it suitable for high performance drive applications.

Table 2: Dynamic response parameters of Genetic-PI and Fuzzy Logic Controller

		I_{strat} [A]	E_{ss} [%]	M_P [%]	T_r [sec]
No-Load	Genetic-PI	0.11	3%	0.06	8.98
	Fuzzy	0.06	0	0.06	4.47
F_L=100N	Genetic-PI	0.25	0.2	0.03	8.98
	Fuzzy	0.09	0	0.03	4.53
F_L=150N	Genetic-PI	1.5	0	≈ 0	8.98
	Fuzzy	0.11	0	≈ 0	4.57

In the next step, the THD index of the seven-phase LIM drive supplied with five-level CHB-VSI with five-band hysteresis modulation is studied and compared with the traditional two-level VSI. THD index has been evaluated for both topologies considering both harmonic and interharmonic components.

Unlike power system analysis in which the power frequency is almost considered constant (i.e. 50 Hz), in variable speed drives the inverter frequency is variant and dependent on the reference speed and external loading condition. Thus, at first, the fundamental frequency should be computed. Then, according to the fundamental frequency, the harmonic and interharmonic components should be extracted from the frequency spectrum of the signal. Consequently, the THD index can be calculated from (17). For harmonic analysis and evaluation of the fundamental component (frequency and amplitude), a time window equal to 10 seconds (in steady-state operating condition) has been considered to achieve 0.1 Hz frequency resolution. The time step of the simulation (the data sampling time) has been considered equal to 50 microseconds. For THD calculations, THD parameters were calculated using time windows with the length of 10 cycles of the fundamental frequency (f_1) according to the IEC 61000-4-30 standard [35]. Thus, the frequency resolution will be equal to 1/TW (where TW=10/f_1 is time window length). In this paper, harmonics and interharmonics were calculated utilizing Fast Fourier Transform (FFT) on the time domain waveforms obtained from the simulation. Total simulation time of 14 seconds has been considered to have more accurate THD values with higher precision. Afterward, the results of the first 3 seconds (from 14 seconds) were omitted to guaranty the steady-state operation of the drive. Then, the remaining 11 seconds have been divided into time windows (9 or 10 time windows depending on f_1). Each window length was considered equal to 10 times of f_1 according to the IEC 61000-4-30 [35]. Consequently, for each waveform different THD values related to the different time windows have been extracted and the minimum, maximum, and mean of THD values have been recorded.

In Fig. 9 (a), the seven-phase LIM phase current and phase voltage supplied with five-level CHB-VSI (for h=0.5 A) at 1.5 m/s command speed and 100 N external force are shown. Similarly, the seven-phase LIM phase current and phase voltage supplied with the traditional two-level VSI for the same operating conditions is presented in Fig. 9 (b). It is obvious that in LIM drive fed through the CHB-VSI, waveforms are more sinusoidal in comparison with the ones fed through the two-level VSI. In Addition, for h=0.5 A, the average switching frequency (f_s) of the CHB and traditional VSI semiconductor switching devices are computed and illustrated in these figures which are equal to 206 Hz and 86 Hz, respectively. By decreasing the hysteresis band, the average switching frequency will increase. For h=0.1 A, the average switching frequency of the CHB and traditional VSI switching devices are 1594 Hz and 290 Hz, respectively

Figs. 10 (a)-(b) display the frequency spectrums of the LIM phase voltage for both CHB-VSI and traditional VSI. To show more clearly the frequency spectrum, the spectrums are depicted separately for both lower frequency components (top figure) and higher frequency components (bottom figure). Similarly, the frequency spectrums of the LIM phase current for both CHB and traditional VSI are illustrated in Figs. 11 (a)-(b). From these figures, the LIM phase voltage THD values for CHB and traditional VSI are equal to 28.01% and 45.90%, respectively. Correspondingly, the phase current THD values for CHB and traditional VSI are equal to 4.74% and 8.73%, respectively.

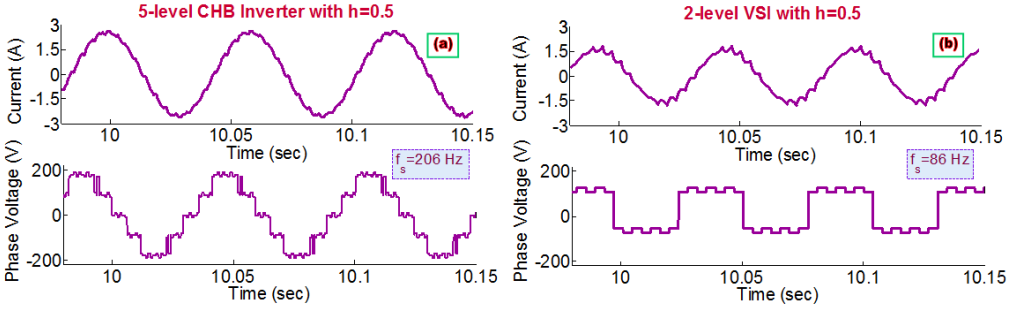

Fig. 9: The LIM phase current and phase voltage; (a) five-level CHB-VSI (b) two-level voltage source inverter.

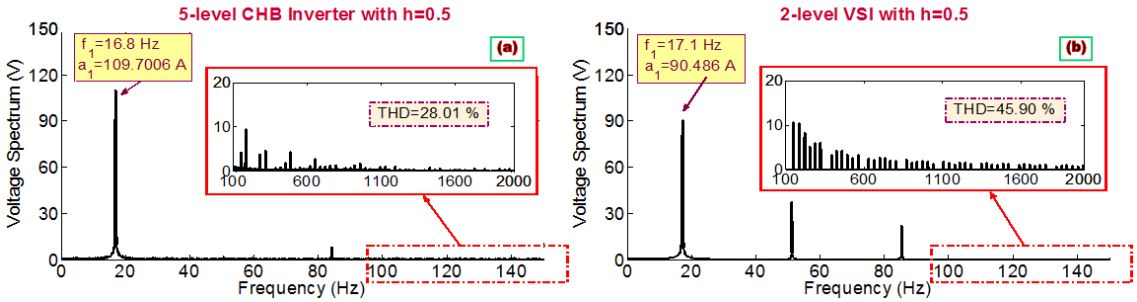

Fig. 10: The frequency spectrum of the seven-phase LIM phase voltage; (a) five-level CHB-VSI (b) two-level voltage source inverter.

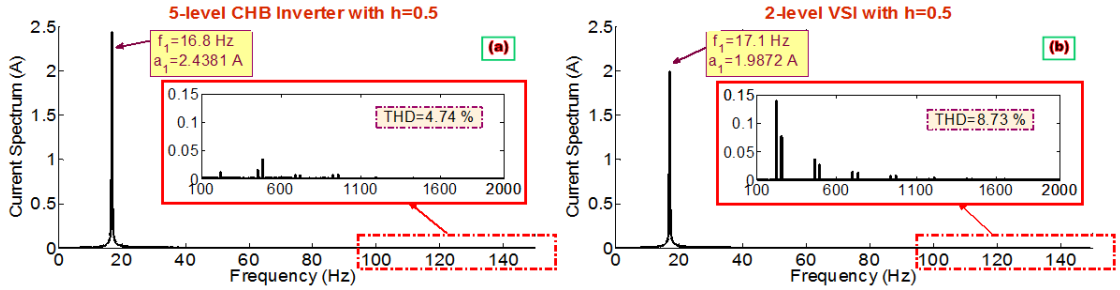

Fig. 11: The frequency spectrum of the seven-phase LIM current; (a) five-level CHB-VSI (b) two-level voltage source inverter.

It is clear from the figures that the magnitudes of harmonic and interharmonic components caused by the five-level CHB-VSI are significantly reduced in comparison with the two-level VSI. The THD indices of the LIM phase voltages and phase currents are computed for the CHB and the traditional VSI, different hysteresis bands, and different external forces. The seven-phase LIM drive was running with 0.9 m/sec command speed. Figs. 12-13 represent the THD indices of the LIM phase voltage and currents for The CHB and the traditional VSI, different hysteresis bands, and different external forces. Furthermore, the value of the calculated THD indices (in percent) and the fundamental component (amplitude and frequency) of the LIM phase voltages and currents are summarized in the Appendix.

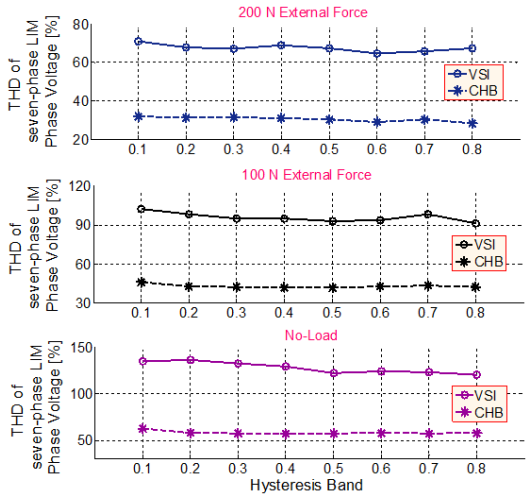

Fig. 12: Comparison of THD values [%] of the seven-phase LIM phase voltage supplied with five-level CHB and two-level VSI for different hysteresis bands and different external forces.

It is perceptible from the results that harmonic and interharmonic contents resulted from the five-level CHB-VSI are remarkably less than the traditional two-level VSI. Furthermore, generally by increasing the hysteresis band and by decreasing the external forces, the THD values will increase. It should be noted that if interharmonics are considered in THD calculations, the THD indices may have high values and even more than 100% in highly distorted conditions.

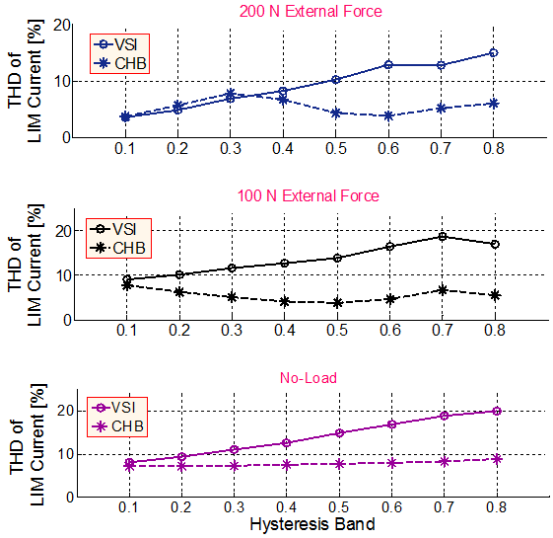

Fig. 13: Comparison of THD values [%] of the seven-phase LIM phase current supplied with five-level CHB and two-level VSI for different hysteresis bands and different external forces.

According to the results, it is evident that the FLC of seven-phase LIM drive offers perfect dynamic characteristics including fast and accurate speed

response, which is also adaptive to the imposed external forces. Furthermore, the application of five-level CHB-VSI with five-band hysteresis modulation guarantees for lower THD indices and power quality improvement of the seven-phase LIM drive.

Conclusion

This paper presents a comparative study between the five-level Cascaded H-bridge (CHB) inverter and the traditional two-level VSI on the harmonic content of the multiphase linear induction motor drive with Fuzzy Logic Controller (FLC). Due to the existence of current a control loop in the multiphase LIM drive controlling diagram, the five-level CHB-VSI has utilized a multiband hysteresis modulation scheme and the two-level VSI has used the traditional three-level hysteresis modulation strategy. Since current waveforms generated by the hysteresis modulations possess random and stochastic components (except the fundamental sinusoidal component), the THD indices have been evaluated for both inverters considering both harmonic and interharmonic components. Simulation results manifest that the proposed Fuzzy Logic controller utilized for multiphase LIM drive presents satisfactory performance including fast response, no overshoot, negligible steady-state error, and lower maximum starting current. Furthermore, the applied five-level n-phase Cascaded H-bridge (CHB) VSI incorporating with multiband hysteresis modulation guarantees for harmonic and interharmonic reduction in the LIM drive.

Appendix

Fuzzy Logic controller gains: K_ω=0.008, K_e=0.05, K_i=1000
Genetic-PI controller gains: K_i=230.0118, K_p=84.3147

Table 3: LIM parameters

Phase voltage	240 V	R'_r	11.78 Ω
Current	5 A	L_{ls}	0.42 H
Power	1 HP	L'_{lr}	0.42 H
Pole pairs	2	L_m	0.4 H
Pole pitch	0.0465 m	λ^*_{dr}	0.9776 wb
Secondary length	0.82 m	M	4.775 kg
R_s	13.2 Ω	*Damping*	1 kg/s

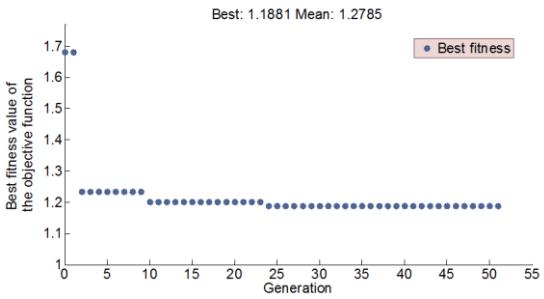

Fig. 14: The best objective functions in each generation during the optimization of PI gains using the genetic algorithm.

Author Contributions

This work is the continuations of the PhD thesis of P.Hamedani under supervision of Prof. A.Shoulaei. P.Hamedani carried out the data analysis, interpreted the results, and wrote the manuscript.

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Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

Abbreviations

D	LIM length
M	Primary weight
v_r	LIM speed
L'_r	Self-inductance of the secondary
R'_r	Resistance of the secondary
L'_{lr}	Leakage inductance of the secondary
R_s	Resistance of the primary
L_{ls}	Leakage inductance of the primary
L_{m0} (1-$f(Q)$)	Magnetizing inductance of LIM
ω_r	Secondary angular speed
ω	Synchronous angular speed
ω_{sl}	Slip angular frequency
F	LIM thrust
τ	Motor pole pitch
n	Number of phases
h	Hysteresis band
V_{dc}	DC bus voltage
u_1, …, u_n	logic variables
V_1 , …, V_n	Phase-to-neutral voltages
THD	Total Harmonic Distortion
TDHD	Total discrete harmonic distortion
TIHD	Total interharmonic distortion
m	Harmonic order
m_{max}	Maximum harmonic order
IRSS	Root sum squared value of the current interharmonics
f_1	Fundamental frequency
Δf	Frequency resolution
i_{1s}^*, i_{2s}^*, …, i_{ns}^*	Command primary currents
i_{qs}^*	Command q-axis primary current
i_{ds}^*	Command d-axis primary current
λ_{dr}^*	Nominal d-axis secondary flux
k_1, …, k_5	Importance coefficients
E_{SS}	Steady-state error

M_p	Overshoot
T_r	Rise time
T_S	Settling time
M_T, M_E, M_L	Scaling factors
P and L	Penalty factors
$\Delta V_r(n)$	Speed error
$\Delta e(n)$	Change of speed error
F_{obj}	Objective function
F_e^*	Command LIM force
K_ω, K_e, K_i	Fuzzy Logic controller gains
K_i, K_p	Genetic-PI controller gains

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Research paper

Stock Price Prediction Using Machine Learning and Swarm Intelligence

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Abstract

Background and Objectives: Stock price prediction has become one of the interesting and also challenging topics for researchers in the past few years. Due to the non-linear nature of the time-series data of the stock prices, mathematical modeling approaches usually fail to yield acceptable results. Therefore, machine learning methods can be a promising solution to this problem.

Methods: In this paper, a novel machine learning approach, which works in two phases, is introduced to predict the price of a stock in the next day based on the information extracted from the past 26 days. In the first phase of the method, an automatic clustering algorithm clusters the data points into different clusters, and in the second phase a hybrid regression model, which is a combination of particle swarm optimization and support vector regression, is trained for each cluster. In this hybrid method, particle swarm optimization algorithm is used for parameter tuning and feature selection.

Results: The accuracy of the proposed method has been measured by 5 companies' datasets, which are active in the Tehran Stock Exchange market, through 5 different metrics. On average, the proposed method has shown 82.6% accuracy in predicting stock price in 1-day ahead.

Conclusion: The achieved results demonstrate the capability of the method in detecting the sudden jumps in the price of a stock.

Introduction

Nowadays stock markets play a significant role in the countries' economies. Using the stock market, the personal savings and administering funds can be guided through important industries which in turn result in growing the country's economy and also make the investors profit. Investing in a profitable company is critical for investors. So reducing the risk of investing is of great importance. Therefore, the stock market prediction has become one of the interesting and also challenging tasks for researchers and investors. Professional traders use fundamental and technical analysis to predict the future of stocks. In fundamental approaches, the parameters of the company are used while in technical analysis, based on Dow theory [1] the stock price history is important. In the last three decades, several mathematical approaches have been suggested for stock price prediction but the results were not satisfying because of the non-linearity and non-stationary nature of the financial time series data [2]. In recent years, many data scientists have concentrated on developing stock price prediction models based on non-linear and complex machine learning methods such as artificial neural networks (ANN) and regression methods. Several types of research have been conducted in the field of using different types of neural networks for stock price prediction in the last years. Some of these researches have shown that ANN has few drawbacks and

it is not suitable for this purpose due to the complexity of the data and enormous noise. Probably the main reasons are unsuccessful training strategy for multilayer networks and also tend to fall into a local optimum solution which can cause overfitting [3]. Thus using powerful methods to analyze the complex time series data of stock prices is necessary. Metaheuristics are powerful optimization algorithms designed to solve complex and hard optimization problems. In this research, a prediction model based on support vector regression (SVR) [4] and particle swarm optimization (PSO) [5], [6] is introduced which is evaluated on 5 companies' datasets in the Tehran Stock Exchange market. The proposed method works in two-phases. In the first phase, an automatic clustering algorithm, which is based on PSO, is used to cluster the data points and in the second phase a hybrid regression model, which is a combination of PSO and SVR, is trained for each cluster. In both phases, PSO is selected due to its low complexity in compare to other metaheuristics and also effectiveness in solving hard and complex optimization problems, which is also addressed in several literatures [7]-[9].

To estimate the target value of an unknown sample, first, it should be assigned to the closest centroid then, the target value is estimated using the regression model, trained by the samples of the corresponding cluster. Clustering the data points in the first phase, and training independent regression models for different clusters, in the second phase, can remarkably reduce the noise effect, which is shown in our experiments. On the other hand, data complexity and scale are the two main challenges in stock price prediction which can reduce the accuracy of the machine learning method. Dividing the data points into different clusters using an automatic clustering algorithm, can solve this problem. Learning and extracting the hidden patterns and also recognizing the trends hidden in a small cluster of similar samples, are easier tasks compared to learning a huge dataset. Thus, clustering the data points in the first phase and then training different regression models for different clusters, is an effective method for analyzing massive time-series data. Feature selection is another important factor that can improve the accuracy of the proposed method. Eliminating redundant features reduces the ambiguity and complexity of the data points in each cluster.

The main novelties of this research are:

1. Using a novel automatic clustering algorithm that can find the number of clusters in the first phase.

2. Training optimal regression method for each cluster in the second phase. In this optimal regression method, called PSO-SVR, PSO is used for feature selection and parameter optimization for SVR.

The results achieved for 5 symbols in the Tehran Stock Exchange market demonstrate the fabulous performance and effectiveness of the proposed method. The rest of the paper is organized in the following manner: in section 2 the similar works are reviewed and analyzed. In section 3, the raw data and the extracted features are completely described. Sections 4 and 5 are devoted to the proposed method and experimental results respectively.

Related Works

In [10], Gozalpour and Teshnehlab have proposed a prediction method based on deep neural networks. Also, they have used principal component analysis (PCA) and an autoencoder network for dimension reduction. In their research, the data of the past 30 days has been used to predict the closing price of the next day. Their data includes closing price, opening price, highest price, lowest price, and volume of the stock transactions. The method is tested on three NASDAQ symbols. Despite using a complex method, the main drawback of this research is ignoring technical indicators of the stock data. In [11], a method called (2D)2PCA+Deep NN is introduced for stock multimedia prediction. Although, the method has shown improvement in stock multimedia prediction, in case of large window size it has shown poor performance. Besides that, using PCA, as a preprocessing unit, and training a deep neural network is a time-consuming procedure which is a drawback. In another research, Ramezanian et al. have proposed a complicated method which is an integrated framework including genetic network programming (GNP), multilayer perceptron (MLP), and time-series models for stock return forecasting and rule extraction [12]. The performance of the method has been tested on 9 symbols active in the Tehran Stock Exchange market. In their research, the GNP model along with reinforcement learning and multi-layer perceptron is applied to classify data and also time-series models to forecast the stock return. Moreover, the rules of accumulation, based on the GNP model's results are utilized to forecast the return. In addition to the high complexity of the proposed method, which may result in slow training, the major drawback is the high possibility of being trapped in the local optimum point in the training phase of the MLP. In [13] a hybrid method called BOA-SVR is introduced which is a combination of the butterfly optimization algorithm (BOA) and support vector regression machine (SVR). In this research first, the data is prepared by phase space reconstruction. Then the model is trained on the data. In the model, the BOA algorithm is used to tune the parameters of the SVR since its performance is highly dependent on the values of the parameters. In the data preparation phase, technical indicators are not considered while they can

improve the performance of the method. Also, BOA can be used to search the solution space for the best feature subset which is ignored in this research. Zahedi and Rounaghi have researched the Tehran Stock Exchange market [14]. They adopted a three-layer feedforward MLP to predict the stock price on the Tehran Stock Exchange. Also, PCA is used in their model for dimension reduction. Again, the main drawback of their method is neglecting the possibility of falling into a local optimum point during the training phase of the MLP network. This problem becomes more intense when dealing with massive and complex datasets. In another research, Akita and his colleagues presented a deep learning method for stock prediction [15]. The proposed model is tested on 10 companies in the Tokyo stock market. In their paper, they have proposed an approach that converts newspaper articles into their distributed representations via a method, called Paragraph Vector, and models the temporal effects of past events on opening prices about multiple companies with LSTM. Even though the news published in newspapers affects the stock prices, gathering financial news from different newspapers and converting them to numerical information is a very hard task which makes this method less applicable than other methods. In a similar but more comprehensive research, conducted by Khan et al., the related tweets in Twitter and the financial news from Business Insider are extracted and converted into numerical format [16]. Also, the historical data of the stocks are used to create a structured dataset. Several classifiers are used and evaluated in this research. like the previous research, this method suffers from gathering non-uniform and complex data that should be interpreted using sentiment analysis. Rustam and Kindantani have proposed a method to predict the closing price of stocks in the Indonesian stock market [17]. In this method first, a dataset is created by calculating 14 indicators from raw data. After dimensionality reduction using PSO, SVR is used to estimate the closing price of the next day. PSO is used to search the solution space for the best feature subset with the minimum value of MSE function. This means that SVR should be trained, for each search agent, on a massive dataset in each iteration to calculate MSE value. Although SVR is a strong regression method, in the case of processing big datasets it fails to perform well. In our method, which is introduced in section 4, to overcome this problem the dataset was divided into different clusters by using an automatic clustering algorithm, then SVR was trained for each cluster. In [18] Omidi and his colleagues used a simple ANN model to predict the future price of stocks. They have evaluated their method capability on the Tractor manufacturing company in the Tehran stock market. Excluding technical indicators and the high possibility of being trapped in local optimum point in the training process of ANN, are the main disadvantages of their method. In an interesting research, a hybrid model is introduced for stock price prediction by Gocken et al [19]. In this research, the Harmony Search (HS) algorithm is used to find the best architecture of the Jordan Recurrent Neural Network (JRNN) and also the best subset of input variables. HS searches the solution space to find the optimal number of hidden neurons, the best technical indicators as input variables, and the best transfer function. Thus, HS should explore and exploit a very high dimensional feature space which increases the probability of being trapped in the local optimum point. On the other hand, training JRNN for each search agent in each iteration makes their method very slow especially, in the training phase. In another research conducted recently, Nikou and her colleagues investigated the performance of deep learning on stock price prediction [20]. They have used the LSTM network to predict the close price of iShares MSCI United Kingdom. Also, they have compared the achieved results to three data mining techniques (Artificial neural network, SVR, and Random Forest). In their research, the effects of technical indicators are not analyzed and the close price has been just considered as the input value. on the other hand, despite SVR has shown better performance than neural network and Random Forest, its parameters have not been tuned with a powerful optimization algorithm. In 2020, Chandar proposed a hybrid method, called GWO-ENN, for stock price prediction which is evaluated on NYSE and NASDAQ stock data [21]. In this method, GWO is used to optimize the Elman Neural Network. The proposed method uses 10 technical indicators to forecast the close price in 1 day ahead. Unlike the previously mentioned researches, only technical indicators are used as input variables and the historical data of the past days are excluded. Gandhmal and his colleagues have provided a review paper on stock market prediction techniques which is very helpful in analyzing different methods proposed for stock price prediction up to now [22].

Data Preparation

The historical data of the stocks are freely accessible on the website of the Tehran Stock Exchange Market[1]. This historical data contains open price, close price, highest price, lowest price, and volume of the transactions for each working day. Besides that, building an accurate model, it is necessary to calculate technical indicators. In this research the following indicators are used for data preparation: MACD, Bollinger bands (upper band, the middle band, and lower band), fast stochastic,

[1] www.tsetmc.com

SI, and William index. Therefore, a structured dataset containing the historical data and the indicators is created with the window size of 26 [23]. For example, the first object of the dataset contains the historical data and the indicators calculated for the period of 26 days, from the first day to the 26th day, which are listed in a vector form. The second object of the dataset contains similar information from the second to the 27th working day. Other objects of the dataset are calculated using the same scheme. As mentioned before, for each day, the historical data contains 5 items including open price, close price, highest price, lowest price, and volume of the transactions. So for the whole period, each object has 130 items. Also, 7 more items are showing the values of the indicators for the corresponding period. Therefore, each object of the dataset is a vector with a size of 137. The target value of the object is the close price of the first day after the 26 days. For instance, for the first object the close price of day 27, is the target value and similarly, the close price of day 28 is the target value of the second object. This means that the main goal of this research is to estimate the stock price of tomorrow. In other words, to estimate the price of a stock in tomorrow using this model, the information of the past 26 days is needed. In the next section, the proposed method is completely explained.

Proposed Method

A two-phase method is presented in this paper for stock price prediction. In the first phase, an automatic clustering algorithm, called APSO-Clustering, is used to partition the dataset into different clusters. APSO-Clustering, which is designed and developed in our previous project, searches the solution space to find the proper number of clusters and the position of the centroids simultaneously. The effectiveness and the power of this automatic clustering method are proved in our last papers [24], [25]. In the second phase, an optimized regression method called PSO-SVR is trained for each cluster. In this method, PSO is used to find the best feature subset from 137 features of the dataset and to find the optimal kernel function's value of SVR. In the next subsections, support vector regression, APSO-Clustering method, and PSO-SVR are completely clarified.

A. Support vector regression

Support vector regression is the promoted version of the support vector machine [26]. SVR uses a new loss function called ε-insensitive loss function which is used to penalize data greater than ε [27]. SVR is a non-linear kernel-based regression method that provides the best regression hyperplane considering the smallest risk minimization principle in high-dimensional feature space [28]. Assume that $D = \{(x_i . y_i)\}_i^n$ is the training dataset that the regression model is supposed to be built on. In this dataset x_i is the ith data point, y_i is its target value, d is the dimension, and n is the number of data points in the dataset. The following formula shows the function of SVR:

$$y = f(x) = W^T \emptyset(x) + b \tag{1}$$

Where $\emptyset$ is a non-linear mapping function which maps the data points from input space to feature space, W is the vector of weight coefficients and b is the bias term. In the training phase the goal is to find W and b through solving the following optimization problem:

$$\min \frac{1}{2} \|W\|^2 + C \sum_{i=1}^{n} (\xi_i + \xi_i^*)$$
$$\text{s.t.:} \begin{cases} y_i - W^T \phi(x_i) - b \le \varepsilon + \xi_i \\ y_i - W^T \emptyset(x_i) - b \ge -\varepsilon - \xi_i^* \\ \xi_i . \xi_i^* \ge 0 . i = 1 . \cdots . n \end{cases} \tag{2}$$

Where C is the penalty factor, ε is insensitive loss function and ξ_i and ξ_i^* are slack variables that measure the difference between the model's output and the target value beyond ε. After solving the optimization problem through Lagrangian multipliers and conditions for optimality, the following equation can be represented as the dual form of (1):

$$f(x) = \sum_{i=1}^{n} (\beta_i - \beta_i^*) \cdot K(x_i . x) + b \tag{3}$$

In this equation, β_i and β_i^* are nonzero Lagrangian multipliers and $K(x_i . x)$ is the kernel function. In this paper, Gaussian kernel function is used which is shown in (4):

$$K(x_i . x_j) = exp\left(-\gamma \|x_i - x_j\|^2\right) \tag{4}$$

According to equation (4) defining the value of γ is necessary. In other words, the value of γ has an important effect on the final accuracy of the regression model. Therefore, finding the best value for γ is of great importance which has been done by PSO in this research.

B. APSO-Clustering method

APSO-Clustering is an automatic clustering method that can detect the proper number of clusters in addition to the position of the centroids. Inability in finding the number of clusters is one of the drawbacks of common and popular clustering methods such as K-means and fuzzy C-means which makes them inefficient in clustering big datasets. although many methods have been proposed to estimate the number of clusters such as [29], [30] but in the case of big data clustering, complexity and huge amount of data make them inaccurate. In 2000, a promoted version of K-means, called X-means [31], is introduced which can find the number of clusters, but the main advantage of APSO-Clustering, over X-means, is its high accuracy in

partitioning complex and massive datasets. APSO-Clustering clusters the data points in two stages. In the first stage, detecting the appropriate number of clusters and in the second stage, finding the centroids are the main goals. Both stages are based on a non-automatic clustering method called PSO-Clustering. In other words, the PSO-Clustering method is the basic block in both stages. In the first stage, it is used to find the number of clusters and in the second stage, it is tuned to find the position of the k centroids where k is the number of clusters detected in the first stage. Therefore, PSO-Clustering should be explained completely first.

In PSO-Clustering, PSO is used to find the position of the centroids. As mentioned before, it is a non-automatic clustering method which means that k (number of clusters) should be predetermined by the user. So particles, which are potential solutions to the clustering problem, contain $k \times p$ cells where p is the number of features in the dataset, and k is the number of clusters. For fitness evaluation, Calinski-Harabasz index [32] is used which measures the quality of a clustering. PSO-Clustering and k-means perform the same task in different ways. The main downside of k-means is the high probability of finding the local optimum point instead of global point. This results in poor performance, especially when dealing with massive and complex datasets [33]. In PSO-Clustering this problem is covered by using a metaheuristic optimization algorithm. PSO has shown great performance in solving hard and complex optimization problems [34]. High capability in escaping from local optimum points and finding the global point is the main property of PSO. In the first stage of the APSO-Clustering method, PSO-Clustering should be run sequentially with different values of k. In other words, in a sequence, containing 10 steps, PSO-Clustering is run in each step with a specified value of k which is defined using the following equation:

$$k_{new} = k_{old} \pm \alpha \tag{5}$$

where α is a random integer number, k_{new} is the value of k in the current step and k_{old} is the value of k in the previous step. At the end of the first stage, among the solutions found in different steps of the sequence, the solution with the best fitness value determines the best value of k.

In the second stage, the PSO-Clustering method searches the solution space to find the exact position of k centroids, while k is the output of the first stage. In the second stage, the number of the particles and the iteration number are set to 50 and 600 respectively. These numbers are 5 and 150 in each step of the sequence in the first stage. In Fig. 1, the pseudo-code of the APSO-Clustering method is demonstrated.

C. PSO-SVR

PSO-SVR is a hybrid regression method which has been introduced by Xiong and Xu in 2006 [35]. Also, it has been used in different researches in the last years. For example, in 2015, Hu and his colleagues have used PSO-SVR for short-term traffic flow forecasting [36]. In their research, PSO is used for tuning the parameters of SVR. The performance of SVR is heavily dependent on the kernel function and the value of its parameter. Gaussian kernel (or RBF) is one of the most popular kernel functions which usually yields high accuracy [37]. In our method, PSO is used to find the proper value of the Gaussian function's parameter (γ). Besides that, PSO searches the solution space to find the best feature subset among the 137 features of the dataset. So in the proposed method, PSO is used for feature selection and parameter tuning while in [33], parameter tuning is the only task of PSO.

```
Stage 1:
Inputs: number of sequences, length of sequence, number of population
For i=1 to number of sequences do:
        1.k = Generate a random integer number
        2. beginning population = Generate a random population
        3.Current state.fitness = inf
        4. Current state.k=Ø
        for j=1 to length of sequence do:
                if (j==1) do:
                        current state.k=k
                end
                best fitness = PSO-Clustering(k, beginning population)
                if best fitness < current state.fitness
                        current state.fitness=best fitness
                        curent state.k=k
                end
                k = current state.k ± ε
        end
Best[i] = current state.k
End
Output: find the best solution which has the best fitness amount and its corresponding k
and its corresponding beginning population
Stage 2:
Final output = PSO-Clustering(best k, beginning population)
```

Fig. 1: pseudo-code of APSO-Clustering [25].

Each particle contains 137 cells for feature selection, which are encoded in binary form, and one cell for the value of γ. Mean squared error (MSE) function is used for fitness evaluation which is calculated using a 3-fold cross-validation method. In the second phase of the proposed method, for each cluster, a PSO-SVR model is trained. In fact, for each cluster, an SVR is trained with the optimal value of γ and the best feature subset, found by PSO. To estimate the target value of an unknown sample, first, the cluster of the sample is found based on the closeness of the sample to the centroids. Then the corresponding regression model estimates the target value of the unknown sample. In Fig. 2, the flow chart of PSO-SVR is shown. In the next section, the final results of the proposed method for 5 symbols of the Tehran Stock Exchange market are presented.

Experimental results

Five symbols of the Tehran Stock Exchange market are selected for performance evaluation including *Chekaren*, *Shekabir*, *Tepompy*, *Sharak, and Hekhazar*. The accuracy is measured using MSE, MAE, MAPE, RMSE, and R^2 metrics. To compare the performance of PSO with another metaheuristic, the results of GWO-SVR is also measured. This means that the second phase of the proposed method is done by the two metaheuristics to reach a fair comparison between the performance of PSO and GWO. Also, the results of simple SVR are shown for each dataset to analyze the effect of clustering and feature selection. In all of the experiments, 70% of the datasets are used for training and 30% for testing. All of the results, written in the following tables, are for testing data.

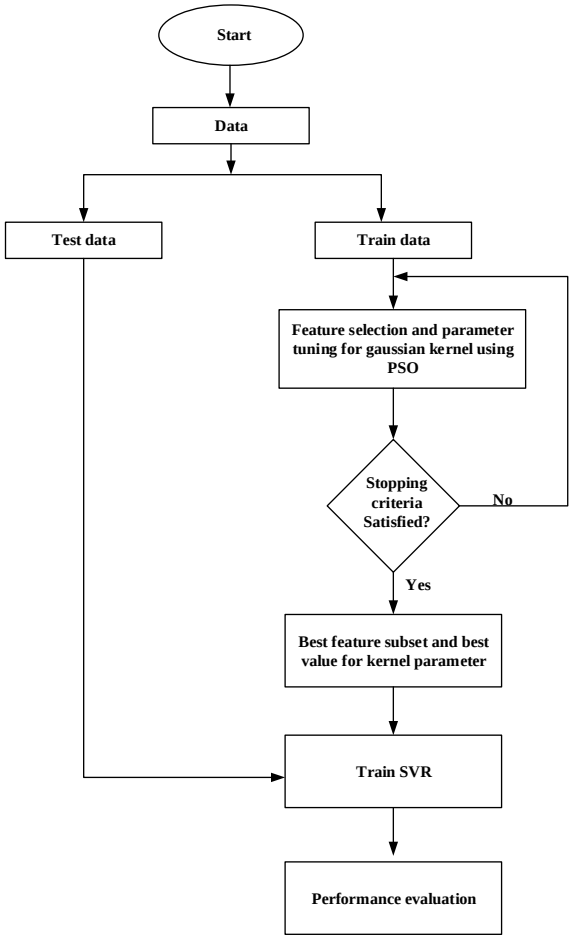

Fig. 2: Flow chart of PSO-SVR.

In the second phase of the proposed method, when PSO-SVR and GWO-SVR are training, 20% of the training data is used for validation which means that for each search agent, after training SVM with 80% of the training data, the fitness value is measured by calculating MSE on the validation data. In PSO-SVR and GWO-SVR, the number of search agents and the maximum number of iterations are set to 15 and 150 respectively which are found after several experiments. For each dataset, the number of detected clusters, the number of selected features, and the optimal values of γ are written separately.

D. Chekaren

Daily information for this symbol (from 2001/3/26 to 2019/11/17) is extracted from the website of the Tehran Stock Exchange market. After creating a dataset using the raw data and technical indicators, in the first phase of the proposed method, APSO-Clustering has divided the data points into 2 clusters. Table 1 and Table 2, presents the details and the accuracy of the results achieved by PSO-SVR and GWO-SVR in the second phase.

Table 1: The details of the results achieved by PSO-SVR and GWO-SVR for Chekaren.

Method	Number of clusters	Number of selected Features	Values of γ
PSO-SVR	2	65, 71	1, 4
GWO-SVR	2	131, 121	1,2

Table 2: The accuracy achieved by the three methods for Chekaren

Method	MSE	MAE	MAPE	RMSE	R^2
PSO-SVR	6.83×10^6	1.62×10^3	32.62	2.62×10^3	0.87
GWO-SVR	8.34×10^6	1.88×10^3	32.21	2.88×10^3	0.84
SVR	5.46×10^7	3.64×10^3	93.23	7.39×10^3	0.0024

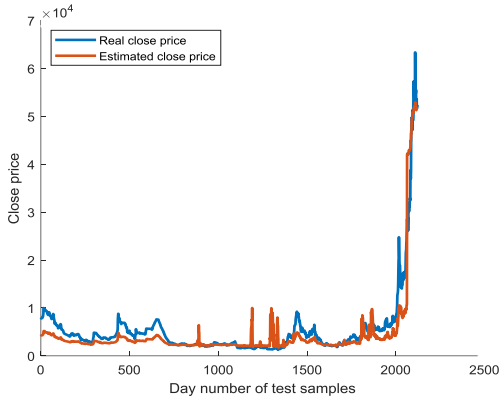

Fig. 3: Real and estimated close price for Chekaren found by PSO-SVR.

According to Table 1, in the second phase, PSO has found 65 and 71 features for the first and second clusters respectively while GWO has detected 131 and 121. Also, the best values found for γ by PSO are 1, 4 for the first and second clusters respectively. These values are 1 and 2 for GWO-SVR. The superiority of the proposed method over the simple SVR with the Gaussian kernel is shown in Table 2. Also in this table, the superiority of PSO over GWO is demonstrated while PSO

has selected fewer features for both clusters in comparison to GWO. In Fig. 3, the blue curve shows the close prices of the test samples and the red curve shows the estimated values which is the output of PSO-SVR. It can be seen, that the red curve approximates the blue curve very well which is confirmed by the amount of R^2. R^2 index for this symbol is 0.87 (for PSO-SVR) which means that the similarity of the two curves is approximately 87 percent while this index is 0.0024 for SVR. According to Fig. 3 and Table 2, the performance of the proposed method, especially in detecting the fluctuations of the stock price, is great. In another point of view, comparing the performance of the proposed method (both PSO and GWO in the second phase) to SVR, we can see the positive effect of clustering and feature selection.

E. Shekabir

For this symbol, which the raw data is recorded from 2011/6/7 to 2019/11/17, 4 clusters are found by APSO-Clustering in the first phase. In the second phase, 4 optimal SVR models are trained for each cluster by PSO and GWO. The number of selected features and the γ values are shown in Table 3. In Table 4, the accuracy measurements achieved by the three methods are shown. According to this table, the accuracy of the proposed method is approximately 87% which means that we can predict the stock price of the next day with an 87% probability of success. Fig. 4 shows the real and estimated price curves. This figure indicates the high capability of the proposed method in detecting the sudden rise and fall in the stock price which is very important for the investors.

Table 3: The details of the results achieved by PSO-SVR and GWO-SVR for Shekabir.

Method	Number of clusters	Number of selected Features	Values of γ
PSO-SVR	4	64, 59, 64, 76	1, 4, 1, 1
GWO-SVR	4	32, 42, 38, 29	2, 4, 1, 1

Table 4: The accuracy achieved by the three methods for Shekabir

Method	MSE	MAE	MAPE	RMSE	R^2
PSO-SVR	1.48×10^6	969.12	14.88	1.21×10^3	0.87
GWO-SVR	1.85×10^6	1.09×10^3	16.25	1.36×10^3	0.84
SVR	4.53×10^6	1.28×10^3	28	2.12×10^3	0.62

According to Table 4, PSO has a slight superiority over GWO while it has selected more features.

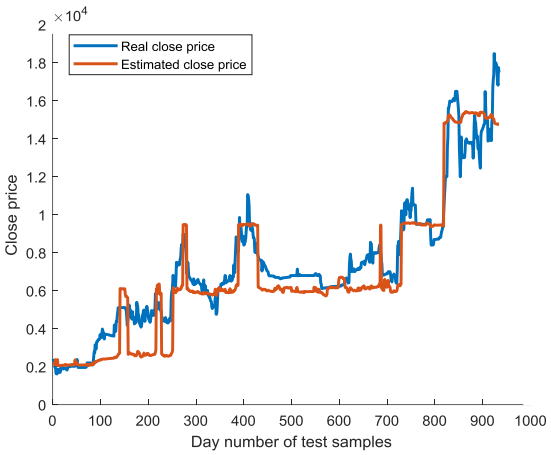

Fig. 4: Real and estimated close price for Shekabir found by PSO-SVR.

F. Tepompy

For this company, the stock price data is recorded from 2001/3/26 to 2019/11/13. In the first phase of the proposed method, the data points are divided into 2 clusters and in the second phase, two SVR models are trained for each cluster using PSO and GWO. Table 5 and Table 6 include the details and accuracy of the three methods. According to Table 6, PSO has shown a better performance than GWO. Also, the superiority of PSO-SVR and GWO-SVR over simple SVR shows the effectiveness of the proposed method. Fig. 5, demonstrates the real and the estimated curves of the close price.

Table 5: The details of the results achieved by PSO-SVR and GWO-SVR for Tepompy.

Method	Number of clusters	Number of selected Features	Values of γ
PSO-SVR	2	67, 68	3, 1
GWO-SVR	2	29, 19	2, 1

Table 6: The accuracy achieved by the three methods for Tepompy.

Method	MSE	MAE	MAPE	RMSE	R^2
PSO-SVR	9.3×10^5	816.76	22.97	966.06	0.63
GWO-SVR	1.06×10^6	906.74	26.27	1.03×10^3	0.57
SVR	2.78×10^6	1.45×10^3	52.09	1.66×10^3	0.10

G. Sharak and Hekhazar

In Tables 7 to 10, the details and the accuracy of the results achieved for these two symbols are presented. Also, the corresponding curves are shown in Fig. 6 and Fig. 7.

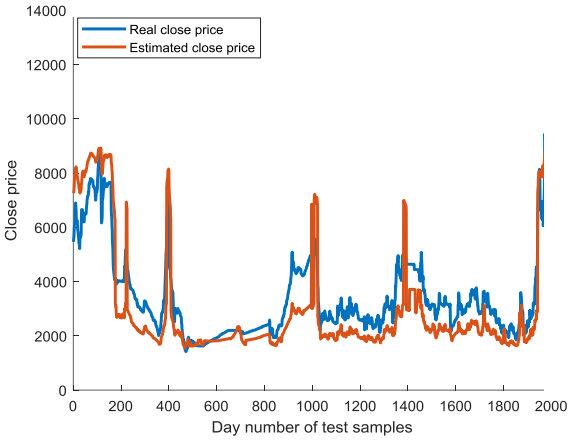

Fig. 5: Real and estimated close price for Tepompy found by PSO-SVR.

Table 7: the details of the results achieved by PSO-SVR and GWO-SVR for Sharak

Method	Number of clusters	Number of selected Features	Values of γ
PSO-SVR	4	73, 74, 66, 68	1, 1, 1, 3
GWO-SVR	4	38, 30, 34, 35	2, 3, 2, 3

Table 8: the details of the results achieved by PSO-SVR and GWO-SVR for Hekhazar.

Method	Number of clusters	Number of selected Features	Values of γ
PSO-SVR	3	65, 65, 66	1, 4, 4
GWO-SVR	3	31, 30, 52	3, 4, 5

Table 9: The accuracy achieved by the two methods for Sharak.

Method	MSE	MAE	MAPE	RMSE	R^2
PSO-SVR	2.60×10^{6}	1.16×10^{3}	17.81	1.61×10^{3}	0.89
GWO-SVR	2.54×10^{6}	1.18×10^{3}	20.26	1.59×10^{3}	0.90
SVR	2.33×10^{7}	3.67×10^{3}	74.84	4.83×10^{3}	0.09

Table 10: The accuracy achieved by the two methods for Hekhazar.

Method	MSE	MAE	MAPE	RMSE	R^2
PSO-SVR	1.61×10^{6}	956.90	19.4	1.27×10^{3}	0.87
GWO-SVR	1.69×10^{6}	980.99	19.67	1.30×10^{3}	0.86
SVR	1.01×10^{7}	2.85×10^{3}	72.89	3.18×10^{3}	0.21

In all of the experiments conducted for these 5 symbols, the proposed method has shown a better performance than SVR. Actually, the tables show the dramatic effect of using clustering and feature selection. Figures 3 to 7 indicate that although in some cases, the proposed method has failed to predict the exact price, in all experiments it has demonstrated a great capability in detecting rise and falls of the stock price.

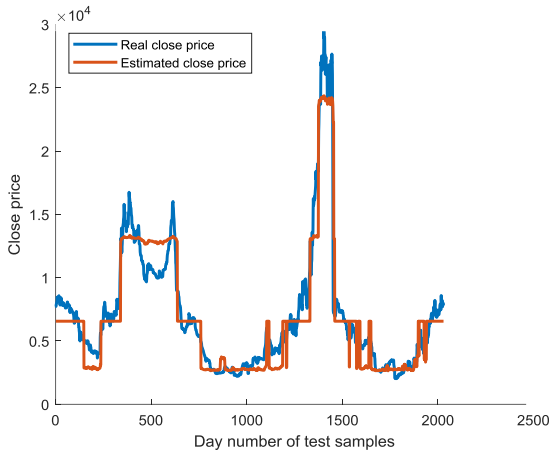

Fig. 6: Real and estimated close price for Sharak found by PSO-SVR.

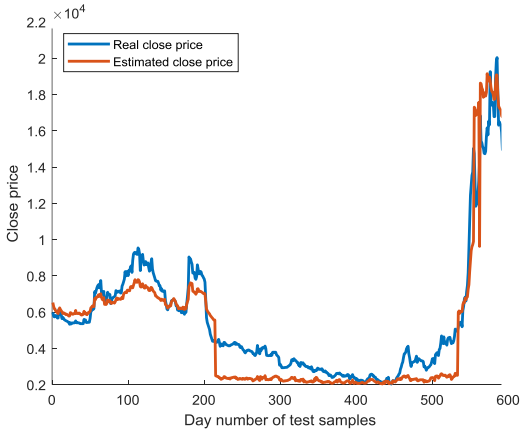

Fig. 7: Real and estimated close price for Hekhazar found by PSO-SVR.

In Table 11, the average accuracy measurements of PSO-SVR and GWO-SVR are written to reach a general comparison between the performance of GWO and PSO. According to this table, although the performances of PSO and GWO are very close to each other, there is a slight difference between their accuracy which shows the superiority of PSO. The most important result which can be extracted from Tables 1 to 11 is the effectiveness of the proposed idea based on using clustering and hybrid regression method for stock price prediction.

Table 11: The average accuracy of PSO-SVR and GWO-SVR

Method	MSE	MAE	MAPE	RMSE	R^2
PSO-SVR	2.69×10^{6}	1.10×10^{3}	21.53	1.53×10^{3}	0.82
GWO-SVR	3.09×10^{6}	1.20×10^{3}	22.93	1.63×10^{3}	0.80

Results and Discussions

Stock price prediction is one of the challenging tasks because of the chaotic and non-linear trend of stock

prices. Due to the availability of the historical data of the stocks in different markets, predicting the future price of stocks has become one of the interesting topics for data scientists. Therefore, different linear or non-linear methods have been introduced in the past years. In this paper, a new machine learning method is introduced to tackle this challenge. The performance of the proposed method is tested on 5 companies in the Tehran stock market. The results indicate that this method has great power in detecting the jumps in the stock price. For future works, we can improve this method to predict the stock price for more than 1 day ahead, which can help us in producing buy and sell signals.

Conclusion

The results indicate that it is possible to predict the stock price trends using swarm intelligence methods with acceptable accuracy. In other point of view, the results demonstrate the power and effectiveness of the swarm intelligence methods in solving hard and complex optimization problems.

Authors contributions

The proposed method is designed and implemented by Iman Behravan and the results are interpreted by Dr. Seyed Mohammad Razavi.

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Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

Abbreviations

PSO	Particle Swarm Optimization
SVR	Support Vector Regression
ANN	Artificial Neural Network
APSO-Clustering	Automatic PSO-Clustering
PCA	Principle Component Analysis
GNP	Genetic Network Programming
MLP	Multi-Layer Perceptron
BOA	Butterfly Optimization Algorithm
LSTM	Long-Short Term Memory
JRNN	Jordan Recurrent Neural Network
GWO	Grey Wolf Optimizer
MACD	Moving Average Convergence Divergence

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Biographies

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Research paper

A High-Performance Model based on Ensembles for Twitter Sentiment Classification

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Abstract

Background and Objectives: Twitter Sentiment Classification is one of the most popular fields in information retrieval and text mining. Millions of people of the world intensity use social networks like Twitter. It supports users to publish tweets to tell what they are thinking about topics. There are numerous web sites built on the Internet presenting Twitter. The user can enter a sentiment target and seek for tweets containing positive, negative, or neutral opinions. This is remarkable for consumers to investigate the products before purchase automatically.

Methods: This paper suggests a model for sentiment classification. The goal of this model is to investigate what is the role of n-grams and sampling techniques in Sentiment Classification application using an ensemble method on Twitter datasets. Also, it examines both binary and multiple classifications, which are classified datasets into positive, negative, or neutral classes.

Results: Twitter Classification is an outstanding problem, which has very few free resources and not available due to modified authorization status. However, all Twitter datasets are not labeled and free, except for our applied dataset. We reveal that the combination of ensemble methods, sampling techniques, and n-grams can improve the accuracy of Twitter Sentiment Classification.

Conclusion: The results confirmed the superiority of the proposed model over state-of-the-art systems. The highest results obtained in terms of accuracy, precision, recall, and f-measure.

Introduction

With an increasing number of tweets over the Webs, tweets have interested more and more. There is a high interest in Sentiment Classification (SC) of tweets [1]-[9]. In many web sites, the user records an opinion, including positive, negative, or neutral sentiments [10]-[11]. Twitter classification is an outstanding problem, which has very few free resources and not available due to modified authorization status. However, all Twitter datasets are not labeled and free, except for our applied dataset.

Many kinds of research in Twitter Sentiment Classification (TSC) have converged on the usage of regular classifiers and machine learning-based classifiers [3], [7], [10]-[13]. The main problem in supervised techniques is the availability of labeled datasets [8]. We can only prepare a rare number of datasets for supervised models because manually collecting them is time-consuming. Also, a few studies [3] converged on the ensemble method. The current authors in 2015

compared the validity of supervised and unsupervised approaches [14].
Yet, tweets are vaguer than other sentiment data like reviews [15].

Different challenges can be studied in TSC [3] concerning other datasets: classification accuracy, data sparsity problem, and neutral tweets. These cause to largest of tweets incorrectly classified. It revealed that Part of speech (POS) features were not helpful in the micro-blogging [1]. In the current study, we examine to define a way that increases classification performance.

In this article, we suggest a novel model, namely NEST, to improve TSC. Specifically, the boosting method, n-gram features, bootstrapping sampling, and Term Frequency–Inverse Document Frequency (TFIDF) weighting mechanism applied. The suggested model is novel, because it applies both binary and multiple datasets and combines n-gram, sampling techniques, and ensemble methods for TSC. We reveal that our model plays a vital role in the performance of the model. We produced multiple classifications containing positive, negative, or neutral tweets. We showed that the combination of TFIDF, sampling, and n-gram has a better result for both datasets. Also, we show that the usage of ensemble methods and combined with n-grams can increase the accuracy of TSC. Twitter-Sanders-Apple (TSA) datasets used in all experiments. The effectiveness of the suggested model compared with the methods in [4], [21], [26]-[27], [30], [32]. Our findings exposed that our features are well in two datasets. The obtained results presented in two experiments and validated that our model outperforms the existing methods on the datasets. The highest f-measure obtained 93.52% by our model on TSA2; whereas, Padmaja and Hegde [32] obtained 89.73%. Also, the best f-measure of the NSET achieved 89.64%; whereas, the highest f-measure in the literature obtained 81.25% by Pandey et al. [4] on the TSA3. It revealed that our model works better than the other methods based on genetic algorithm (GA) in [32] and cuckoo search in [4]. It also revealed that the NSET works better than the other methods based ensembles in [21], fuzzy rules in [26], [30], and supervised techniques in [27].

The innovations of this study indicated as follows:

- The model is of an ensemble nature
- Applying sampling technique and n-gram besides weighting mechanism for improving classification efficiency
- Providing the boosting selector in conjunction with the popular classifier
- Choosing the best features based on the feature selection stage and two error indices
- Employing both two and three classes datasets on Twitter

The rest of this article organized as follows: Sec. 2 and Sec. 3 presents available techniques and related works, respectively. The proposed model is shown in Sec 4 and evaluated in Sec. 5. Finally, the conclusion and future works display in Sec. 6.

Available Machine Learning Techniques

The machine learning (ML) techniques for text classification algorithms, like maximum entropy (ME), naive Bayes (NB), and support vector machines (SVM), have achieved peerless success in SC text categorization, and these classifiers provided feasibility in their tasks. On reviewing the experiment dataset, the results of SVM was virtually better than other ML techniques. Hence we in our model used it to improve classification performance. Here, the summarization of some of the popular ML techniques in this context is of concern.

The ML approaches applied supervised, unsupervised, and semi-supervised methods and employed linguistic features. The lexicon-based approaches divided into corpus-based and dictionary-based approaches. The main advantage of them is to support in determining domain and context-specific opinion words using a domain corpus. In lexicon-based approaches, a document divides by aggregating the sentiment orientation of all available words. A document with more positive words classified as positive; whereas, the document with more negative words categorized as negative. Hybrid approaches combined the advantages of both approaches to improve the performance of SC.

Explanations of some classifiers are of concern herein.

A. Naïve Bayes

NB obtained reasonable accuracy. It is simple and assumed independent features.

Also, it mainly used when the size of the training set is not vast. Here, (1) is applied [16] to calculate the probability of event A in column A, provided that class C holds.

$$P(K=A\,|\,C)=\frac{1}{\sqrt{2\pi\sigma^{2}{}_{K=C}}}e^{-\frac{A-\mu_{K=C}}{2\sigma^{2}{}_{K=C}}} \quad (1)$$

where, $\mu k=c$ is the column K mean, while the row belongs to the class C and $\sigma^{2}_{k=c}$ is the variance of the kth therein, and no input classification is required. An example presented to explain the Bayes Continuous Decider, where, there exist four features with positive or negative classes.

B. Maximum Entropy

Unlike NB, ME is assumed dependent features [17]. This technique estimates $P(c\,|\,d)$ in

$$P_{ME}(c\,|\,d)=\frac{1}{Z(d)}e^{\sum_{i}\lambda_{i,c}F_{i,c}(d,c)} \quad (2)$$

where, Z(d) is a normalization function and $F_{i,c}$ is a function for feature F_i and class *c*, as in

$$F_{i,c}(d,c') = \begin{cases} 1 & n_i(d) > 0 \quad and \quad c' = c \\ 0 & otherwise \end{cases} \tag{3}$$

C. Neural Network

Here, a description of the perceptron classifier is of concern: If *m* is the count of the selected features and the dataset is named P, each user named P_i would have been assigned the *m* features, and if any connection attribute *x* is considered, there are variables x_1 to x_m for each connection. These inputs are samples of the training network. It is the training method with a supervisor because the network is trained through samples with the correct output (Fig. 1).

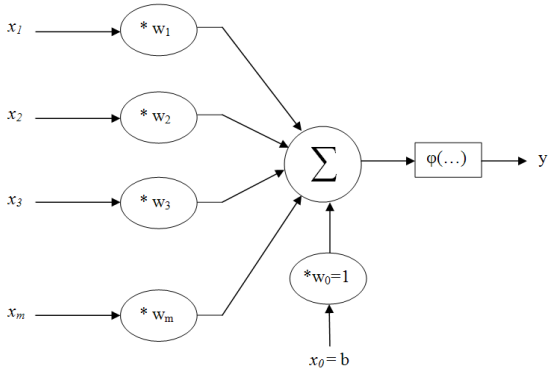

Fig. 1: Single-layer perceptron [18].

D. Support Vector Machine

In this structure, first, the attribute table converts into a set of data points $\{(x_1,c_1),(x_2,c_2),...,(x_n,c_n)\}$, and then, these divide into two classes $c_i = \{-1,1\}$. Each x_i is a p-dimensional vector of real numbers, which are the same properties extracted from the previous step.

Linear classification methods try to separate data by constructing a hyperplane, which is a linear equation). The SVM classification method, which is one of the linear classification methods, finds the best hyperplane that separates data from two classes with maximum margin. A picture of a data set belonging to two classes, which selects the best hyperplane for separating them exposed in Fig. 2. In this form, the data is two-dimensional, that is, each data consists of only two variables [19].

Here explains in detail how to produce a separator hyperplane. An accurate picture of how the separator hyperplane produced through the SVM exposed in Fig. 3.

First, consider a convex hull around the points of each class. In Fig. 3, the convex hull drawn around the points related to class -1 and class +1. Line P is the line that shows the closest distance between two convex hulls. *h*, which is the separating hyperplane, is a line that splits P and is vertical to it. The *b* is the width of the source for the hyperplane with the maximum separation limit. If *b* ignored, the solutions are the only hyperplane that goes beyond the source. The vertical distance of the hyperplane to the source achieved through dividing the absolute value of the parameter *b* by the length *w*.

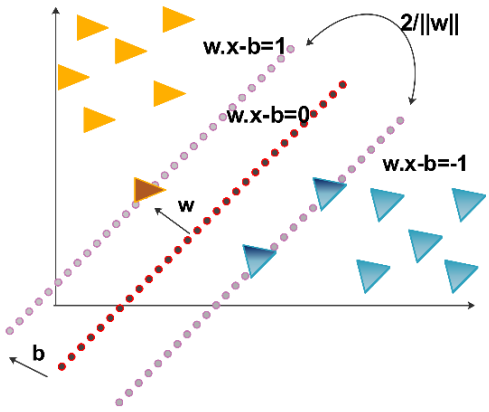

Fig. 2: Hyperplane with maximum separator boundary with separating boundaries for classification.

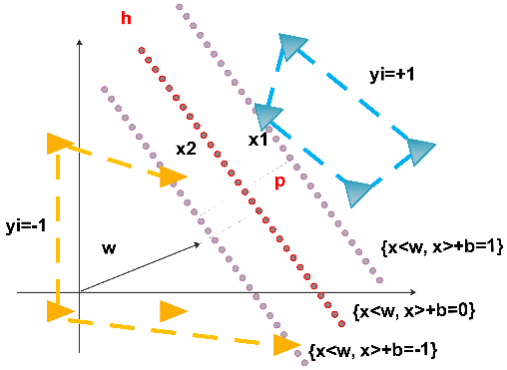

Fig. 3: How to build a separating hyperplane between two data classes in two-dimensional space.

The basic idea is to choose the proper separator. It refers to the separator that is farthest from the neighboring points on both floors. This answer has the highest boundary with points on two different floors and can be bounded by two parallel hyperplanes that pass through at least one of the floor points. These vectors are named support vectors. The mathematical equations for these two parallel hyperplanes are of concern (5) and (6).

$$w.x - b = 1 \tag{4}$$

$$w.x - b = -1 \tag{5}$$

It is remarkable to remark that if the training data are linearly separable, the two boundary hyperplanes can be chosen in such a way that there is no data between them, and then, the distance between the two parallel hyperplanes can be maximized. Applying geometric theorems, the distance between the two hyperplanes is $|\frac{w}{2}|$, So you have to $|w|$ Minimized. It is also necessary to

prevent data points from being placed within the boundary, for which a mathematical constraint added to the formal definition. For each *i*, it ensured through employing the following constraints that no point placed on the boundary. For data related to the first and second floors, (7) and (8) are of concern, respectively.

$$w.x_i - b \geq 1 \tag{7}$$

$$w.x_i - b \leq -1 \tag{8}$$

The following constraint can be shown as follows.

$$c_i(w.x_i - b) \leq 1 \qquad 1 \leq i \leq n \tag{9}$$

Related Work

SC has attracted a great deal of attention in recent years. A large number of methods proposed for improving classification performance. These methods differ from each other in the way the architecture of the classifier, algorithm parameters, or preprocessing methods. Here, the summarization of some of the existing articles on the TSA datasets are of concern:

In 2009, Liu et al. suggested an ESLAM model. They try to train a language model based on manually labeled data [20].

Expressed ensemble techniques are effective for SC of feature sets and classification algorithms. For example, in 2013, Hassan et al. proposed an ensemble framework in [21] and used a combination of unigrams and bigrams, POS, and semantic features derived from WordNet (WN) and SentiWordNet (SWN). Authors applied several base learners like NN, Random Tree (RT), NB, Bayes Net, Logistic Regression (LR), and SVM. Despite using the bootstrap model and several classifiers, their framework was not more effective than our approach. They obtained 76.30% of accuracy. Unfortunately, their different datasets are not available. In 2015, Lima et al. [22] introduced a polarity analysis framework for Twitter, which follows ML approaches. They utilized four datasets to estimate the performance of their framework. Additionally, they employed five kinds of classifiers like NB, SVM, Decision Trees (DT), and Nearest Neighbors (KNN).

In 2017, Keshavarz and Abadeh [23] combined both corpora and lexicon approaches. For this goal, they produced lexicons from the text. Also, they applied a novel GA to solve the SC problem. Adaptive sentiment lexicons generated by the algorithm to choose the best features. Their experiments conducted on six datasets. Also, Bala [24] used supervised and unsupervised techniques. The results obtained on three labeled datasets. Also, the author conducted a feature selection using a GA to verify results. The experiments reveal that the obtained results via supervised techniques are different on datasets. After the preprocessing stage, the document term matrix produced using unigram and bigram. Next, features extracted and supervised learning algorithms like NB, SVM, and DT applied to the datasets. Also, Pandey et al. [4] proposed a novel clustering method using k-means and cuckoo search in 2017. They achieved an accuracy of 81.4 and 82.20% for TSA2 and TSA3, respectively.

In 2018, Haider et al. [25] investigated the impact of adverbs for SC. Also, Trupthi et al. [26] investigated the effective topic modeling methodology Latent Dirichlet Allocation (LDA) to extract the keywords in a clustering manner. Next, they applied the keywords using the Possibilistic fuzzy c-means approach for twitter sentiment analysis.

The present researchers in [27] proposed a model named SFT for TSC in 2018. The goal of our model was to investigate the role of weighting feature techniques in SC using supervised methods on the Twitter data set. The applied classifier in the current article is based on the SFT model in our previous article.

Abdolahi and Zahedi in [28] introduced a method to consolidate the external word correlation knowledge into short and long stories in both local and global coherence in 2018. Using the effect of combined word2vec vectors, they confirm that their proposed method is free of the language and its semantic concepts. They received 87.03% of accuracy. Behravan et al. [29] in 2018 suggested a new clustering method for big datasets using Particle Swarm Optimization (PSO) algorithm. Their proposed method was a two-stage algorithm: (1) search the solution space for a proper number of clusters and (2) search to find the position of the centroids.

In 2018, Vashishtha and Susan in [30] estimated the sentiment of social media posts using a novel set of fuzzy rules. Their system combines Natural Language Processing techniques and Word Sense Disambiguation using nine fuzzy rule-based systems. They reached 59.7, 58.9, and 68.6% of precision, recall, and f1-score on the TSA3 datasets, respectively.

In 2019, Tripathi et al. [31] suggested a novel Map-Reduce based K-means to cluster the large scale data. Also, Padmaja and Hegde [32] proposed a system consists of three phases; data collection, preprocessing, and classification of sentiments. In the third phase, a hybrid classifier applied to classify the twitter sentiment classes.

In 2020, Abbas et al. [33] offered a classification model with four classifiers, and varying techniques consist of NB, DT, multilayer perceptron, and LR to form a single ensemble classifier. They gained an accuracy of 82.2% on Twitter. Also, Jiang et al. [34] develop a novel NN-based model, namely MAN, to conduct the aspect-level SC tasks.

In 2020, Naseem et al. [35] shown a transformer-based method for SA and applied deep intelligent contextual embedding to heighten the quality of tweets by removing noise. They also employed the bidirectional Long Short Term Memory (LSTM) network to define the sentiment of a tweet. They reached an accuracy of 96.2% on airline datasets.

In 2020, Samad et al. [36] studied the effect of seven text processing scenarios on Twitter. Their experiments revealed negative effects on SC of two common text processing steps: 1) stop word removal; 2) averaging of word vectors to represent individual tweets. Word selection from context-driven word embedding showed that only the ten most important words in Tweets cumulatively produce over 98% of the maximum accuracy. Also, Nemattolahzadeh et al. [37] suggested a method to utilize experimental data for identifying the influence network between individuals in social networks. Their method was based on convex optimization and could identify interaction patterns accurately. The three models were the most comprehensive and vastly models in the literature considered.

In 2020, Sharma and Jain in [38] presented a study on Twitter sentiment analysis where tweets collected and sentiments behind the tweet assessed using various ML techniques. They extracted data from twitter, and text preprocessing and feature extraction employed to the textual data. Correlation-based attribute selection methods applied and ML classifiers consist of SVM, NB, Random Forest, Meta classifier, and LR analyzed to confirm which classifier gives better results. They obtained an accuracy of 88.2% on the Cambridge Analytica dataset.

The NSET Model

The NSET model proposed in five stages: (1) preprocessing; (2) sampling; (3) weighting mechanism; (4) feature selection; (5) classification; and (6) performance evaluation. Fig. 4 tabulated the NSET model in detail.

Three main contributions of the NSET decorated in orange color.

In preprocessing, the n-grams applied to handle important relations. Next, a bootstrapping sampling performed to boost accuracy. After performing the TFIDF, classification methods run on test datasets. The AdaBoost method through the 10-fold cross-validation scheme on the dataset adjusted. In our model, shuffled and stratified samplings applied. In all experiments, results in terms of 10-fold cross-validation obtained.

The goal of this article is to study the role of n-grams and sampling using an ensemble method. Here, the stages of the model described.

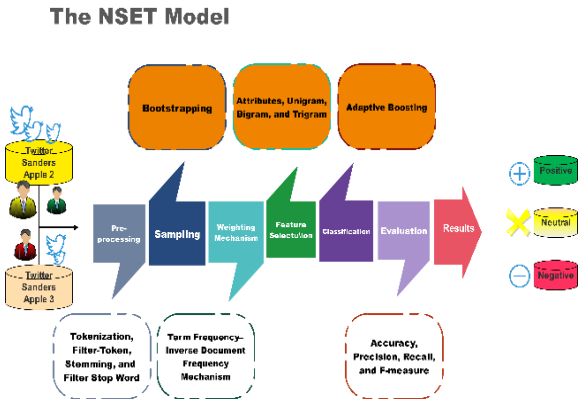

Fig. 4: The steps of the NSET for Twitter Sentiment Classification.

A. Preprocessing

Preprocessing stages including Tokenization, Filtering Token, Stemming, Filtering Stop Word, and N-grams. First, useless characters and words tokenized. Each tweet convert in a sequence of tokens and filters based on their length. The root of each word found through stemming. According to the stop word list, the stop words in each tweet eliminated and filtered.

B. Sampling

Here, attribute subset selection techniques used to improve the classification performance. Bootstrapping technique applied to obtain higher accuracy in our NSET model. This type of sampling applied sampling with replacement. So, the sample may not have all unique examples. Once an example selects, it remained a candidate for selection and can choose again. Additionally, it may generate a sample that is greater in size than the original dataset [39]. When a tuple selected, it has equal probability to select and add to the training set again.

C. Weighting Mechanism

TFIDF weighing mechanism used to produce word vector. It consists of two ratings, regularity and inverse regularity of phrase. Inverse document frequency investigated by splitting the number of records. TFIDF mechanism defined as in

$$TFIDF = TF \,.\, Log\,(N / F_t) \tag{10}$$

TF is the frequency of word t in document d, N is the number of documents, and Ft is the number of documents, including word t. It did not assign high scores to frequent words [40].

D. Feature Selection Methods

Feature selection methods extract a subset of features from all possible lists of features in the dataset to present the prediction results. These methods work at two levels: first, the selection of the subset of attributes through an attribute evaluator algorithm, and second is

the evaluation of the search heuristics via a search algorithm. Feature selection can be done in three ways:

• Evaluating the performance of the set of attributes by using a specific classifier, namely wrapper method.

• Selecting attributes as a filter in the preprocessing phase of data analytics.

• Selecting a set of attributes as a unigram, bigram, and trigram in the preprocessing phase of data analytics.

E. Classification

Ensemble methods apply multiple models to obtain better predictive performance than could be obtained from any of the constituent models. Ensembles may become more flexible in the functions. However, some ensemble techniques, especially bagging, tend to reduce problems related to over-fitting of the training data. Empirically, ensembles tend to yield better results when there is significant diversity among the models. Boosting is an ensemble method that can be used in conjunction with many other learning algorithms to improve their performance.

AdaBoost is a nested method and tries to build a better model using the learner provided in its subprocess. AdaBoost is a meta-algorithm and can be used in conjunction with many other learning algorithms to improve their performance. AdaBoost is sensitive to noisy data and outliers. However, it can be less susceptible to the overfitting problem than most learning algorithms.

The classifiers it uses can be weak, but as long as their performance is not random, they will improve the final model. To sum up, we used AdaBoost in conjunction with the SVM classifier [41].

Here, the pseudo-code of our model expressed as:

Pseudo-code for the NSET model

```
while (Website is Online) do
TW=Get-T (Tweets)
for each tweet in TW do
    Tokenizing, Splitting, Filtering, Stemming,
   Omitting Stop words, and Generating N-gram
 end for
W=Pre-process (a set of words)
W-s=Sample (W)
for each set of words in W-s do
    Constructing a word vector via TFIDF schema
 end for
WV=Get-TFIDF (a set of weights)
F=Feature-Selection (WV)
for each word vector in F do
    Applying the bootstrapping, storing the results
    Applying the SVM classifier
 end for
Best-F=SVM-Classifier (F)
Model=Ensemble (Best-F)
Per=Evaluation (Model)
end while
```

Here, the pseudo-code of our ensemble expressed as:

Pseudo-code for the Ensemble

```
for each classifier do
    W=Weigh-Vote (F)
    C=Predict (W)
  Add W to weight for the class
 end for
return the class with the biggest weight
```

Results and Discussions

Here, measures for evaluating SC introduced. P and N are the numbers of positive and negative tuples. TP refers to the positive tuples that correctly labeled by the classifier. TN refers to the number of true negatives. FP is the negative tuples that incorrectly labeled as positive. FN is the positive tuples that mislabeled as negative. Accuracy is the sum of actual tuples that classified TP and the number of TN relative to the total number of classified instances. Precision stated as the percentage of tuples that labeled as positive and actual. Recall refers to the percentage of tuples that labeled positive. F-measure combines precision and recall into a single measure [39]. F-measure comes from a weighted harmonic mean of precision and recall. Also, mean absolute error (MAE) and root absolute error (RAE) for error evaluation employed. These measures computed in Eq. (11) to (16) [42]-[43].

$$Accuracy = \frac{TP + TN}{P + N} \tag{11}$$

$$Precision\,(P) = \frac{TP}{TP + FP} \tag{12}$$

$$Recall\,(R) = \frac{TP}{P} \tag{13}$$

$$F - measure = \frac{2PR}{P + R} \tag{14}$$

$$MAE = \frac{\sum_{i=1}^{n} |y_i - x_i|}{n} \tag{15}$$

$$RAE = \frac{\sum_{i=1}^{n} |x_i - \overline{x_i}|}{\sum_{i=1}^{n} |y_i - \overline{y_i}|} \tag{16}$$

F. Dataset

Two datasets prepared by Niek Sanders applied. However, the datasets used in other studies are not

openly available, except for Sanders. You can found it in this address, http://www.sananalytics.com. The detailed information of two corpora shown in Table 1.

Table 1: A description of the used datasets

Datasets	Number of instances	Number of instances in classes		
		Positive	Negative	Neutral
TSA2	479	163	316	-
TSA3	988	163	316	509

Dataset 1: This dataset is a subset of TSA and consists of 479 tweets. There are 163 positive and 316 negative tweets in the given dataset.

Dataset 2: This dataset is also a subset of TSA and contains 988 tweets. It has three classes having 163 positive, 316 negative, and 509 neutral tweets.

G. Experiments

To achieve state-of-the-art results R implementation applied to conduct experiments on the sanders dataset. The accuracy and efficiency of the NSET model examined. The experiments try to evaluate the effectiveness of n-grams and sampling. Moreover, the impact of the ensemble method and the combination of preprocessing techniques estimated.

Assumptions**:** The default setting chosen in all experiments. For classification, a supervised method of SVM as a base learner used to receive the highest performance and combine supervised and ensemble methods. In our previous work, experiments showed that SVM is one of the best classifiers on the TSA dataset. The linear kernel and the value for the parameter epsilon=1.0 for LibSVM (C-SVC) determined by cross-validation. All related parameters set optimal. For cross-validation, 10-fold using shuffled used in all experiments.

Experiment I. The first experiment investigated the effect of the TFIDF mechanism and n-grams on the evaluation metrics using AdaBoost and sampling on TSA2. We used Term Frequency and TFIDF mechanisms in the primary preprocessing stage. However, it reveals that the Term Frequency mechanism cannot improve performance. The TFIDF weighting mechanism was useful. Hence, the TFIDF mechanism considered both experiments. We showed that 10-fold cross-validation with shuffled often is better than a stratified one. Moreover, the data using bootstrapping sampling reduced. The obtained results obtained shown in Table 2.

The highest results in each column of the table marked as bolded text. The highest accuracy highlighted at 90.61%. Also, this result achieved when used bigrams. Bigrams provide a good balance among unigrams and an ability to obtain the sentiment expression patterns. However, SVM confuses when trigrams used. It found that the highest f-measure is 93.52%, which belongs to bigrams.

Experiment II. The second experiment investigated the effect of the TFIDF mechanism and n-grams on the evaluation metrics using AdaBoost and sampling on the TSA3.

We showed that 40-fold cross-validation with stratified is better than shuffled one for this dataset. Therefore, 10-fold cross-validation using stratified used in this experiment. Also, the data using bootstrapping sampling reduced. The obtained results showed in Table 3.

The highest accuracy highlighted 87.65%, which belongs to the unigram feature. However, SVM confuses when n-gram with higher levels applied. The highest f-measure obtained at 89.64%.

Table 2: The performance of the NSET on the TSA2 (%)

N	ACT / PRE	Confusion matrix		Results			
		POS	NEG	P	R	F	A
1	POS	113	11	91.13	75.84	82.78	90.19
	NEG	36	319	89.86	96.67	93.14	
2	POS	109	5	95.61	73.15	82.89	90.61
	NEG	40	325	89.04	98.48	93.52	
3	POS	105	5	95.45	70.47	81.08	89.77
	NEG	44	325	88.08	98.48	92.99	

Note: ACT= Actual, POS=Positive, NEG=Negative, PRE=Prediction, P=Precision, R=Recall, F=F-measure, A=Accuracy

As shown in Fig. 5, the highest accuracy obtained when bigrams used. But this matter was not verified for TSA3.

Fig. 6 compares the evaluation metrics for the NSET on the datasets. Also, the error indices of two experiments show that the obtained results can be good enough (Table 4).

For TSA2, all results are higher than those of TSA3. Besides, the values of precision are above 95% for both datasets.

We showed that the NSET make a batter for binary classification according to these datasets. Nonetheless, this model outperforms the existing methods for multiple classification tasks.

Table 3: The performance of the NSET on the TSA3 (%)

N	ACT PRE	Confusion matrix POS	NEG	NEU	Results P	R	F	A
1	POS	121	2	4	95.28	70.35	80.94	
	NEG	4	243	19	91.35	83.51	87.25	87.65
	NEU	47	46	502	84.37	95.62	89.64	
2	POS	119	3	8	91.54	69.19	78.81	
	NEG	6	239	18	90.87	82.13	86.28	86.74
	NEU	47	49	499	83.87	95.05	89.11	
3	POS	118	3	5	93.65	68.60	79.19	
	NEG	4	231	15	92.40	79.38	85.40	86.43
	NEU	50	57	505	82.52	96.19	88.83	

Note: ACT= Actual, POS=Positive, NEG=Negative, NEU= Neutral, PRE=Prediction, P=Precision, R=Recall, F=F-measure, A=Accuracy

Table 4: Error comparison

Experiment N0.	MAE	RAE
I	0.0876	0.0978
II	0.0977	0.0998

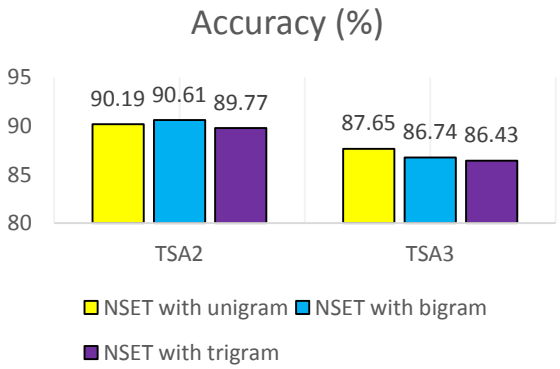

Fig. 5: The highest accuracy for the NSET based on n-grams.

H. Discussion

Here, the effects of n-grams and ensemble investigated on the TSA. The effectiveness of the suggested model examined the two datasets and compared them with the methods in Trupthi et al. [26], our previous model [27], Padmaja and Hegde [32], Vashishtha and Susan in [30], Hassan et al. [21], and Pandey et al. [4].

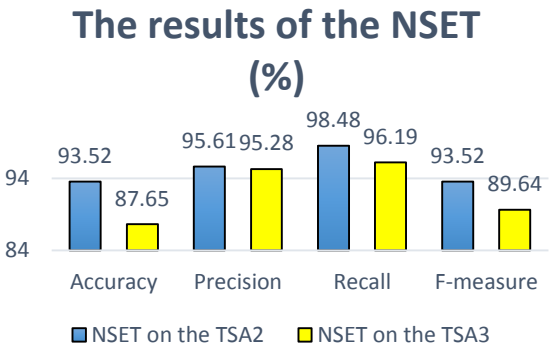

Fig. 6: The highest results for the NSET on two datasets.

The obtained results presented in two experiments and validated that the NSET outperforms the existing methods on the datasets, except for the achieved accuracy on the TSA2. Fig. 7 illustrates the performance of the NSET model and others in terms of accuracy. The highest accuracy gained 92.78% by Padmaja and Hegde [32] on the TSA2 and 82.2% by Pandey et al. [4]. In the TSA3, whereas the NSET received 90.61 and 87.65% for TSA2 and TSA3, respectively. However, we examine more alternatives to improve accuracy.

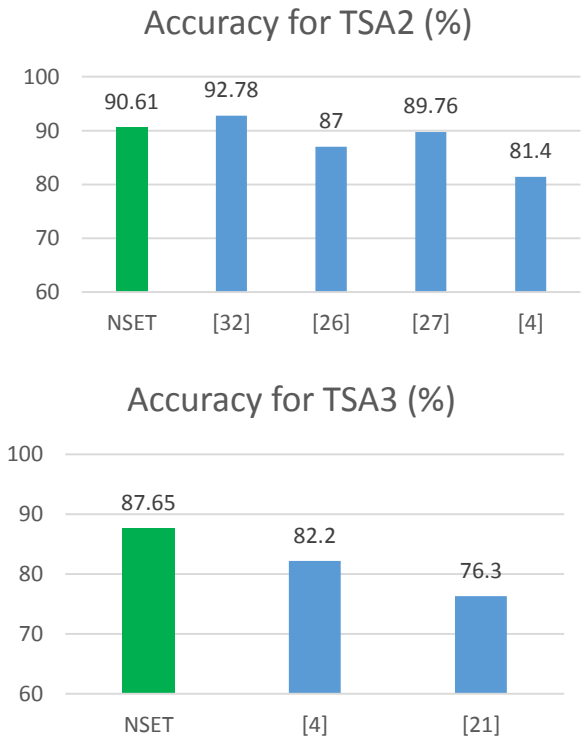

Fig. 7: The comparison of accuracy among the NSET and others.

Fig. 8 illustrates the performance of the NSET model and others in terms of precision. The best precision in

the literature achieved 90.4% by our previous model [27] on the TSA2 and 82.34% by Pandey et al. [4] on the TSA3. The highest precision gained 95.25% by the NSET, whereas Padmaja and Hegde [32] obtained 85.2%. It was approximately 10% higher than that one. We show that bigram features can work well using our model on the TSA2, but with the increasing to trigram, the embedded SVM in our mode confuse and it cannot improve more. Besides, the increase of n in the model causes few improvements in some cases of the TSA3. It also revealed that our model is better than the proposed model by Pandey et al. [4] through a cuckoo search on the TSA3. It finds that an uncomplicated and accurate model can be good enough in this context.

Fig. 9 illustrates the performance of the NSET model and others in terms of recall. On the other hand, the best recall of the NSET gained 98.48% on the TSA2, but Padmaja and Hegde [32] obtained 90.05%. This value for Trupthi et al.

[26] and our previous model [27] achieved 89.06 and 85.4%, respectively. It is also shown that the recall of our model received 96.19% on the TSA3; whereas, Pandey et al. [4] obtained 80.16%, an increase of approximately 16%. These differences revealed that the best criteria can be the f-measure.

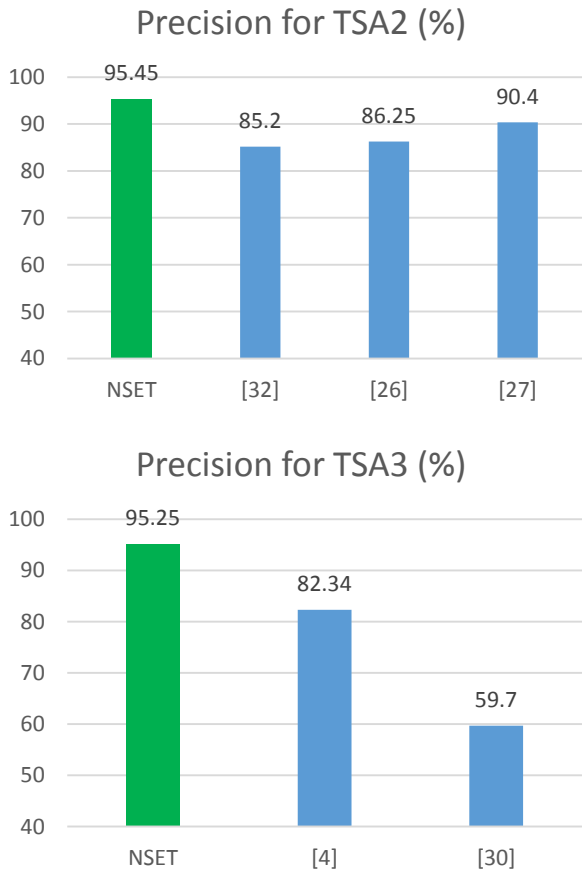

Fig. 8: The comparison of precision among the NSET and others.

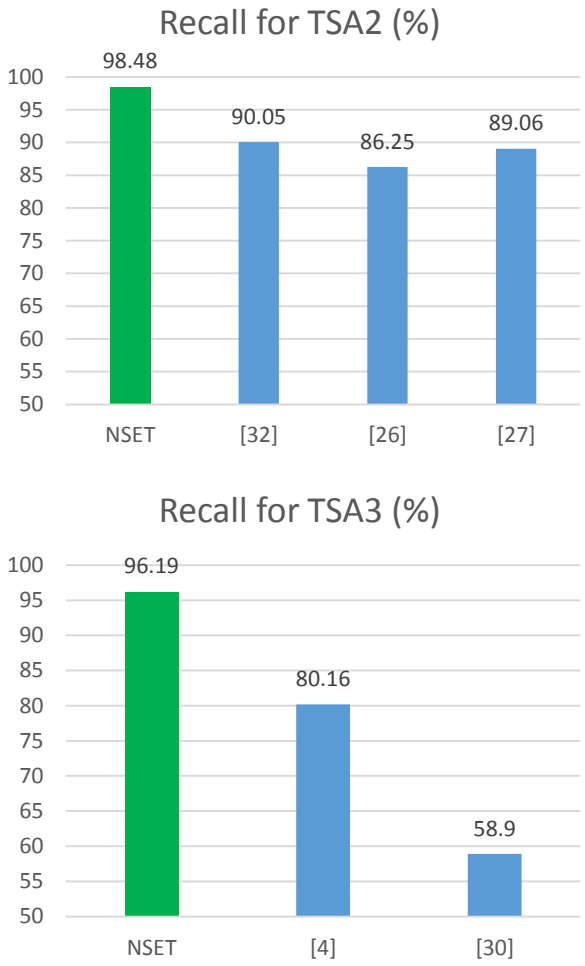

Fig. 9: The comparison of recall among the NSET and others.

It reflects the highest f-measure gains in both datasets. The f-measure for the comparison works is of concern in Fig. 10.

It is clear from the comparison that the NSET shows better accuracy for classification. It is a notable difference between the models. The highest f-measure reached 93.52% by our model on TSA2; whereas, Padmaja and Hegde [32] obtained 89.73%, approximately 4% more. The best f-measure of the NSET gained 89.64%; whereas, the highest f-measure in the literature received 81.25% by Pandey et al. [4] on the TSA3.

The results showed that the NSET is more accurate than its predecessors. It showed that the combination of TFIDF, sampling, and n-gram is a good alternative for both used datasets.As a limitation in the used dataset, the tweets are very short in the TSA3. Therefore, the obtained results have not a significant improvement, and these are the same approximately in this dataset. For this reason, we want to work more in the preprocessing stage to choose the best feature in this dataset.

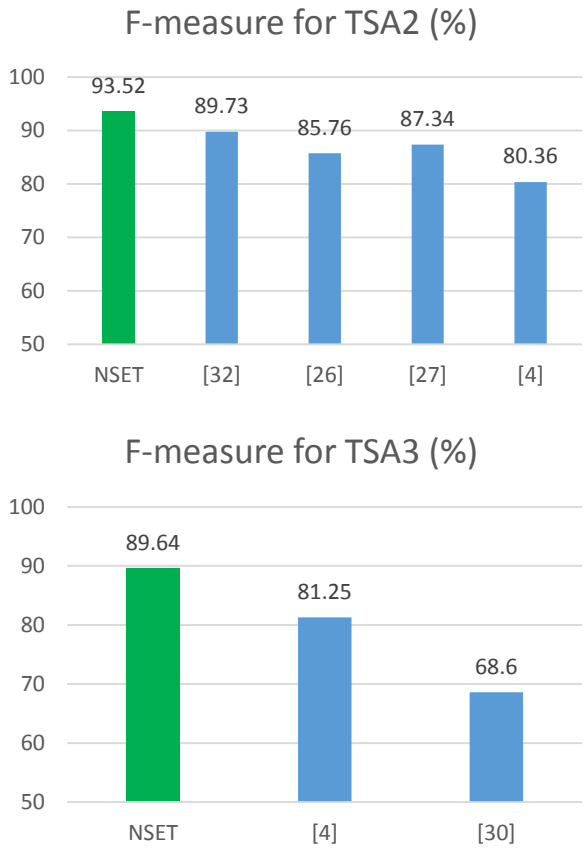

Fig. 10: The comparison of f-measure among the NSET and others.

Conclusion

The NSET suggests a model for both binary and multiple classifications, which classify the dataset into positive, negative, or neutral classes. Compared to the existing studies on Twitter SC which, either depends on sophisticated features or complicated learning procedure, the NSET is more simple and straightforward. The effect of n-grams using the ensemble method and sampling technique on the Twitter datasets is investigated. The highest f-measure achieved 93.52%, which belongs to bigrams. Bigram features construct the relationship of words to improved results. Experimental results demonstrated that the present model outperforms the existing methods based on two experiments on the datasets. Maximum precision obtained 95.45%, an increase of 10%. The NSET is very redeeming in comparison to others since it applied more related words using n-grams and sampling techniques.

The results revealed that the NSET is more accurate than its predecessors. It is also shown that the combination of TFIDF, sampling, and n-gram is a good alternative for both datasets. Our findings exposed that bigram features are well only in the TSA2; whereas, unigrams achieved the best performance for the TSA3. It revealed that our model works better than the other methods based GA in [32], cuckoo search in[4], ensembles in [21], fuzzy rules in [26], [30], and supervised techniques in [27].

We believe that performance can still be improved. As future work, we aim to study the use of heuristic algorithms as a way to improve feature selection and reduce the feature.

Authors contributions

R. Asgarnezhad designed the experiments, carried out the data analysis, interpreted the results and wrote the manuscript. S. A. Monadjemi corrected the proofing the article. Soltanaghaei supported the article.

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Conflict of Interest

The authors declare that they have no conflict of interest.

Abbreviations

TFIDF	Term Frequency-Inverse Document Frequency
$\mu k = c$	The column K mean and the row belongs to the class C
$\sigma^2_{k=c}$	The variance of the kth
Z(d)	A normalization function
$F_{i,c}$	A function for feature F_i and class *c*
m	The count of the selected features
P	The dataset
$\{(x_1,c_1),(x_2,c_2),...,(x_n,c_n)\}$	A set of data points
x_i	A p-dimensional vector of real numbers
TF	The frequency of word *t* in document *d*
N	The number of documents
Ft	The number of documents including word *t*
MAE	Mean Absolute Error
RAE	Absolute Error

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Research paper

Designing a new robust control for virtual inertia control in the microgrid with regard to virtual damping

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Abstract

Background and Objectives: Virtual inertia control, as a component of a virtual synchronous generator, is used for the implementation of synchronous generator behaviour in microgrids. In microgrids that include high-capacity distributed generation resources, in addition to virtual inertia, virtual damping can also lead to improvement of frequency stability of the microgrid. The purpose of the control method for the islanded microgrid is to be: 1) robust to the uncertainty of the microgrid parameters. 2) Weaken the disturbances on the islanded microgrid (wind turbine, solar cell, Loads). 3) Improved response speed related to microgrid frequency deviation (reduced settling time).

Methods In this paper, designing a new robust control method for controlling virtual inertia in microgrids, with regard to virtual damping, has been attempted. The proposed method has a higher degree of freedom compared to the conventional robust controllers, which provides better control of the system.

Results: Results of the proposed method for virtual inertia control with regard to virtual damping has been compared in several scenarios –with virtual inertia control based on optimized PI controllers with regard to virtual damping, virtual inertia control based on model predictive control (controller) with regard to virtual damping, Self-adaptive virtual inertia control using fuzzy logic, virtual inertia control with regard to virtual damping, and virtual inertia control without virtual damping (conventional methods). Compared to other control methods, the proposed controller has improved the settling time due to the frequency deviations of the islanded microgrid by 27%. According to the results of the scenarios, the proposed controller has been able to reduce the frequency error due to load and distributed generation resource disturbances and compared to other controllers, and this frequency deviation has been reduced by 68%.

Conclusion: According to the simulation results, the proposed controller has a better performance than other controllers in improving the frequency stability of the islanded microgrid.

Introduction

Due to the increasing need for power generation, the distributed generation resources have penetration into the power system and have gradually replaced conventional systems [1], [2]. Wind Turbines and solar cells (Photovoltaic) are among the most widely used sources of production in the power system [3], [4]. Since these sources exchange power with the microgrid through power electronic converters, when a disturbance occurs in the microgrid, it causes higher

frequency and voltage deviations in the system due to the low inertia of the system (power electronic converters) [5], [6]. Increasing the capacity of distributed generation sources such as wind turbines and Photovoltaic (PV) in the microgrids more and more will cause many problems in the stability of voltage and frequency due to the lack of inertia, compromising the stability of the microgrid [7]-[9]. Thus, the concept of the virtual synchronous generator (VSG) in the microgrid was introduced to implement the behavior of synchronous generators of the power system. Implementing this method improves the inertia, output impedance, and stability of the microgrid [10]-[12].

Virtual inertia control is a special part of the virtual synchronous generator (VSG). The virtual inertia control can be implemented on energy storage systems (ESS), enabling them to operate like traditional synchronous generators. As a primary stimulus, the virtual inertia control can improve the frequency stability with the occurrence of disturbances in the microgrid [13], [14]. In microgrids, in addition to virtual inertia, the existence of virtual damping can help improve frequency stability. For example, when load disturbance occurs, virtual inertia, as a prime mover, prevents too much frequency decline, and the existence of virtual damping provides more damping to the microgrid (Fast damping of fluctuations). Various control methods have been used for virtual inertia to improve the frequency stability of the islanded microgrid. The control method used for virtual inertia must meet the following objectives.

1) It is robust to the uncertainty of the microgrid parameters.

2) Weaken the effect of disturbance on the microgrid frequency.

3) Improve the response speed to the islanded microgrid frequency deviations.

Control methods for virtual inertia control in the islanded microgrid can be divided into two categories: 1) Controller design for virtual inertia control without considering virtual damping [15]-[24]. 2) Controller design for virtual inertia with considering virtual damping [25].

In [15], the PI controller (proportional-integral controller) has been used to control virtual inertia control in the AC/DC microgrid. A control method for an electric vehicle has been provided in the microgrid based on the virtual inertia control method using a PI controller [16]. The PI controller used for virtual inertia does not perform well against the uncertainty of microgrid parameters as well as disturbances. In [17], the researchers have employed the coefficient diagram method as a robust controller to virtual inertia control in the islanded microgrids. The coefficient diagram method used for virtual inertia performs well against the uncertainty of microgrid parameters but does not perform well in attenuation of disturbance. In [18], an adaptive control method has been applied to virtual inertia control in the microgrid to improve frequency stability. The adaptive control method is robust to disturbance and uncertainty of microgrid parameters, but the response speed does not well. In [19], the researchers have focused on the design of a neural-fuzzy controller to virtual inertia control in the islanded microgrids. The neural-fuzzy controller is unable to weaken the disturbances on the islanded microgrid. In [20], an H∞ controller has been designed to virtual inertia control in the microgrid with the influence of distributed generation sources. In [21], it has been focused on the design of Adaptive Virtual Inertia Control-Based Fuzzy Logic in the microgrid with the influence of distributed generation sources aimed at improving frequency stability. In [22], the researchers have designed an H∞ controller to the virtual inertia control in the microgrid by considering the phase-locked loop in the microgrid model. The control methods used in [22] are robust to disturbance and uncertainty of microgrid parameters, but the settling time (response speed) of the islanded microgrid frequency deviations is long. In [23], a model predictive control (controller) has been designed to the virtual inertia control in the microgrid targeted to improve frequency stability. The model predictive control (controller) performs well against disturbances, but is not relatively robust to the uncertainty of microgrid parameters. A virtual inertia controller has been designed for an islanded microgrid with two areas in [24]. In [25], virtual inertia control with regard to virtual damping has been designed for islanded microgrids. The control method used in [25] has a good settling time (response speed) but is not robust to disturbances and uncertainty of island microgrid parameters. Therefore, it is necessary to have a proper control method that can be resistant to the uncertainty of the parameters of the islanded microgrid and can weaken high disturbances and also have a suitable response speed.

In this paper, a new robust control method of output feedback based on linear matrix inequality for virtual inertia control with regard to virtual damping for the islanded microgrids has been utilized. The proposed control method does not require measuring of all the modes and uses only output feedback. The proposed method has a higher degree of freedom compared to the conventional robust controllers, which provides better control of the system. In the proposed method, all the uncertainties related to the microgrid parameters are considered and the criterion for weakening the disturbance is also considered in it. The purpose of the control method is to be: 1) robust to the uncertainty of

the microgrid parameters. 2) Weaken the disturbances on the islanded microgrid (wind turbine, solar cell, Loads). 3) Improved response speed related to microgrid frequency deviation (reduced settling time). Results of the proposed method for virtual inertia control with regard to virtual damping has been compared in several scenarios - with the consideration of the uncertainty of islanded microgrid parameters as well as disturbances imposed upon the microgrid - to virtual inertia control based on optimized PI controllers with regard to virtual damping, virtual inertia control based on model predictive control (controllers) with regard to virtual damping, Self-adaptive virtual inertia control using fuzzy logic, virtual inertia control with regard to virtual damping, and virtual inertia control without virtual damping (conventional methods), and performance of the proposed method with respect to response speed, decrease in frequency deviation, and robustness to parameter uncertainty and disturbances imposed upon the islanded microgrid is shown.

The proposed method has been verified based on Lyapunov's criteria. Simulation has been performed in Matlab Software.

The article includes the islanded microgrid structure, designing a new robust controller for islanded microgrids, simulation, and conclusion.

Microgrid Structure

A. Virtual inertia control with regard to virtual damping on the islanded microgrid

The objective of designing a virtual inertia control system is providing the appropriate virtual inertia and damping in microgrids that possess vast distributed generation resources. Since this microgrid does not possess adequate inertia in comparison to power systems, this control section operates as a separate control section to maintain microgrid frequency stability in the transient and steady states [15]-[24]. In Fig. 1, the dynamic model (microgrid) of virtual inertia control with consideration of virtual damping is shown.

The virtual inertia control is a derivative control in which the frequency variations rate is added as the additional active power to the reference microgrid during disturbances and incidents acting on the microgrid. Virtual damping has also been used for more rapid damping of microgrid frequency deviation [17], [25]. The derivative control, which is highly sensitive to the frequency measurement noises, uses a low-pass filter to solve this problem. The low-pass filter simulates the behavior of an energy storage system (ESS) [17].

Therefore, virtual inertia control with regard to virtual damping prevents microgrid frequency instability and improves microgrid inertia and damping.

B. Components of the islanded microgrid

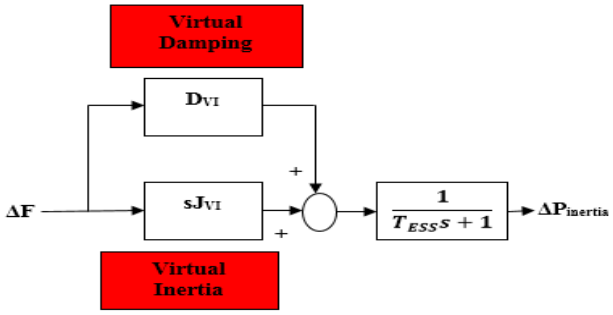

Fig. 1: Dynamic model of virtual inertia control in the microgrid with regard to virtual damping [25].

Fig. 2 shows the structure of the islanded microgrid. The studied microgrid consists of a 15 MW of a thermal power plant, 7.5 MW of a solar farm, 8.5 MW of a wind farm, and 4.5 MW of energy storage system (ESS). The microgrid also consists of two types of load: 10 MW of industrial load and 5 MW of a residential load [25]. Virtual inertia control with consideration of virtual damping is implemented to the energy storage system, as a compensator, is expected to support the load-frequency control system in keeping a balance between production and consumption in the microgrid [20]. The dynamic model of the islanded microgrid is shown in Fig. 3. The model used for the islanded microgrid components was a reduced-order model, which is a proper model for frequency stability analysis in microgrids. According to Fig. 3, three control structures were considered to enable the islanded microgrid function well against disturbances and improve the frequency stability in the islanded microgrid: virtual inertia control, Primary control and secondary control (LFC) [18]-[25]. For designing a controller for virtual inertia control with consideration of virtual damping in the islanded microgrid, at first, the state-space model of the islanded microgrid was attained, and was proceeded with designing the proposed control method for virtual inertia control with consideration of the microgrid virtual damping.

C. State-space model of the islanded microgrid

The state-space model of the islanded microgrid for virtual inertia control with regard to virtual damping to improve the frequency stability is shown as (1). The disturbances on the islanded microgrid are shown in (2) [22]-[25]. In (1) and (2), Δf is the microgrid frequency deviation. ΔP_W is the generated from the wind turbine. ΔP_g is generated from the governor. ΔP_{ACE} is generated from the area control. $\Delta P_{inertia}$ is generated from virtual inertia power. ΔP_{PV} is generated from the solar power. ΔP_I is commercial load power, and ΔP_R is residential load power.

Designing a new robust controller for virtual inertia control with consideration of virtual damping

A. The proposed controller structure

The new robust control method has been designed for virtual inertia control with consideration of virtual damping in the islanded microgrid. The controller structure is designed in such a way that there is the uncertainty of parameters and disturbance in the studied islanded microgrid. Also, we cannot measure all states and modes, and even if it can, it will cost more due to the need for more sensors. The control system is designed in such a way that the islanded microgrid would be free of external disturbances and under the uncertainty of parameters with an asymptote stable output feedback and can meet the $\frac{\|z\|_{L_2}}{\|w\|_{L_2}} \le \gamma$ criterion in the presence of disturbances in the microgrid. The structure of the islanded microgrid (with parameter uncertainty and under disturbance) for virtual inertia control (with virtual damping) with the proposed dynamic controller is shown in Fig. 4. In Fig. 4, y is the frequency deviation of the islanded microgrid, D is disturbance entering the islanded microgrid, and u is control signal. The dynamics of the islanded microgrid is modeled by considering the regulated output (Z) as (3).

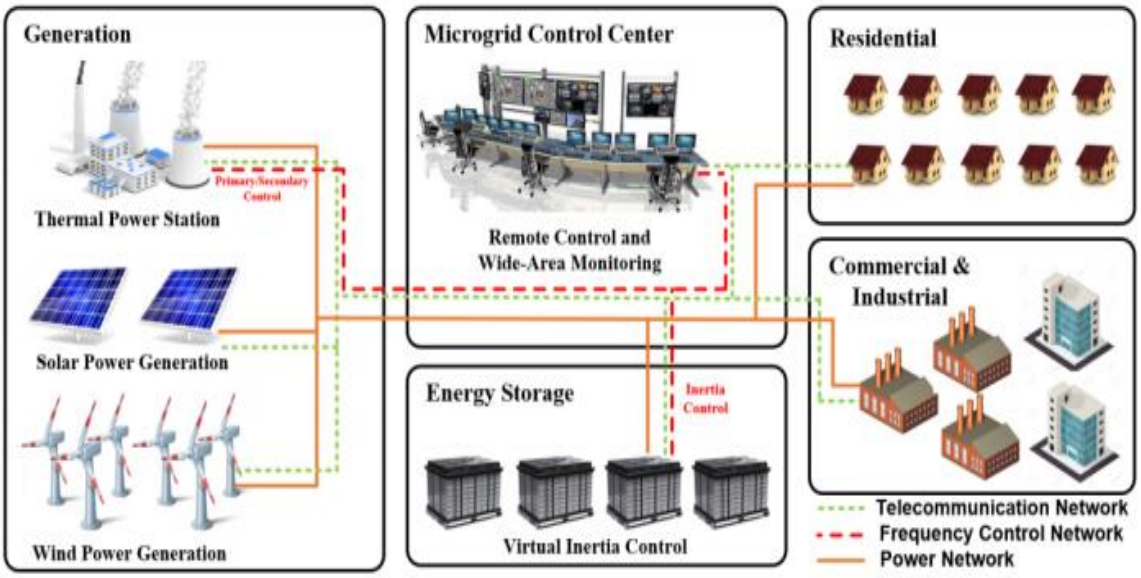

Fig. 2: The structure of the islanded microgrid [24], [25].

$$\begin{bmatrix} \dot{\Delta f} \\ \dot{\Delta P_m} \\ \dot{\Delta P_g} \\ \dot{\Delta P_{ACE}} \\ \dot{\Delta P_{inertia}} \\ \dot{\Delta P_W} \\ \dot{\Delta P_{PV}} \end{bmatrix} = \begin{bmatrix} \frac{-D}{2H} & \frac{1}{2H} & 0 & 0 & \frac{1}{2H} & \frac{1}{2H} & \frac{1}{2H} \\ 0 & \frac{-1}{T_t} & \frac{1}{T_t} & 0 & 0 & 0 & 0 \\ \frac{-1}{RT_g} & 0 & \frac{-1}{T_g} & \frac{-1}{T_g} & 0 & 0 & 0 \\ \beta K_i & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{D_{VI}}{T_{ESS}} & 0 & 0 & 0 & \frac{-1}{T_{ESS}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{T_{WT}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{T_{PV}} \end{bmatrix} \begin{bmatrix} \Delta f \\ \Delta P_m \\ \Delta P_g \\ \Delta P_{ACE} \\ \Delta P_{inertia} \\ \Delta P_W \\ \Delta P_{PV} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \frac{J_{VI}}{T_{ESS}} \\ 0 \\ 0 \end{bmatrix} [u] + \begin{bmatrix} 0 & 0 & \frac{-1}{2H} & \frac{-1}{2H} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{T_{WT}} & 0 & 0 & 0 \\ 0 & \frac{1}{T_{PV}} & 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta P_{solar} \\ \Delta P_{wind} \\ \Delta P_I \\ \Delta P_R \end{bmatrix}$$

$$y = [1 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0] \begin{bmatrix} \Delta f \\ \Delta P_m \\ \Delta P_g \\ \Delta P_{ACE} \\ \Delta P_{inertia} \\ \Delta P_W \\ \Delta P_{PV} \end{bmatrix} \tag{1}$$

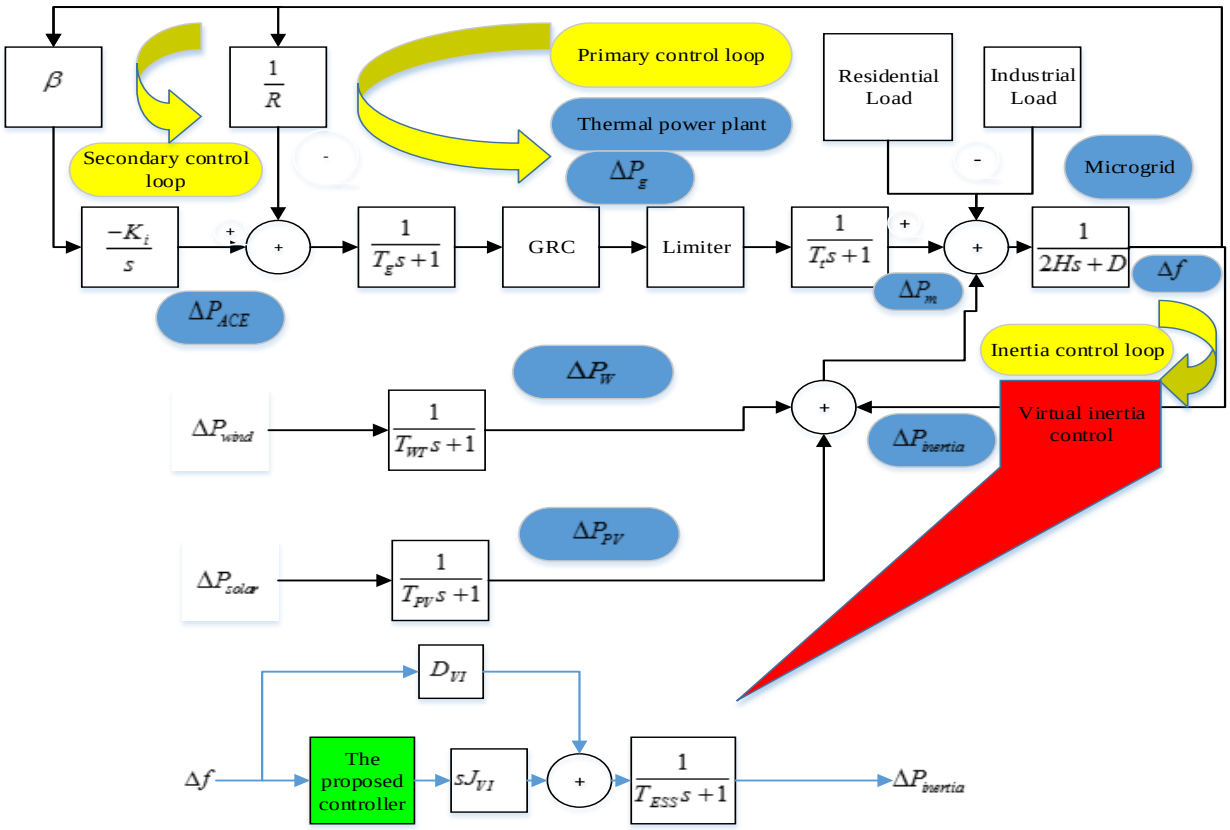

Fig. 3: The dynamic model of the islanded microgrid [23].

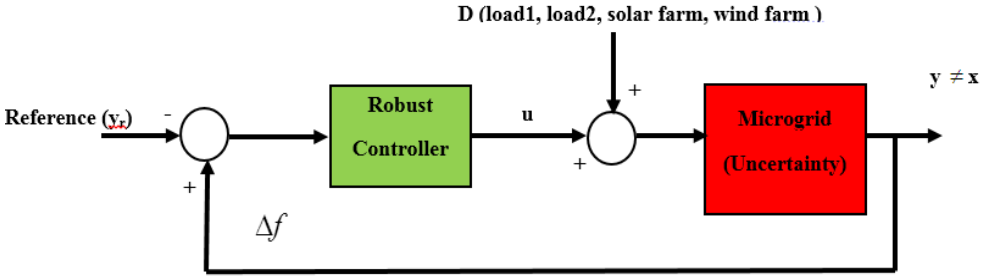

Fig. 4: The Islanded microgrid structure with proposed controller.

$$w^T = [\Delta P_{solar} \quad \Delta P_{wind} \quad \Delta P_I \quad \Delta P_R] \tag{2}$$

$$\begin{aligned} \dot{x} &= A_{n\times n}(t)x_{n\times 1} + B_{n\times m}(t)u_{m\times 1} + D_{n\times d}(t)w_{d\times 1} \\ z &= C_{1_{q\times n}}(t)x_{n\times 1} + D_{11}(t)w + D_{12_{q\times m}}(t)u_{m\times 1} \\ y &= C_2(t)x_{n\times 1} + D_{21}(t)w + D_{22}(t)u \end{aligned} \tag{3}$$

Z is a virtual output that is only used for design and is selected so that it achieves the desired goals for the islanded microgrid. Z is a more general case than y (system output). In this article, z is the same as the frequency deviation of the islanded microgrid, on which the effect of disturbances (wind farm, solar farm, and load) is weakened.

In (3), $A_{n\times n}$ is the system matrix, $B_{n\times m}$ is the input matrix, $D_{n\times d}$ is the disturbance matrix, $C_{1_{q\times n}}=C_2$ is the output matrix, *n* is the number of state variables, *m* indicates the control inputs, *d* is the number of disturbances, and $D_{21}(t)=D_{22}(t)=0$. *y* is the linear system measurement output (frequency deviation of the islanded microgrid), and *q* is the number of regulated outputs [26]. Since in the islanded microgrid, $C_2 \neq I$, the robust output feedback control has been used. The variable *z* can be selected with regard to the control design criterion. In the proposed method, all the parameters of the linear system can be assumed uncertain, so it has been modeled as (4) [26]-[28]. The uncertainty given in (4) has been re-considered as in (5) (structure bonded), wherein *F(t)* has been taken as 1×1. In (5), the choice of M and N parameters is the responsibility of the designer. The structure of the dynamic controller proposed for virtual inertia control

(with consideration of virtual damping) in the islanded microgrid has uncertainty and disturbance, which is represented as (6).

$$\left\{\begin{array}{l} A(t)=A+\Delta A(t)=A+\Delta A \\ B(t)=B+\Delta B(t)=B+\Delta B \\ D(t)=D+\Delta D(t)=D+\Delta D \\ C_1(t)=C_1+\Delta C_1(t)=C_1+\Delta C_1 \\ D_{12}(t)=D_{12}+\Delta D_{12}(t)=D_{12}+\Delta D_{12} \\ C_2(t)=C_2+\Delta C_2(t)=C_2+\Delta C_2 \end{array}\right\} \quad (4)$$

$$\left\{\begin{array}{l} \Delta A_{n\times n}=M_{A_{n\times 1}}F_{1\times 1}(t)N_{A_{1\times n}} \\ \Delta D_{n\times d}=M_{D_{n\times 1}}F_{1\times 1}(t)N_{D_{1\times d}} \\ \Delta B_{n\times m}=M_{B_{n\times 1}}F_{1\times 1}(t)N_{B_{1\times m}} \\ \Delta C_{1_{q\times n}}=M_{C1_{q\times 1}}F_{1\times 1}(t)N_{C1_{1\times n}} \\ \Delta C_{2_{p\times n}}=M_{C2_{p\times 1}}F_{1\times 1}(t)N_{C2_{1\times n}} \\ \Delta D_{12_{q\times m}}=M_{D12_{q\times 1}}F_{1\times 1}(t)N_{D12_{1\times m}} \\ F_{1\times 1}^T(t)\times F_{1\times 1}(t)\le I, F^2(t)\le 1 \end{array}\right\} \quad (5)$$

$$\left\{\begin{array}{l} \dot{\hat{x}}_{n\times 1}=\hat{A}_{n\times n}\hat{x}_{n\times 1}+\hat{B}_{n\times p}y_{p\times 1} \\ u_{m\times 1}=\hat{C}_{m\times n}\hat{x}_{n\times 1} \end{array}\right\} \quad (6)$$

By combining (3) and (6), the closed-loop system structure (the islanded microgrid and controller) can be represented as in (7).

$$\left\{\begin{array}{l} \dot{x}=A(t)x+B(t)\hat{C}\hat{x}+D(t)w \\ z=C_1(t)x+D_{12}(t)\hat{C}\hat{x} \\ \dot{\hat{x}}=\hat{A}\hat{x}+\hat{B}C_2x \end{array}\right\} \quad (7)$$

In (7), if $\hat{x}$ and x incline toward zero, then the entire closed-loop system will be stable. Considering $\bar{x}=\begin{bmatrix} x \\ \hat{x} \end{bmatrix}_{2n\times 1}$, Equation (7) is rewritten as (8).

$$\dot{\bar{x}}=\begin{bmatrix} A(t) & B(t)\hat{C} \\ \hat{B}(t)C_2(t) & \hat{A} \end{bmatrix}_{2n\times 2n}\bar{x}+\begin{bmatrix} D(t) \\ 0 \end{bmatrix}_{2n\times d}w_{d\times 1}=\bar{A}\bar{x}+\bar{D}w \quad (8)$$

B. Objectives of the control system

For the closed-loop system (The islanded microgrid system with disturbance and parameter uncertainty and the proposed controller), there are 2 main objectives:

1. Being asymptotically stable without disturbance of the closed-loop system and under parameter uncertainty.

2. Achieving the performance of in the presence of disturbance and uncertainty of the closed-loop system with the primary zero conditions.

In the paper, the Lyapunov stability criterion has been used to prove the stability of the proposed method. For this purpose, the Lyapunov stability criterion was applied to the islanded microgrid system with disturbance. The Lyapunov criterion and the closed-loop system structure are defined as (9). The two conditions (9(a)) and (9(c)) are essential for the stability based on the Lyapunov criterion.

$$\left\{\begin{array}{ll} v=\bar{x}^T p\bar{x}>0\Rightarrow p>0 & (9(a)) \\ \dot{\bar{x}}=\bar{A}\bar{x}+\bar{D}w & (9(b)) \\ \dot{v}=\dot{\bar{x}}^T p\bar{x}+\bar{x}^T p\dot{\bar{x}}=\bar{x}^T\bar{A}^T p\bar{x} & \\ +w^T\bar{D}^T p\bar{x}+\bar{x}^T p\bar{A}\bar{x}+\bar{x}^T p\bar{D}w<0 & (9(c)) \end{array}\right\} \quad (9)$$

To prove the (9(a)), meaning that $v>0$, the matrix P, P^{-1} is defined as (10) [26]. In (10), the matrices R, T, S, and U are symmetrical because P and P^{-1} are symmetric. Meanwhile, PP^{-1} must become an identity matrix in accordance with (11).

The linearization matrix has been considered as (12) [26]. According to (12), $p\beta_1=\beta_2$. Also, from (13) [26], the linear matrix inequality has been obtained for the first Lyapunov criterion (9(a)), meaning that if the linear matrix inequality (13) is bigger than zero, then the first criterion is met ($v>0$).

$$p=\begin{bmatrix} S_{n\times n} & N_{n\times n} \\ N_{n\times n}^T & U_{n\times n} \end{bmatrix}, p^{-1}=\begin{bmatrix} R_{n\times n} & M_{n\times n} \\ M_{n\times n}^T & T_{n\times n} \end{bmatrix} \quad (10)$$

$$pp^{-1}=\begin{bmatrix} SR+NM^T & SM+NT \\ N^TR+UM^T & N^TM+UT \end{bmatrix}=\begin{bmatrix} I_{n\times n} & 0 \\ 0 & I_{n\times n} \end{bmatrix} \quad (11)$$

$$\beta_1=\begin{bmatrix} R & I \\ M^T & 0 \end{bmatrix}, \beta_2=\begin{bmatrix} I & S \\ 0 & N^T \end{bmatrix} \quad (12)$$

$$\beta_1^T p\beta_1=\beta_1^T\beta_2=\begin{bmatrix} R & M \\ I & 0 \end{bmatrix}\begin{bmatrix} I & S \\ 0 & N^T \end{bmatrix} =\begin{bmatrix} R & RS+MN^T \\ I & S \end{bmatrix}=\begin{bmatrix} R & I \\ I & S \end{bmatrix}>0 \quad (13)$$

To calculate the second Lyapunov criterion (9(c)) and to convert it into a linear matrix inequality, Equations (14) to (29) have been proved.

The equation $\frac{\|z\|_{L_2}}{\|w\|_{L_2}} \le \gamma$, which is the criterion for reduction of disturbances compared to the islanded microgrid system's states under uncertainty, has been written in accordance with (14). The objective function has been represented as the function *j*, and the negativity of the function *j* meets the second Lyapunov criterion, i.e. $\dot{v} < 0$. The upper bound for the objective function *j* has been obtained according to (15). If (16) exists, then the function *j* will be negative, and the second Lyapunov criterion will be met. Therefore, Equation (16) must be converted into a linear matrix inequality. Equation (16) has been converted, through substitution and *Schur complement*, into (17). Since *P* is symmetric, so $P^T=P$ and $p=\beta_2\beta_1^{-1}$ and, accordingly, equation (17) has converted into (18). Equation (18) is not of the linear matrix inequality that can be solved by Yalmip, so it is necessary to make changes to the (18) that can be considered a linear matrix inequality. Equations (19) and (20) have been defined in order for linearizing (18) .The linearization of (18) has been demonstrated in accordance with (21). By substituting (8) and (12) in (21), (22) has been obtained.

$$\begin{cases} \int_0^\infty z^T z \, dt \le \gamma^2 \int_0^\infty w^T w \, dt \\ j = \int_0^\infty (z^T z - \gamma^2 w^T w) dt \le 0 \end{cases} \quad (14)$$

$$\begin{cases} j \le \int_0^\infty (z^T z - \gamma^2 w^T w) dt + v(x(\infty)) - v(x(0)) \\ j \le \int_0^\infty (z^T z - \gamma^2 w^T w + \dot{v}) dt < 0 \end{cases} \quad (15)$$

$$z^T z - \gamma^2 w^T w + \dot{v} < 0 \quad (16)$$

$$\delta_1 = \begin{bmatrix} \bar{A}^T p + p\bar{A} & p\bar{D} & \begin{bmatrix} C_1^T(t) \\ \hat{C}^T D_{12}^T(t) \end{bmatrix} \\ \bar{D}p & \gamma^2 I & 0 \\ \begin{bmatrix} C_1(t) & D_{12}(t)\hat{C} \end{bmatrix} & 0 & -I \end{bmatrix} < 0 \quad (17)$$

$$\delta_2 = \begin{bmatrix} \bar{A}^T \beta_2\beta_1^{-1} + p\bar{A} & \bar{\beta}_1^T \beta_2^T \bar{D} & \begin{bmatrix} C_1^T(t) \\ \hat{C}^T D_{12}^T(t) \end{bmatrix} \\ D\beta_2\beta_1^{-1} & \gamma^2 I & 0 \\ \begin{bmatrix} C_1(t) & D_{12}(t)\hat{C} \end{bmatrix} & 0 & -I \end{bmatrix} < 0 \quad (18)$$

Subsequently, (22), after substituting (23), HAS BEEN CONVERTED INTO (24). The definitions of the parameters $\hat{A}, \hat{B}, \hat{C}$ in (23) have been adopted from [26]-[28] and in (24), the constant parameters have been separated from the uncertain parameters by different matrices. In (24), the o matrix is linear matrix inequality, and the matrices o_1 to o_{13} are not linear matrix inequality. In (24), the matrices o_1 to o_{13} are uncertain. In order to make o_1 to o_{13} matrices appear linear matrix inequality, changes must be made in the matrices. According to (25), the above band is first defined for o_1 to o_{13} matrices. In (26), $\bar{o}_1$ to $\bar{o}_{13}$ are the up band of o_1 to o_{13} matrices Then, according to (26) and (27), the matrices $\bar{o}_1$ to $\bar{o}_{13}$ are converted to linear matrix inequality. According to (27), if $\delta_4<o$, then $\delta_3<o$ and the second Lyapunov criterion will be met. In (28), for the first time, the Schur complement is used for $\bar{o}_1$ and entered into the o-matrix. In order for all $\bar{o}_2$ to $\bar{o}_{13}$ matrices to enter the o matrix, the Schur complement is used 12 more times. And finally, the (29) is shown. Finally, Liapanov's second criterion (9-c) is shown as (29). Equation (29) is an inequality of the linear matrix in which all the uncertainties of system parameters and disturbances are modeled.

$$\begin{cases} \delta_2 < 0 \\ \varsigma > 0 \end{cases}, \varsigma^T \delta_2 \varsigma < 0 \quad (19)$$

$$\varsigma = \begin{bmatrix} \beta_1 & 0 & 0 \\ 0 & I & 0 \\ 0 & 0 & I \end{bmatrix}, \varsigma^T = \begin{bmatrix} \beta_1^T & 0 & 0 \\ 0 & I & 0 \\ 0 & 0 & I \end{bmatrix} \quad (20)$$

$$\delta_3 = \begin{bmatrix} \beta_1^T & 0 & 0 \\ 0 & I & 0 \\ 0 & 0 & I \end{bmatrix} \delta_2 \begin{bmatrix} \beta_1 & 0 & 0 \\ 0 & I & 0 \\ 0 & 0 & I \end{bmatrix} = \quad (21)$$

$$\begin{bmatrix} \beta_1^T \bar{A}^T \beta_2 + \beta_2^T \bar{A} \beta_1 & \beta_2^T \bar{D} & \beta_1^T \begin{bmatrix} C_1^T(t) \\ \hat{C}^T D_{12}^T(t) \end{bmatrix} \\ \bar{D}\beta_2 & \gamma^2 I & 0 \\ \begin{bmatrix} C_1(t) & D_{12}(t)\hat{C} \end{bmatrix} \beta_1 & 0 & -I \end{bmatrix} < 0$$

C. The New Proposed Controller Design Steps

1) State-space related to the islanded microgrid

2) Determining φ1, φ2, and φ3 (Degrees of freedom).

3) Solving the linear matrix inequality (13 & 29) and $\Gamma_1, \Gamma_2, \Gamma_3, \Gamma_4, \Gamma_5, \Gamma_6, \Gamma_7, \Gamma_8, \Gamma_9, \Gamma_{10} > 0$ using YALMIP.

4) Obtaining $L_{n\times p}, K_{m\times n}, E_{n\times n}, S_{n\times n}, R_{n\times n}$ through Steps (2) and (3).

5) Determining *N* and *M* as *N=I* and *M=I-RS*.

6) Obtaining the controller parameters via equation (23).

Fig. 5 shows the controller design steps for controlling virtual inertia in the islanded microgrid.

Results and Discussion

The Islanded microgrid parameters are shown in Table 1. Dynamic controller values for the islanded microgrid, according to the new proposed control method, are shown in the appendix section. Simulation has been considered in six scenarios in order to compare the performance of the proposed controller for virtual inertia control with consideration of virtual damping in the microgrid. In scenario (1), load disturbance has been imposed upon the microgrid. In scenario (2), load disturbance has been imposed, considering uncertainty in microgrid parameters (inertia). In scenarios (3), (4), (5), (6) and (7), various disturbances, including load and distributed generation resources (wind farm, solar farm) have been imposed upon the islanded microgrid.

$$\delta_3=\begin{bmatrix} A(t)R+RA^T(t)+M\hat{C}(t)B^T(t) & A(t)+RA^T(t)S+M\hat{C}^T(t)B^T(t)S+RC_2^T(t)\hat{B}^T(t)N^T+M\hat{A}^T(t)N^T & D(t) & RC_1^T(t)+M\hat{C}^T(t)D_{12}^T(t) \\ A^T(t)+SA(t)R+SB(t)\hat{C}M^T+N\hat{B}(t)C_2(t)+N\hat{A}M^T & A^T(t)S+SA(t)+N\hat{B}C_2(t)\hat{B}^TN^T & SD(t) & C_1^T(t) \\ D^T(t) & D^T(t)S & -\gamma^2 I & 0 \\ C_1(t)R+D_{12}(t)\hat{C}M^T & C_1(t) & 0 & -I \end{bmatrix}<0 \quad (22)$$

$$\hat{A}=N^{-1}(E-LC_2R-SAR-SBK)M^{-T},\ \hat{B}=N^{-1}L,\hat{C}=KM^{-T} \quad (23)$$

$$\delta_3=\begin{bmatrix} AR+RA^T+BK+K^TB^T & A+E^T & D & RC_1^T+K^TD_{12}^T \\ A^T+E & A^TS+SA+LC_2+C_2^TL^T & SD & C_1^T \\ D^T & D^TS & -\gamma^2I & 0 \\ C_1R+D_{12}K & C_1 & 0 & -I \end{bmatrix}+o_1+o_2+o_3+o_4+o_5+o_6+o_7+o_8+o_9+o_{10}+o_{11}+o_{12}+o_{13}<0$$

$$o_1=\begin{bmatrix} \Delta AR+R\Delta A^T & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix},o_2=\begin{bmatrix} \Delta BK+K^T\Delta B^T & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix},o_3=\begin{bmatrix} 0 & \Delta A & 0 & 0 \\ \Delta A^T & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix},o_4=\begin{bmatrix} 0 & R\Delta A^TS & 0 & 0 \\ S\Delta A^TR & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

$$,o_5=\begin{bmatrix} 0 & K^T\Delta B^TS & 0 & 0 \\ S\Delta BK & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix},o_6=\begin{bmatrix} 0 & R\Delta C_2^TL^T & 0 & 0 \\ L\Delta C_2R & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix},o_7=\begin{bmatrix} 0 & 0 & \Delta D & 0 \\ 0 & 0 & 0 & 0 \\ \Delta D^T & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix},o_8=\begin{bmatrix} 0 & 0 & 0 & R\Delta C_1^T \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \Delta C_1R & 0 & 0 & 0 \end{bmatrix}$$

$$,o_9=\begin{bmatrix} 0 & 0 & 0 & K^T\Delta D_{12}^T \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \Delta D_{12}K & 0 & 0 & 0 \end{bmatrix},o_{10}=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & \Delta A^TS+S\Delta A & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix},o_{11}=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & L\Delta C_2+\Delta C_2^TL^T & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix},o_{12}=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & S\Delta D & 0 \\ 0 & \Delta D^TS & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad (24)$$

$$,o_{13}=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \Delta C_1^T \\ 0 & 0 & 0 & 0 \\ 0 & 0 & \Delta C_1 & 0 \end{bmatrix},o=\begin{bmatrix} AR+RA^T+BK+K^TB^T & A+E^T & D & RC_1^T+K^TD_{12}^T \\ A^T+E & A^TS+SA+LC_2+C_2^TL^T & SD & C_1^T \\ D^T & D^TS & -\gamma^2I & 0 \\ C_1R+D_{12}K & C_1 & 0 & -I \end{bmatrix}$$

$$\sigma F\upsilon+\upsilon^TF^T\sigma^T\le\Gamma\sigma\sigma^T+\Gamma^{-1}\upsilon^T\upsilon,F^TF\le I \quad (25)$$

$$o_1=\sigma_1 F\upsilon_1+\upsilon_1^T F^T\sigma_1^T\le\Gamma_1\sigma_1\sigma_1^T+\Gamma_1{}^{-1}\upsilon_1^T\upsilon_1,\qquad o_2=\sigma_2 F\upsilon_2+\upsilon_2^T F^T\sigma_2^T\le\Gamma_2\sigma_2\sigma_2^T+\Gamma_2{}^{-1}\upsilon_2^T\upsilon_3$$

$$o_3=\sigma_3 F\upsilon_3+\upsilon_3^T F^T\sigma_3^T\le\Gamma_3\sigma_3\sigma_1^T+\Gamma_3{}^{-1}\upsilon_3^T\upsilon_3,\qquad o_4=\sigma_4 F\upsilon_4+\upsilon_4^T F^T\sigma_4^T\le\Phi_1\sigma_4\sigma_4^T+\Phi_1{}^{-1}\upsilon_4^T\upsilon_4$$

$$o_5=\sigma_5 F\upsilon_5+\upsilon_5^T F^T\sigma_5^T\le\Phi_2\sigma_5\sigma_5^T+\Phi_2{}^{-1}\upsilon_5^T\upsilon_5,\qquad o_6=\sigma_6 F\upsilon_6+\upsilon_6^T F^T\sigma_6^T\le\Phi_3\sigma_6\sigma_6^T+\Phi_3{}^{-1}\upsilon_6^T\upsilon_6$$

$$o_7=\sigma_7 F\upsilon_7+\upsilon_7^T F^T\sigma_7^T\le\Gamma_4\sigma_7\sigma_7^T+\Gamma_4{}^{-1}\upsilon_7^T\upsilon_7,\qquad o_8=\sigma_8 F\upsilon_8+\upsilon_8^T F^T\sigma_8^T\le\Gamma_5\sigma_8\sigma_8^T+\Gamma_5{}^{-1}\upsilon_8^T\upsilon_8$$

$$o_9=\sigma_9 F\upsilon_9+\upsilon_9^T F^T\sigma_9^T\le\Gamma_6\sigma_9\sigma_9^T+\Gamma_6{}^{-1}\upsilon_9^T\upsilon_9,\qquad o_{10}=\sigma_{10}F\upsilon_{10}+\upsilon_{10}^T F^T\sigma_{10}^T\le\Gamma_7\sigma_{10}\sigma_{10}^T+\Gamma_7{}^{-1}\upsilon_{10}^T\upsilon_{10}$$

$$o_{11}=\sigma_{11}F\upsilon_{11}+\upsilon_{11}^T F^T\sigma_{11}^T\le\Gamma_8\sigma_{11}\sigma_{11}^T+\Gamma_8{}^{-1}\upsilon_{11}^T\upsilon_{11},\quad o_{12}=\sigma_{12}F\upsilon_{12}+\upsilon_{12}^T F^T\sigma_{12}^T\le\Gamma_9\sigma_{12}\sigma_{12}^T+\Gamma_9{}^{-1}\upsilon_{12}^T\upsilon_{12}$$

$$o_{13}=\sigma_{13}F\upsilon_{13}+\upsilon_{13}^T F^T\sigma_{13}^T\le\Gamma_{10}\sigma_{13}\sigma_{13}^T+\Gamma_{10}{}^{-1}\upsilon_{13}^T\upsilon_{13}$$

$$\sigma_1=\begin{bmatrix}M_A\\0\\0\\0\end{bmatrix},\upsilon_1=\begin{bmatrix}N_AR&0&0&0\end{bmatrix},\sigma_2=\begin{bmatrix}M_B\\0\\0\\0\end{bmatrix},\upsilon_2=\begin{bmatrix}0&N_A&0&0\end{bmatrix}$$

$$\sigma_3=\begin{bmatrix}M_A\\0\\0\\0\end{bmatrix},\upsilon_3=\begin{bmatrix}0&N_A&0&0\end{bmatrix},\sigma_4=\begin{bmatrix}0\\SM_A\\0\\0\end{bmatrix},\upsilon_4=\begin{bmatrix}N_AR&0&0&0\end{bmatrix}$$

$$\sigma_5=\begin{bmatrix}0\\SM_B\\0\\0\end{bmatrix},\upsilon_5=\begin{bmatrix}N_BK&0&0&0\end{bmatrix},\sigma_6=\begin{bmatrix}0\\LM_{C_2}\\0\\0\end{bmatrix},\upsilon_6=\begin{bmatrix}N_{C_2}R&0&0&0\end{bmatrix}$$

$$\sigma_7=\begin{bmatrix}M_D\\0\\0\\0\end{bmatrix},\upsilon_7=\begin{bmatrix}0&0&N_D&0\end{bmatrix},\sigma_8=\begin{bmatrix}0\\0\\0\\M_{C_1}\end{bmatrix},\upsilon_8=\begin{bmatrix}N_{C_1}R&0&0&0\end{bmatrix}$$

$$\sigma_9=\begin{bmatrix}0\\0\\0\\M_{D_{12}}\end{bmatrix},\upsilon_9=\begin{bmatrix}N_{D_{12}}K&0&0&0\end{bmatrix},\sigma_{10}=\begin{bmatrix}0\\SM_A\\0\\0\end{bmatrix},\upsilon_{10}=\begin{bmatrix}0&N_A&0&0\end{bmatrix}$$

$$\sigma_{11}=\begin{bmatrix}0\\LM_{C_2}\\0\\0\end{bmatrix},\upsilon_{11}=\begin{bmatrix}0&N_{C_2}&0&0\end{bmatrix},\sigma_{12}=\begin{bmatrix}0\\SM_D\\0\\0\end{bmatrix},\upsilon_{12}=\begin{bmatrix}0&0&N_D&0\end{bmatrix}$$

$$\sigma_{13}=\begin{bmatrix}0\\0\\0\\M_{C_1}\end{bmatrix},\upsilon_{13}=\begin{bmatrix}0&N_{C_1}&0&0\end{bmatrix},\quad \bar{o}_1=\Gamma_1\sigma_1\sigma_1^T+\Gamma_1^{-1}\upsilon_1^T\upsilon_1,\quad \bar{o}_2=\Gamma_2\sigma_2\sigma_2^T+\Gamma_2^{-1}\upsilon_2^T\upsilon_2 \tag{26}$$

$$\bar{o}_3=\Gamma_3\sigma_3\sigma_3^T+\Gamma_3^{-1}\upsilon_3^T\upsilon_3,,\quad \bar{o}_4=\Phi_1\sigma_4\sigma_4^T+\Phi_1{}^{-1}\upsilon_4^T\upsilon_4,\quad \bar{o}_5=\Phi_2\sigma_5\sigma_5^T+\Phi_2{}^{-1}\upsilon_5^T\upsilon_5,\quad \bar{o}_6=\Phi_3\sigma_6\sigma_6^T+\Phi_3{}^{-1}\upsilon_6^T\upsilon_6$$

$$,\bar{o}_7=\Gamma_4\sigma_7\sigma_7^T+\Gamma_4^{-1}\upsilon_7^T\upsilon_7,\quad \bar{o}_8=\Gamma_5\sigma_8\sigma_8^T+\Gamma_5^{-1}\upsilon_8^T\upsilon_8,\quad \bar{o}_9=\Gamma_6\sigma_9\sigma_9^T+\Gamma_6^{-1}\upsilon_9^T\upsilon_9,\quad \bar{o}_{10}=\Gamma_7\sigma_{10}\sigma_{10}^T+\Gamma_7^{-1}\upsilon_{10}^T\upsilon_{10}$$

$$,\bar{o}_{11}=\Gamma_8\sigma_{11}\sigma_{11}^T+\Gamma_8^{-1}\upsilon_{11}^T\upsilon_{11},\quad \bar{o}_{12}=\Gamma_9\sigma_{12}\sigma_{12}^T+\Gamma_9^{-1}\upsilon_{12}^T\upsilon_{12},\quad \bar{o}_{13}=\Gamma_{10}\sigma_{13}\sigma_{13}^T+\Gamma_{10}^{-1}\upsilon_{13}^T\upsilon_{13}$$

$$\delta_3 \le o + \sum_{i=1}^{13} \bar{o}_i = \delta_4 < 0 \tag{27}$$

$$\delta_4 = o + \sum_{i=2}^{13} \bar{o}_i + \begin{bmatrix} \Gamma_1 M_A M_A^T & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} + \begin{bmatrix} RN_A^T \\ 0 \\ 0 \\ 0 \end{bmatrix} \Gamma_1^{-1} \begin{bmatrix} N_A R & 0 & 0 & 0 \end{bmatrix} < 0$$

$$\delta_4 = \begin{bmatrix} o + \sum_{i=2}^{13} \bar{o}_i & \begin{bmatrix} RN_A^T \\ 0 \\ 0 \\ 0 \end{bmatrix} \\ \begin{bmatrix} N_A R & 0 & 0 & 0 \end{bmatrix} & -\Gamma_1 \end{bmatrix} < 0 \tag{28}$$

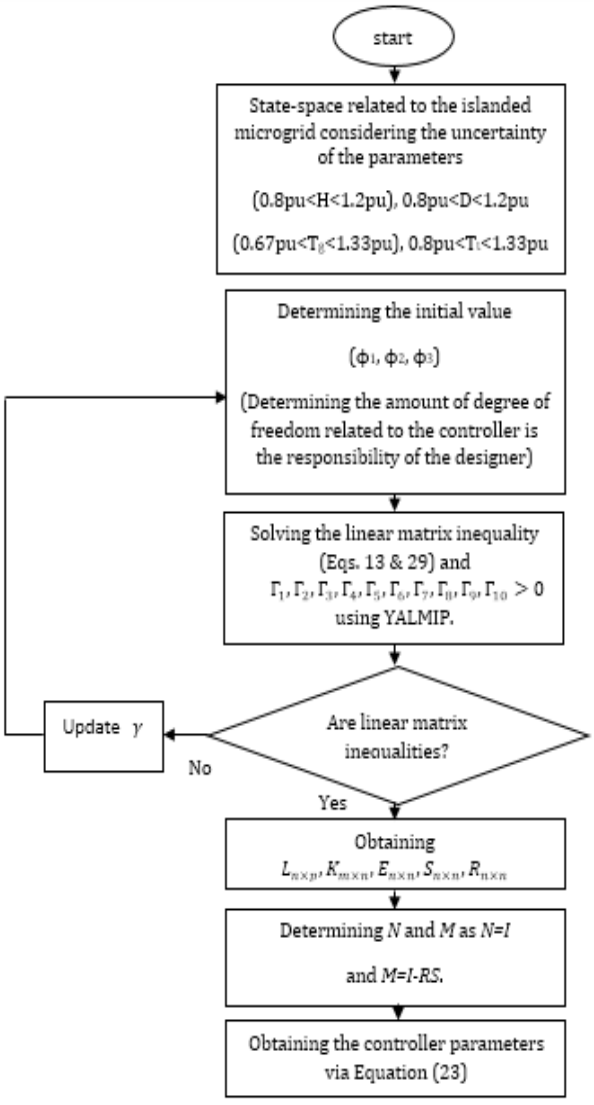

Fig. 5: : The controller design steps for controlling virtual inertia in the islanded microgrid.

Scenario (1): In this scenario, load disturbance of ΔP_{L1}=0.1pu at the time of t=1 has been imposed upon the islanded microgrid [25]. In Fig. 6, the microgrid frequency deviation using various controllers has been depicted. The frequency deviation using the proposed control method is 0.02 Hz. The frequency deviation using the pi-optimizer controller (with virtual inertia and virtual damping) method is 0.12 Hz. frequency deviation using the no controller (with virtual inertia and virtual damping) method is 0.24 Hz, and frequency deviation using the no controller (with virtual inertia) method is 0.26 Hz [25]. According to Fig. 6, the new proposed robust controller shows desirable performance against disturbances, compared to other methods (no controller (with virtual inertia and virtual damping), no controller (with virtual inertia), and pi-optimizer controller (with virtual inertia and virtual damping)). Using the proposed controller, the settling time of frequency deviation is 5.25 seconds. Using the pi-optimizer controller, the settling time of the frequency deviation is 7.16 seconds. Using the no controller (with virtual inertia and virtual damping) method, the settling time of frequency deviation is 8.13 seconds. Using the no controller (virtual inertia) method, the settling time of frequency deviation is 13.44 seconds. The proposed method performs better than other mentioned controllers in terms of damping speed related to microgrid frequency fluctuations.

Scenario (2): In this scenario, load disturbance of ΔP_{L1}=0.1pu at the time of t=1, with the uncertainty of islanded microgrid parameters (-20% inertia), has been imposed upon the islanded microgrid. In Fig. 7, the microgrid frequency deviation using various controllers has been depicted. The frequency deviation using the proposed control method is 0.02 Hz. The frequency deviation using the pi-optimizer controller (with virtual inertia and virtual damping) method is 0.135 Hz. The frequency deviation using the no controller (with virtual inertia and virtual damping) method is 0.27 Hz, and frequency deviation using the no controller (with virtual inertia) method is 0.28 Hz [25]. According to Fig. 7, the new proposed robust controller shows desirable performance against disturbances and uncertainty of islanded microgrid parameters, compared to other

methods. Using the proposed controller, the settling time of the frequency deviation is 5.33 seconds. Using the pi-optimizer controller, the settling time of frequency deviations is 7.42 seconds. Using the no controller (with virtual inertia and virtual damping) method, the settling time of frequency deviation is 9.34 seconds. Using the no controller (virtual inertia) method, the settling time of frequency deviation is 14.51 seconds. The proposed method performs better than other mentioned controllers in terms of damping speed of

frequency fluctuations against the uncertainty of microgrid parameters.

Scenario (3): In this scenario, according to Fig. 8, load and distributed generation resource disturbances, with regard to the uncertainty of islanded microgrid parameters (-20% inertia, -20% damping), have been imposed upon the islanded microgrid [25]. In Fig. 9, the microgrid frequency deviation using various controllers has been depicted. According to Fig. 9, the new proposed robust controller shows desirable performance against disturbances and uncertainty of islanded microgrid parameters, compared to other methods (of no controller (with virtual inertia and virtual damping), no controller (with virtual inertia), and pi-optimizer controller (with virtual inertia and virtual damping)). The maximum frequency deviation using the proposed control method is 0.03 Hz. The maximum frequency deviation using the pi-optimizer controller (with virtual inertia and virtual damping) method is 0.10 Hz. The maximum frequency deviation using the no controller (with virtual inertia and virtual damping) method is 0.22 Hz, and the maximum frequency deviation using the no controller (with virtual inertia) method is 0.26 Hz [25]. According to the results of this scenario, the proposed controller has been able to reduce the frequency error due to load and distributed generation resource disturbances and compared to other controllers; this frequency deviation has been reduced by 68%.

Scenario (4): In this scenario, according to Fig. 8, load and distributed generation resource disturbances, with regard to the uncertainty of islanded microgrid parameters (-20% inertia, -20% damping, +33% Time constant of governor), have been imposed upon the islanded microgrid. In Fig. 10, the microgrid frequency deviation using various controllers is shown. Frequency deviation using the proposed control method is 0.03 Hz. The frequency deviation using the pi-optimizer controller (with virtual inertia and virtual damping) method is 0.11 Hz.

The frequency deviation using the no controller (with virtual inertia and virtual damping) method is 0.31 Hz, and the frequency deviation using the no controller (with virtual inertia) method is 0.39 Hz. Looking at the results, it can be said that the proposed controller has had a good performance in weakening the disturbance caused by the load and distributed generation resources disturbances and has been able to reduce the frequency error by 72%.

Scenario (5): In this scenario, according to Fig. 8, load and distributed generation resource disturbances, with regard to the uncertainty of islanded microgrid parameters (-20% inertia, -20% damping, +33% Time constant of governor, -33% Time constant of Turbine), have been imposed upon the islanded microgrid. In Fig. 11, the microgrid frequency deviation using various controllers is shown. The maximum Frequency deviation using the proposed control method is 0.033 Hz. The maximum frequency deviation using the pi-optimizer controller (with virtual inertia and virtual damping) method is 0.14 Hz. The maximum frequency deviation using the no controller (with virtual inertia and virtual damping) method is 0.35 Hz, and the maximum frequency deviation using the no controller (with virtual inertia) method is 0.45 Hz. The results of this scenario show that the proposed controller is also robust to severe uncertainties, and the frequency error is reduced by 72% compared to the other mentioned control methods.

Scenario (6): In this scenario, according to Fig. 12, load and distributed generation resource disturbances, have been imposed upon the islanded microgrid [21]. In Fig. 13, the microgrid frequency deviation using various controllers is shown. The maximum Frequency deviation using the proposed control method is 0.045 Hz. The maximum frequency deviation using the Self-adaptive virtual inertia control using fuzzy logic is 0.19 Hz [21], and the maximum frequency deviation using the MPC controller (with virtual inertia and virtual damping) is 0.28 Hz [23].

According to the results of this scenario, the MPC controller and Self-adaptive virtual inertia control do not perform well against disturbance, and the effect of disturbance on the microgrid frequency is high. While the proposed controller has been able to greatly weaken the disturbance effect, the frequency error has been reduced by 75% compared to other controllers.

Scenario (7): In this scenario, according to Fig. 12 load and distributed generation resource disturbances, with regard to the uncertainty of islanded microgrid parameters (-20% inertia), have been imposed upon the islanded microgrid. In Fig. 14, the microgrid frequency deviation using various controllers is shown. The maximum Frequency deviation using the proposed control method is 0.054 Hz.

The maximum frequency deviation using the Self-adaptive virtual inertia control using fuzzy logic is 0.21 Hz [21], and maximum frequency deviation using the MPC controller [23] (with virtual inertia and virtual damping)

is 0.30 Hz. According to the results of this scenario, the proposed controller has a better performance than the new controllers used in the field of virtual inertia control.

Conclusion

In microgrids, power electronic converters are utilized for power exchange and possess very low inertia compared to power systems. Therefore, a virtual synchronous generator is used for implementing large synchronous generator behavior in a power system, which provides desirable inertia for the system. Virtual inertia control is a component of the virtual synchronous generator which helps improve microgrid frequency stability. In microgrids with vast energy resources, in addition to virtual inertia, considering virtual damping can reduce system instability. In this paper, designing a new robust control method for controlling virtual inertia in microgrids, with regard to virtual damping, has been attempted. The proposed control method does not require measuring of all the modes and uses only output feedback. According to the simulation results, the proposed controller has a better performance than other controllers in improving the frequency stability of the islanded microgrid.

$$
\begin{bmatrix}
\delta_{11_{n\times n}} & A+E^T & D & RC_1^T+KD_{12}^T & RN_A^T & K^TN_B^T & 0_{n\times1} & 0_{n\times1} & RN_{C_1}^T & KN_{D_{12}}^T & 0_{n\times1} & 0_{n\times1} & 0_{n\times1} & 0_{n\times1} & 0_{n\times1} & RN_A^T & 0_{n\times1} & K^TN_B^T & 0_{n\times1} & RN_{C_2}^T \\
A^T+E & \delta_{22_{n\times n}} & SD & C_1^T & 0_{n\times1} & 0_{n\times1} & N_A^T & 0_{n\times1} & 0_{n\times1} & 0_{n\times1} & SM_A & LM_{C_2} & SN_D & N_{C_1}^T & SM_A & 0_{n\times1} & SM_B & 0_{n\times1} & LM_{C_2} & 0_{n\times1} \\
D & D^TS & \delta_{33_{d\times d}} & 0_{d\times q} & 0_{d\times1} & 0_{d\times1} & N_D^T & 0_{d\times1} & 0_{d\times1} & 0_{d\times1} & 0_{d\times1} & 0_{d\times1} & 0_{d\times1} & 0_{d\times1} & 0_{d\times1} & 0_{d\times1} & 0_{d\times1} & 0_{d\times1} & 0_{d\times1} & 0_{d\times1} \\
C_1R+D_{12}K & C_1 & 0_{q\times d} & \delta_{44_{q\times q}} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} & 0_{q\times1} \\
N_AR & 0_{1\times n} & 0_{1\times d} & 0_{1\times q} & -\Gamma_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
N_BK & 0_{1\times n} & 0_{1\times d} & 0_{1\times q} & 0 & -\Gamma_2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0_{1\times n} & N_A & 0_{1\times d} & 0_{1\times q} & 0 & 0 & -\Gamma_3 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0_{1\times n} & 0_{1\times n} & N_D & 0_{1\times q} & 0 & 0 & 0 & -\Gamma_4 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
N_{C_1}R & 0_{1\times n} & 0_{1\times d} & 0_{1\times q} & 0 & 0 & 0 & 0 & -\Gamma_5 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
N_{D_{12}}K & 0_{1\times n} & 0_{1\times d} & 0_{1\times q} & 0 & 0 & 0 & 0 & 0 & -\Gamma_6 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0_{1\times n} & M_A^TS & 0_{1\times d} & 0_{1\times q} & 0 & 0 & 0 & 0 & 0 & 0 & -\Gamma_7 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0_{1\times n} & M_{C_2}^TL^T & 0_{1\times d} & 0_{1\times q} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\Gamma_8 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0_{1\times n} & M_D^TS & 0_{1\times d} & 0_{1\times q} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\Gamma_9 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0_{1\times n} & N_{C_1} & 0_{1\times d} & 0_{1\times q} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\Gamma_{10} & 0 & 0 & 0 & 0 & 0 & 0 \\
0_{1\times n} & M_A^TS & 0_{1\times d} & 0_{1\times q} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\Phi_1^{-1} & 0 & 0 & 0 & 0 & 0 \\
N_AR & 0_{1\times n} & 0_{1\times d} & 0_{1\times q} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\Phi_1 & 0 & 0 & 0 & 0 \\
0_{1\times n} & M_B^TS & 0_{1\times d} & 0_{1\times q} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\Phi_2^{-1} & 0 & 0 & 0 \\
N_BK & 0_{1\times n} & 0_{1\times d} & 0_{1\times q} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\Phi_2 & 0 & 0 \\
0_{1\times n} & M_{C_2}^TL^T & 0_{1\times d} & 0_{1\times q} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\Phi_3^{-1} & 0 \\
N_{C_2}R & 0_{1\times n} & 0_{1\times d} & 0_{1\times q} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\Phi_3
\end{bmatrix} < 0 \tag{29}
$$

$$
\begin{cases}
\delta_{11_{n\times n}} = AR+RA^T+BK+K^TB^T+(\Gamma_1+\Gamma_3)M_AM_A^T+\Gamma_2M_BM_B^T+\Gamma_4M_DM_D^T \\
\delta_{22_{n\times n}} = A^TS+SA+LC_2+C_2^TL^T+\Gamma_7N_A^TN_A+\Gamma_8N_{C_2}^TN_{C_2},\ \delta_{33_{d\times d}} = -\gamma^2I+\Gamma_9N_D^TN_D \\
\delta_{44_{q\times q}} = -I+(\Gamma_5+\Gamma_{10})M_{C_1}M_{C_1}^T+\Gamma_6M_{D_{12}}M_{D_{12}}^T
\end{cases}
$$

Table 1: The Islanded microgrid parameters [24], [25]

Parameter	value	Parameter	value
Virtual damping, D_{VI}(s)	1.2	Governor Time constant, T_g(s)	0.1
Time constant of ESS, T_{ESS}(s)	10	Turbine Time constant, T_t(s)	0.4
Time constant of wind turbine, T_{WT} (s)	1.4	Droop factor, R (Hz/pu. MW)	2.4
Time constant of solar system, T_{PV}(s)	1.9	Virtual inertia, J_{VI}(s)	1.6
System (microgrid) inertia, H (p.u.MW s)	0.082	Secondary frequency controller, K(s)	0.2
System (microgrid) damping, D (p.u.MW/Hz)	0.016	Frequency bais,	0.99

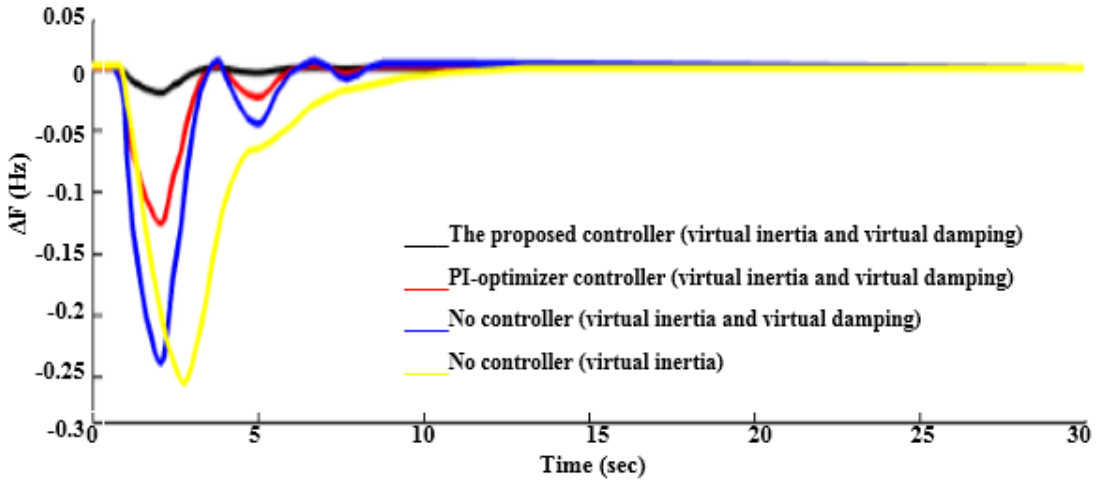

Fig. 6: The frequency deviation using various controllers, Scenario (1).

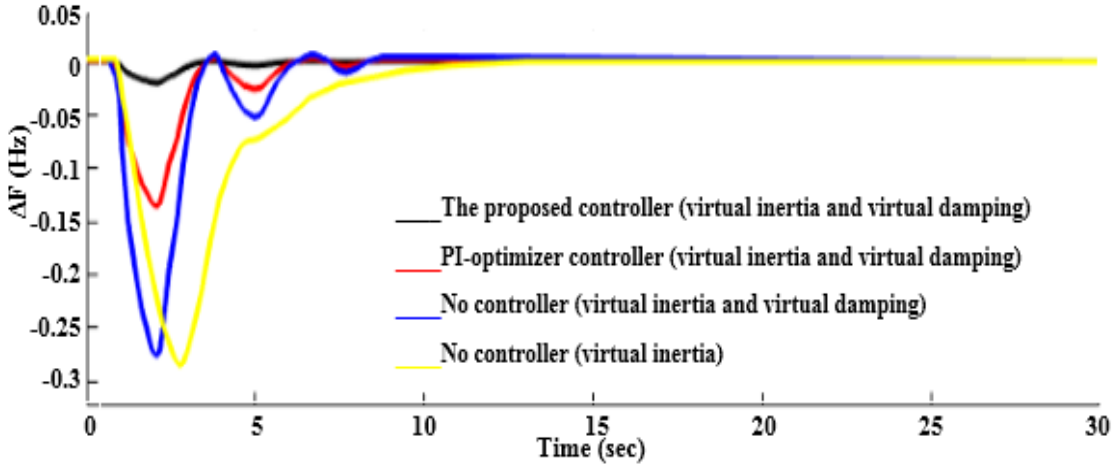

Fig. 7: The frequency deviation using various controllers, Scenario (2).

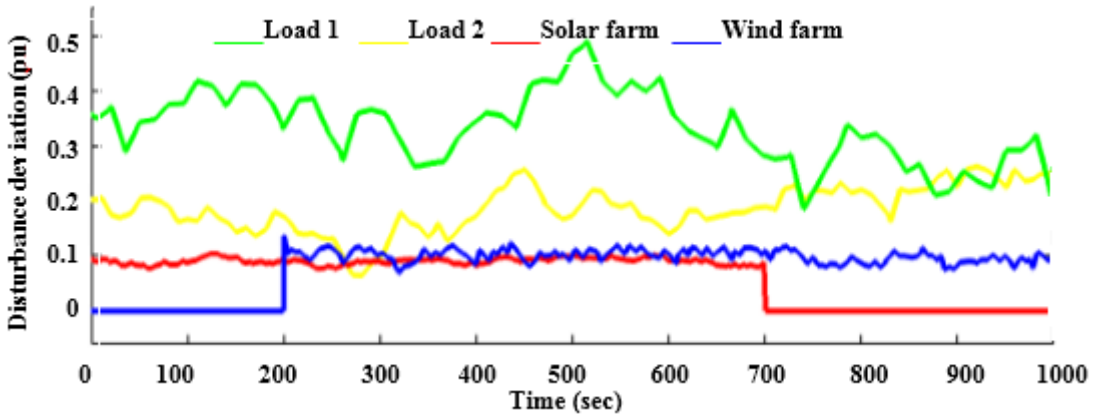

Fig. 8: Disturbances on the islanded microgrid [22]-[25].

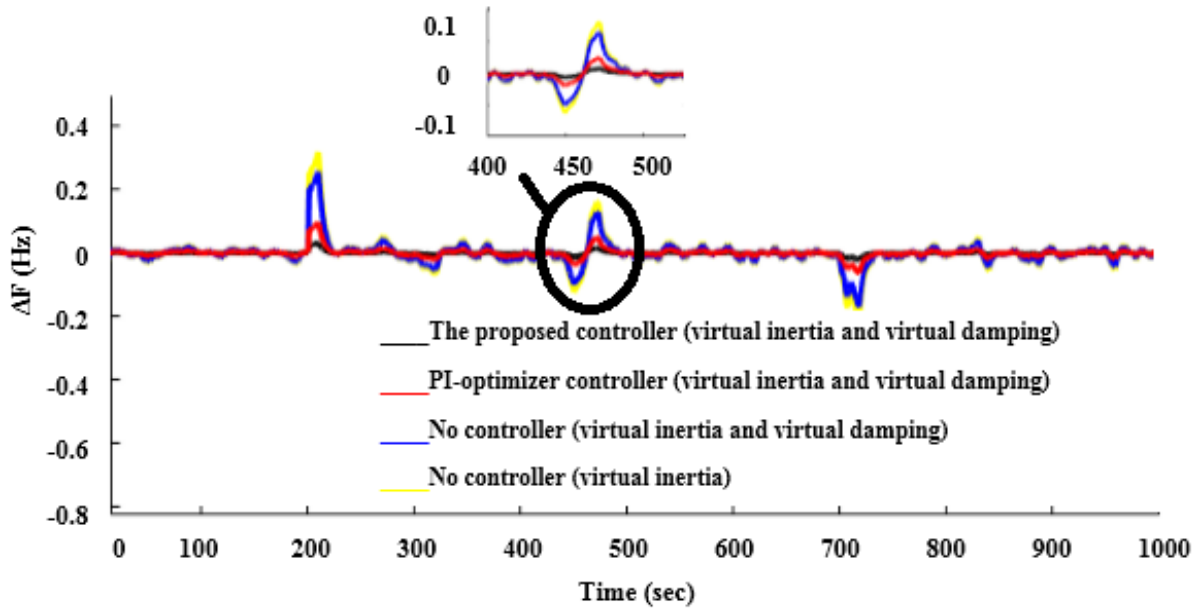

Fig. 9: : The frequency deviation using various controllers, Scenario (3).

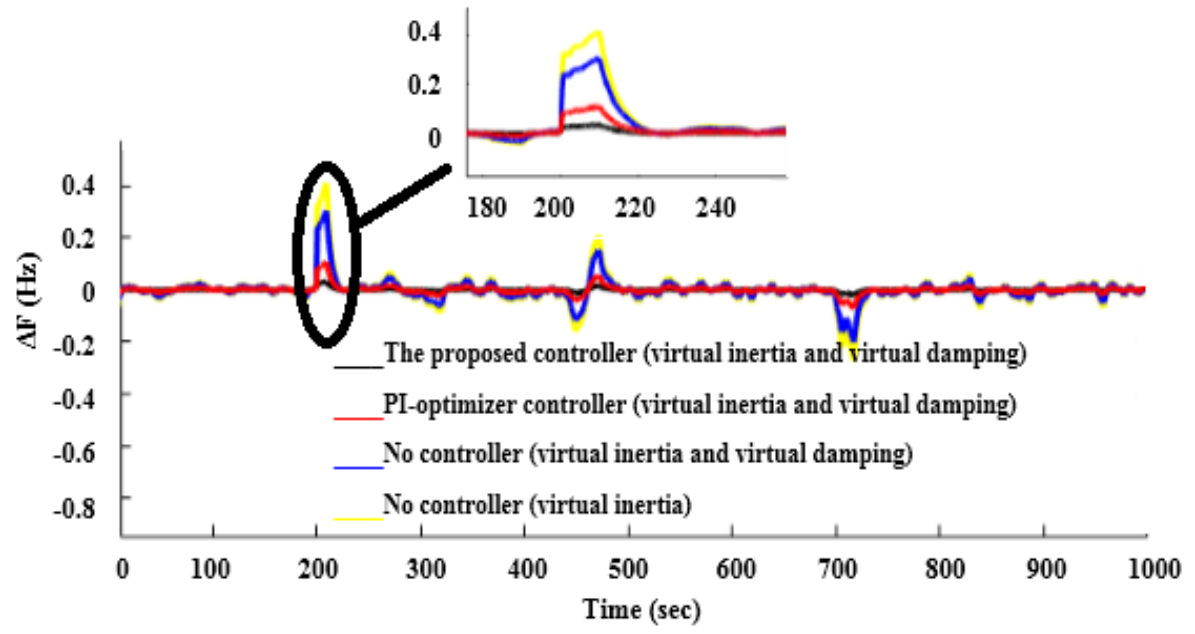

Fig. 10: : The frequency deviation using various controllers, Scenario (4).

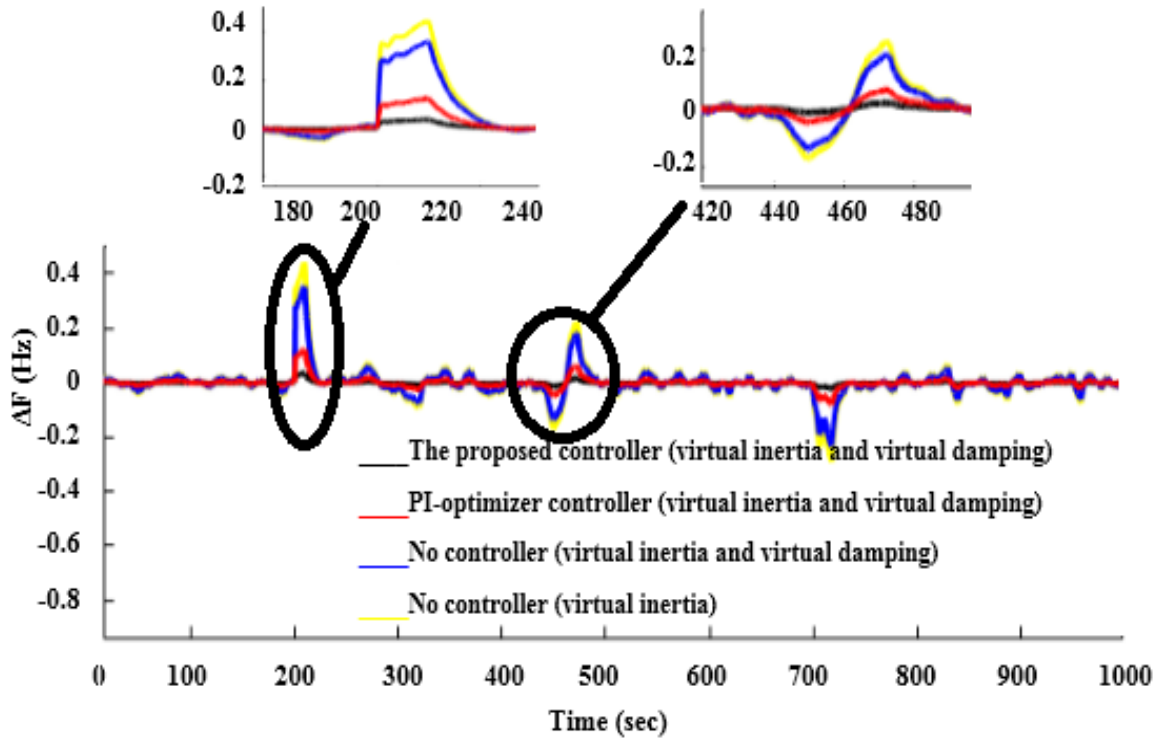

Fig. 11: The frequency deviation using various controllers, Scenario (5).

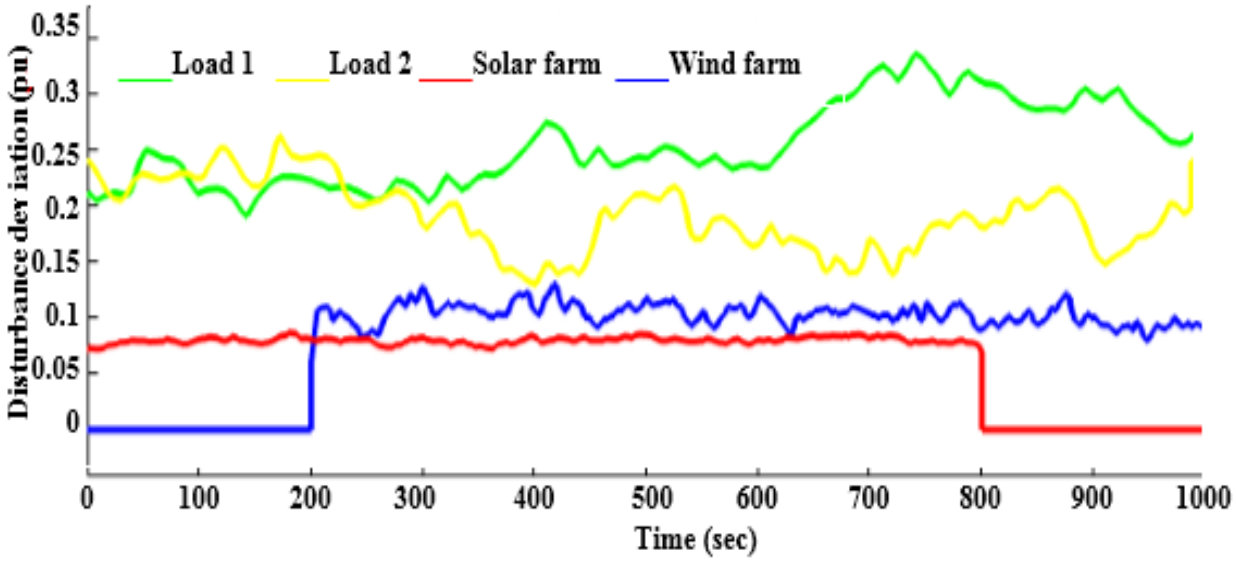

Fig. 12: Disturbances on the islanded microgrid, Scenario (6) [21].

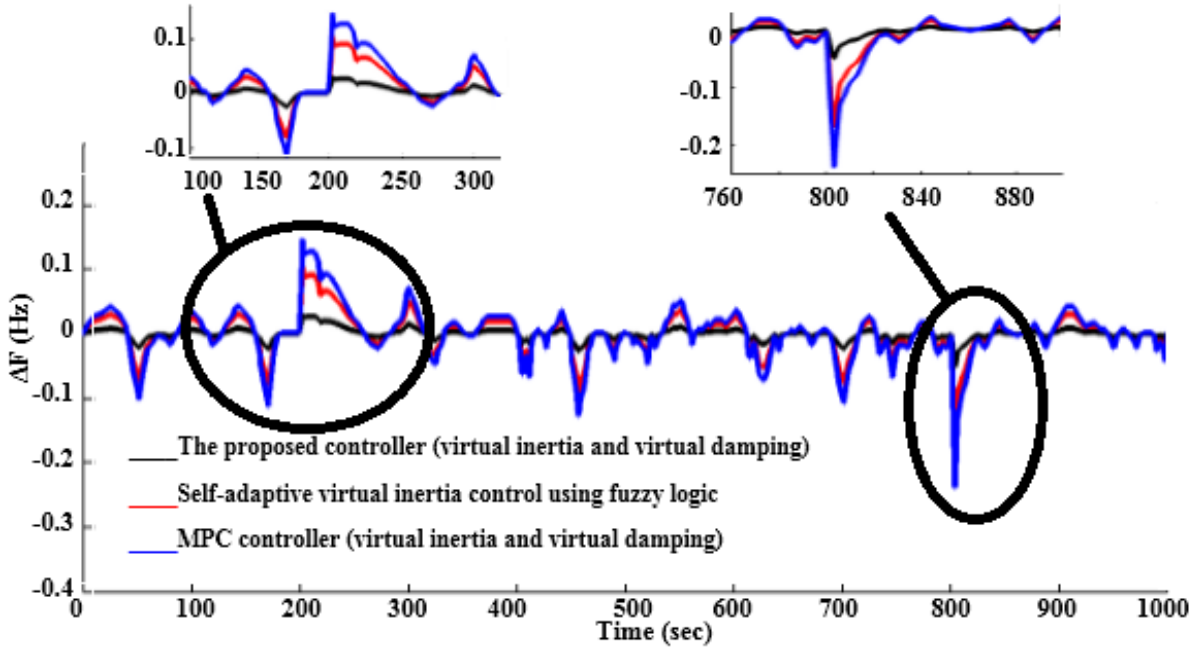

Fig. 13: The frequency deviation using various controllers, Scenario (6).

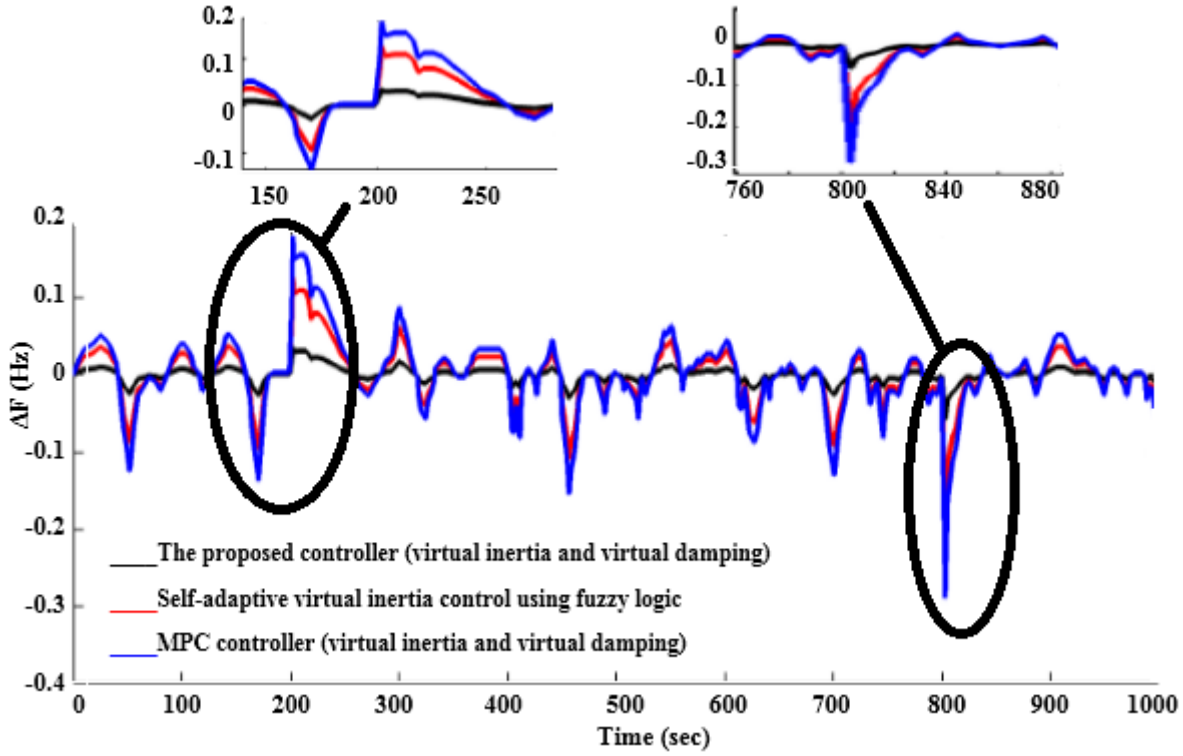

Fig. 14: : The frequency deviation using various controllers, Scenario (7).

Appendix

The proposed controller parameters shown in the appendix can greatly weaken the load disturbances and distributed generation resources disturbances in the islanded microgrid. These dynamic control parameters can also be very robust to the uncertainties of microgrid parameters. The proposed controller parameters are set to be able to track the system reference (the islanded microgrid frequency).

$$\hat{A}=\begin{bmatrix} -176.07 & 4.4335 & 1.3472 & 0.7497 & 0.48059 & 178.08 & 129.61 \\ -130.79 & -5.9675 & 9.9792 & -0.75207 & -0.47191 & -178.53 & -129.96 \\ 21.59 & -0.052115 & -10.55 & 0.087908 & 0.054885 & 20.866 & 15.187 \\ 4809.6 & 176.53 & 73.776 & 30.808 & 19.36 & 7313.8 & 5324.1 \\ -18854 & -68397 & -29366 & -12092 & -7598.9 & -28706 & -20897 \\ -200.52 & -7.2778 & -3.1252 & -1.2864 & -0.80849 & -306.16 & -222.35 \\ -206.71 & -7.5025 & -3.2217 & -1.3262 & -0.83348 & -314.89 & -229.75 \end{bmatrix}, \hat{B}=\begin{bmatrix} -25167 \\ -49106 \\ 90292 \\ 25188 \\ -4813.4 \\ -54.716 \\ -55.91 \end{bmatrix}$$

$$\hat{C}=\begin{bmatrix} 21.077 & 0.76462 & 0.32829 & 0.13518 & 0.084949 & 32.091 & 23.361 \end{bmatrix}$$

Author Contributions

F. Amiri and M. H. Moradi designed the island microgrid model and controller. F. Amiri collected the data and carried out the data analysis. F. Amiri interpreted the results and wrote the manuscript.

Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

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Research paper

Ultra-Low-Energy DSP Processor Design for Many-Core Parallel Applications

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Abstract

Background and Objectives: Digital signal processors are widely used in energy constrained applications in which battery lifetime is a critical concern. Accordingly, designing ultra-low-energy processors is a major concern. In this work and in the first step, we propose a sub-threshold DSP processor.
Methods: As our baseline architecture, we use a modified version of an existing ultra-low-power general purpose processor. Afterwards, we make some modifications to add new instructions to the processor instruction set for better adapting to signal processing applications. In the second step, employing sub-threshold cores in many-core architectures, we use the proposed processor as simple basic cores in a many-core architecture.
Results: In comparison with the baseline architecture, these modifications reduce the program memory size about 42% in average. In addition, data memory accesses are reduced about 60% in average, and more than 90% speed-up is achieved. According to the improvements in total execution time (93%) and power consumption (27%), the total consumed energy is reduced about 95% in average with at most 2.6% area overhead and without increasing the process variation effects on processor specifications.
Conclusion: The results show that for parallel applications, such as FFT in LTE standard, exploiting sub-threshold processors in a many-core architecture not only can satisfy the required performance, but also reduce the power consumption about 50% or even more.

Introduction

Energy constrained applications such as cell phones, wireless networks, and RFID tags are widely used in recent years. Power/energy consumption, performance, and reliability are the main concerns in designing such systems [1], [2], [3]. Moreover, the use of deep sub-micron technologies has made designs even more challenging due to increased variations in process parameters such as gate oxide thickness, channel length, and threshold voltage [2], [4].

Designing processor architecture in the sub-threshold region, where the supply voltage is less than the threshold voltage, can efficiently reduce energy and power consumption [6], [5].

Sub-threshold design provides energy harvesting capability for long-term applications such as health-care signal processing and monitoring wireless networks [2].

However, sub-threshold computing degrades performance and escalates variation problems [6]. Therefore, it is necessary to design custom architectures and utilize alternate techniques to accompany sub-threshold design. Application specific processors are potential candidates to meet the mentioned requirements.

To customize an architecture for a specific application, parameters such as computation width, pipeline depth, ISA definition, memory organization design, and addressing modes need to be considered [7]. Among these parameters, ISA definition is more effective and will affect the others. The complexity of custom instructions can change the execution timing and memory access rate of an application. Hence, custom instructions are useful in improving processor performance and reducing power/energy consumption [7]-[9].

Most of the low-power processors introduced in the literature have been designed to work in the super-threshold or near-threshold regions [10]-[15]. Moreover, processors introduced for the sub-threshold region [8],[16]-[18] are not optimized for computationally-intensive signal processing applications. The growing demand for DSP processors in energy constrained applications motivates our work, where we have simplified an existing ultra-low power general purpose processor [18] according to Pollack's rule [19]. We have added an extra unit corresponding to a new instruction added to the processor's ISA for accelerating signal processing applications. In this paper, we investigate the effects of the added custom instruction on power and energy consumption using specific signal processing applications. The results show that although adding the extra unit increases processor area, which is equivalent to more static energy dissipated in the sub-threshold region, the added custom instruction enables a smaller program memory footprint which in turn significantly reduces power and energy consumption. The proposed processor, to the best of our knowledge, is the first sub-threshold DSP processor; nevertheless, we do not claim that it has the best architecture.

Another usage of ultra-low-energy processors can be found in many-core architectures. These systems may exploit hundreds or thousands of small cores in parallel [20]. According to Pollack's rule [19], the performance of a core is proportional to the square root of the core's complexity (area). Although simplifying the core structure decreases its performance, it can increase the power efficiency. With many ultra-low-power cores one can make, through parallelism, a many-core architecture and then achieve a desirable throughput. According to the Amdahl's law, the serial part of a code will limit the speed-up. Thus parallel applications rationalizes the usage of many-core architectures. An integral part of high-speed wireless networks are Orthogonal Frequency-Division Multiplexing (OFDM) systems, in which signal processing applications such as Fast Fourier Transform (FFT) and Finite Impulse Response (FIR) filtering are exploited as the main operations [21], [22].

In this work, we proposed a novel processor architecture to achieve required performance with higher energy efficiency for target energy-constrained applications such as IoT. The proposed architecture is a general purpose processor with customized instructions for Digital Signal Processing (DSP) domain to improve performance and energy efficiency. Using the proposed DSP processor, one can aggregate many simplified very-low-power cores in parallel to construct very high-speed systems such as OFDM, filter bank, and etc.

The remainder of the paper is organized as follows: Section II reviews related work from the literature and discusses previously designed processors. In Section III the proposed processor architecture is presented along with a detailed description of the added extra unit and the related custom instructions. Section IV introduces our experimental setup and analyzes the obtained results, using specific signal processing applications. The usage of the proposed processor in many-core architectures and its experimental results are described in Section V. Finally, the paper is concluded in Section VI.

Related Works

In this section, we review the various ultra-low power processors introduced in the literature [8], [10]-[18]. For each processor, its main specifications and the techniques exploited by designers to reduce power and energy consumption are discussed.

In [10], a DSP processor known as uAMPS (micro Adaptive Multi-domain Power aware Sensors) has been designed, based on a load-store 16-bit RISC architecture. The processor is designed to work in the near-threshold region and contains an instruction cache and extra units including Multiply-ACcumulate (MAC) unit and custom hardware accelerator cores for FIR filters and FFT operations. Moreover, power gating is used to reduce power and energy consumption. The results show that uAMPS works at 4 MHz with a 0.45V power supply and consumes 10 pJ/Instruction in 90-nm technology.

Kelly *et al.*[23] have proposed a Sensor Network Asynchronous Processor (SNAP). To achieve a low power design, the SNAP designers employed asynchronous circuits by which dynamic power is reduced due to lower switching activities. SNAP/LE, the low energy version of SNAP that is proposed in [11], is based on an event-driven 16-bit RISC processor. Their single-issue processor core executes instructions in order and uses two separate on-chip memory banks for instructions and data. Their results show that in 180-nm technology, SNAP/LE works with 28 MIPS speed and consumes 24pJ energy per instruction at 0.6V. While SNAP/LE has a parallel datapath, another extension of SNAP called BitSNAP [12], has a bit-serial datapath leading to lower area and lower leakage power. In addition, the designers used compression techniques on data to improve the processor's performance. According to their report,

BitSNAP consumes 17 pJ/Instruction in 180-nm technology at 0.6V and provides 6 MIPS execution speed.

Another ultra-low power processor, called Smart Dust [13], has been devised based on a load-store RISC architecture, Harvard architecture for memories, and single cycle per instruction but with no pipelining in the datapath. Furthermore, techniques such as component-level clock gating and guarded ALU inputs were exploited to reduce power. Smart Dust was designed in 250-nm technology to work with a 1.0V power supply at 500 kHz and consumes 12 pJ/Instruction.

Hempstead et al. [14], [15] have used event-driven processing and hardware accelerators to improve power consumption and performance. The accelerators are designed for specific tasks which are common in many wireless sensor network applications. There is an event processing unit investigating events, and based on the event's type, determines which accelerator must be activated. Therefore, the tasks are offloaded to the accelerators and the microcontroller can be power gated. This technique reduces dynamic and leakage power dramatically. Thus Hempstead's processor consumes only 0.44 pJ per equivalent instruction at 12.5 MHz working frequency using a 0.55V power supply in 130-nm technology.

In [16], Nazhandali *et al*. proposed an energy-efficient sub-threshold processor, called Subliminal. The architecture is an accumulator-based CISC architecture with single operand instructions. Nazhandali et al. investigated 21 different architectures by changing the pipeline depth, datapath width, memory organization (von-Neumann vs. Harvard), and use of an explicit register file. The best performing architecture with lower energy consumption and acceptable performance was found using the pareto-optimal curves. The investigated processor specifications are summarized in Table 1. Subliminal is designed in 130-nm technology, works at 182 kHz, and consumes 1.38 pJ/Instruction at 235mV. In [17] and [8] Zhai *et al*. also analyzed process variation in sub-threshold circuits and showed that dynamic frequency scaling is more important than dynamic voltage scaling. In addition, Zhai *et al*. have designed a robust SRAM memory that made the Subliminal processor work correctly from 0.2V to 1.2V. The minimum energy consumption of the processor is 2.6 pJ/Instruction at 0.36V while working at 833 kHz.

The second generation of Subliminal is described in [18]. Subliminal2 is a load-store RISC architecture with two-operand 12-bit instructions. In Subliminal [16], the authors have shown that a smaller code size (with more complex control logic) is more energy-efficient than using a simpler control logic (with larger code size) and therefore, have selected CISC architecture with variable instruction lengths. However, in Subliminal2, Nazhandali *et al*. [18] proposed a compact 12-bit instruction set architecture with complicated addressing modes satisfying both requirements: simple control logic and also a dense code. Table 1 shows the Subliminal2 specifications consuming the lowest energy per instruction (0.6pJ/Instruction) among the sub-threshold processors and works at 142 kHz and 0.2V in 130-nm technology. The low energy processor architectures of sub- and near-threshold processors are summarized in Table 1. Also there are other harware accelerators working for energy-constrained applications such as [24]-[27] which are customized to the application domain to achieve higher computation speed with lower energy consumption. These works are not listed in our candidate baseline architecture because it is not fair to compare a general purpose processor with custom hardware accelerators.

Table 1: Specifications of some ultra-low-power processors

Processor Specifications	Subliminal	Subliminal2	uAMPS
ISA	Accumulator CISC architecture with single operand instruction	load-store RISC architecture with 2-operand instruction	load-store RISC architecture with 3-operand instruction
Data Width (bits)	8	8	16
Instruction Length	32/16/8	12	16
CPI	1	1	1
Pipeline Stages	3	3	3
Registers	4 GPR(32 bits) + 4 pointer register (16bits)	8 GPR(8 bits)	8 GPR + 8 special purpose registers
Memory Architecture	Von-neumann	Harvard	Von-neumann
Program Memory	512*4 bits	128*12 bits	60KB
Data Memory		128*8 bits	
Out-of-Order Execution	no	yes	no
Branch Speculation	no	yes	no
Multiplier	no	no	Yes
MAC	no	no	yes

Processor Architecture

In this work, we use a modified version of the Subliminal2 architecture as the basis of our DSP

processor architecture. The main features of Subliminal2 processor are summarized in Table I and our simplified implementation of the Subliminal2 (hereafter called SSL2) datapath is shown in Fig. 1. Here, we give a brief description of the Subliminal2 ISA as is used in our work and shown in Fig. 2.

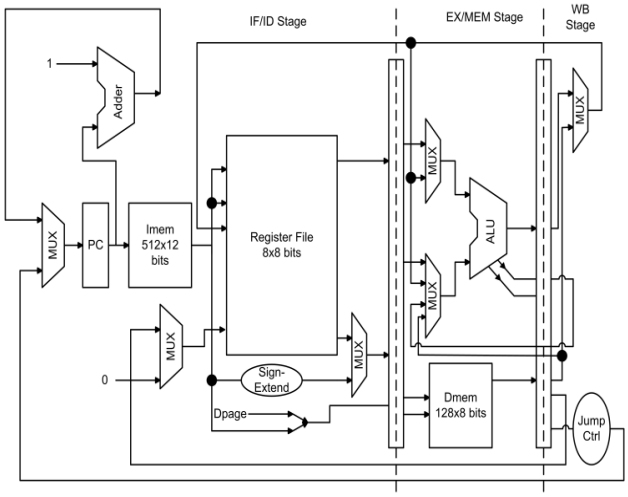

Fig. 1: SSL2 datapath, our simplified implementation of Subliminal2.

As the figure shows, in ALU instructions a P/U bit specifies a preserve/update mode. In the preserve mode the result of the ALU operation is saved in R0, while in the update mode operand A is updated by the ALU result. Using this, Subliminal2 benefits from the advantages of two-operand instructions, namely, smaller instruction length, and three-operand instructions in which source operand will not be overwritten. Note that operand B (OPB) includes five cases:

- MEM: The operand is one of the memory entries which can be accessed through direct memory access.
- REG: It denotes one of the 8 registers in the register file.
- PTR: In SSL2, PTR is used to denote one of the registers (R0 to R3) and it can access memory through indirect access.
- IMM: This is a two-bit immediate value.
- C: Shows a carry operand.

This feature shows that micro-operations are included in the ISA, which leads to smaller code size. For example, to add a register to a memory operand, instead of two instructions: LOAD followed by ADD, only one instruction is used.

The instruction and data memory size in Subliminal2 are 128x12 bits and 128x8 bits, respectively. In SSL2 we changed the instruction memory size to 512x12 bits, adapted to the size of most DSP codes running on. Instruction and data memories are divided into 32 and 8 pages, respectively. Each page has 16 entries. To access data memory, we need 3 bits to indicate the page, and 4 bits to access one of the 16 entries in that page. The PAGE instruction represents the page number, and then with the mode MEM of OPB, as shown in Fig. 2, we can access data memory directly.

In Subliminal2, the JDST part in JUMP instructions indicates the lowest 6 bits of jump target address. In SSL2 we modified the JUMP instruction as follows: For all jump conditions, except CALL, the jump target address will be added to the PC address, thereby we can access -32 to 31 instructions away from the current instruction using 6 bits; however for CALL condition, JDST indicates the lowest 6 bits of jump target address and the other three bits are determined by the PAGE instruction. The details of the instructions are presented in [18]. In Subliminal2, indirect memory access takes two clock cycles. If the load instruction is followed by a dependent ALU operation, then the implemented out-of-order execution feature will monitor the next instruction and if it is independent of ALU result, it will be executed before the ALU operation. We designed the instruction and data memory in the form of flip-flops as in [24]. Therefore, memory access takes only one cycle and there is no need to implement the out-of-order execution feature. Also in SSL2, unlike Subliminal2, the branch speculation scheme has not been implemented for sake of more simplicity. The instruction next to jump is always executed; therefore the compiler has been optimized to support this feature.

The main focus of our work is on designing an ultra-low power DSP processor. FFT operations and FIR filtering are frequently used in wireless networking and signal processing applications. Conventional FFT algorithm requires nlog n multiplications which makes it an important feature of any DSP processor. In SSL2, there is no multiply unit and no multiply instruction, and we need to carry out multiply operations using add instructions.

Here we propose the next version of SSL2 called SSL2Mult. In SSL2Mult we have added a multiply unit to the SSL2 datapath and a MULT instruction to its ISA. Figures 5 and 3 show the SSL2Mult datapath and MULT instruction, respectively. The MULT instruction has two modes for 8-bit unsigned and signed multiplications whose result will be saved in a 16-bit register. In the first cycle, OPA will be overwritten by the lowest 8 bits of the result and in the next cycle, the highest 8 bits of the result are saved in OPB. Moreover, as shown in Fig. 7, FIR filters use multiply-accumulate (MAC) operations. Thus, as our next step we have added a MAC unit and a MAC instruction to SSL2. We call this processor SSL2MAC. The SSL2MAC datapath and MAC instruction are shown in Figs. 6 and 4, respectively.

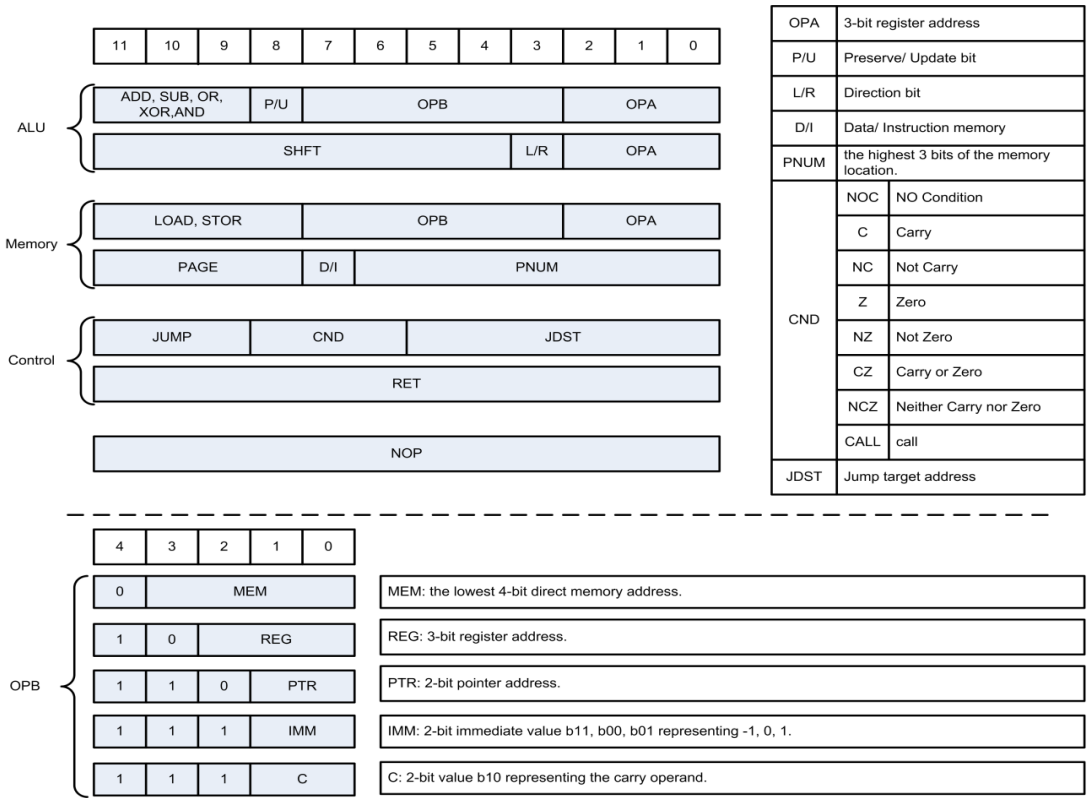

Fig. 2: SSL2 ISA encoding.

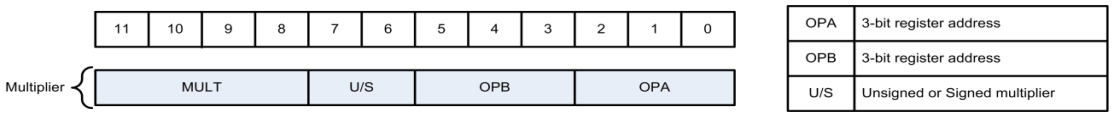

Fig. 3: The added MULT instruction toSSL2 ISA.

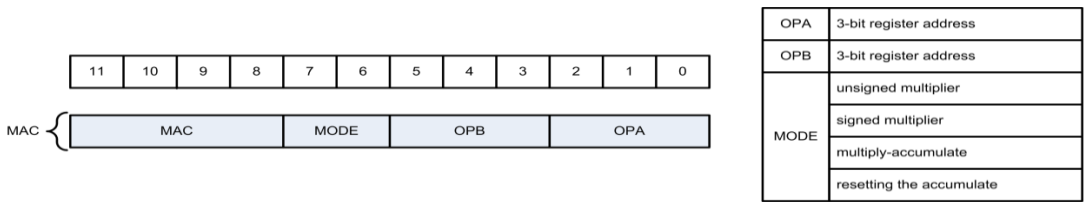

Fig. 4: The added MAC instruction toSSL2 ISA.

Table 2: Specifications of the proposed processors in comparison to subliminal2

Processor Specifications	Subliminal2	SSL2 (our implementation of subliminal2)	SSL2Mult	SSL2MAC
ISA	load-store RISC architecture with 2-operand instruction	load-store RISC architecture with 2-operand instruction	load-store RISC architecture with 2-operand instruction	load-store RISC architecture with 2-operand instruction
Data Width (bits)	8	8	8	8
Instruction Length	12	12	12	12
CPI	1	1	1	1
Pipeline Stages	3	3	3	3
Registers	8 GPR(8 bits)	8 GPR(8 bits)	8 GPR(8 bits)	8 GPR(8 bits)
Memory Architecture	Harvard	Harvard	Harvard	Harvard
Program Memory	128*12 bits	128*12 bits	128*12 bits	128*12 bits
Data Memory	128*8 bits	128*8 bits	128*8 bits	128*8 bits
Out-of-Order Execution	yes	Yes	yes	yes
Branch Speculation	yes	Yes	yes	yes
Multiplier	no	No	no	no
MAC	no	No	no	no

In MAC unit, the multiplier multiplies two 8-bit numbers and the result is added to a 24-bit accumulator. The MAC instruction has four modes: unsigned and signed multiplication, MAC operation, and accumulator reset. Table 2 summarizes the architectures of the proposed processors.

The multiply unit in SSL2Mult and the MAC unit in SSL2MAC increase the processor area, but on the other hand lead to smaller code size.

Furthermore, these units are power gated in applications that do not require them. We need to investigate the advantages and disadvantages of adding these extra units in sub-threshold circuits.

In the next section, we analyze the performance and energy results of the three discussed processors on two benchmarks: FFT and FIR.

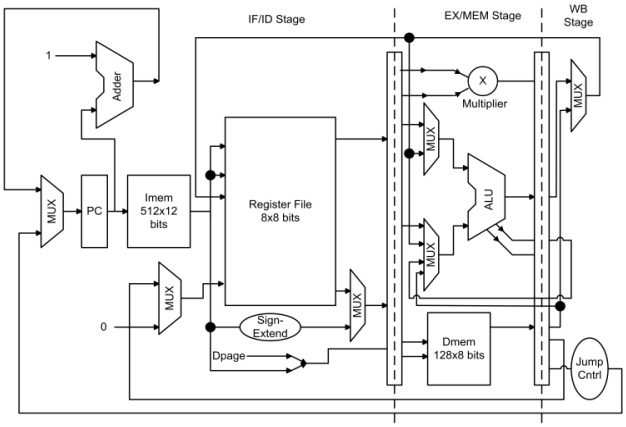

Fig. 5: SSL2Mult datapath.

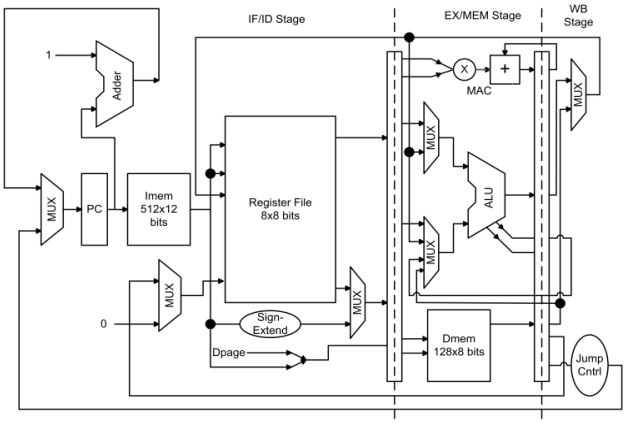

Fig. 6: SSL2MAC datapath.

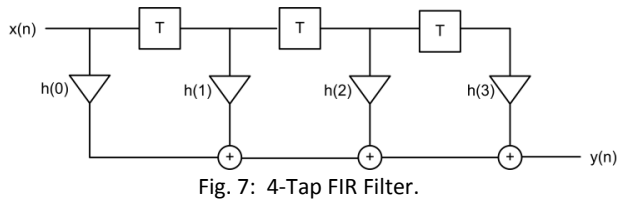

Fig. 7: 4-Tap FIR Filter.

Results and Discussion

Benchmark suits are small sized programs derived from real applications to evaluate the efficiency of processor architectures. SenseBench [29] and WiSeNBench [30] are available suits for wireless sensor networks and other energy-constrained applications. Aside from the benchmarks, well-defined efficiency metrics are essential for detailed analysis of processor performance. These metrics should be measurable and clear in order to be able to evaluate architecture efficiencies. Conventionally, energy per instruction and clock per instruction (CPI) plus clock frequency are used to describe energy consumption and processor performance, respectively [7]. However, using these parameters, we cannot provide effective comparison between RISC and CISC architectures. Therefore, as other essential metrics, we need to consider the total amount of energy consumed to execute the application (energy per data bundle), the total number of cycles to execute the application (clock cycles per data bundle), and the program size (memory footprint) for an appropriate and fair analysis [29]. Table 3 shows the composition of our benchmark applications used to compare the aforementioned efficiency metrics.

Table 3: Benchmark composition algorithms

Benchmark Application	Comments
FFT	16-point Complex-Valued Fast Fourier Transform
FIR	20-Tap FIR Digital Filter

All architecture configurations are synthesized using standard synthesis tools and custom libraries, designed and characterized with 25 basic cells in different supply voltages from 0.25V to 1V in 0.05V steps. Here we present the results of experiments on SSL2Mult and SSL2MAC in comparison to our baseline processor, SSL2.

A. Area

Table 4 shows the area results for all configurations obtained from synthesis tools with the same constraints. According to this table, about 1.5-2.6% area overhead has been added to the baseline design due to multiply and MAC units.

Table 4: Total cell area of different architecture configurations all with 512x12 bits memory

Architecture	SSL2	SSL2Mult	SSL2MAC
Area(µm2)	242228	244861	248631

B. Memory Footprint

The expected memory size of each processor

configuration differs for different benchmark applications due to ISA modifications. Table V shows the memory size categories with their corresponding memory reduction results. This table shows that the custom instruction, added to SSL2's ISA, affects the memory size (code size) only if it is used in the algorithm. For example, when FIR is executed on SSL2Mult or SSL2MAC, it needs less program memory in comparison to the baseline design. Note that for each benchmark the required program memory pages are activated and the unused pages are power gated.

According to Table 5, complex instructions reduce the data memory access (considering reads as well as writes) to 50% and 30% relative to that of SSL2 for both FFT and FIR applications, respectively. Table 5 shows that the total number of executed instructions for FFT and FIR benchmarks in both modified versions are less than that of the baseline version; therefore, the total number of clock cycles required to execute these benchmarks are reduced. As expected, these reductions in memory access reduces the memory access power consumption and total execution time.

Table 5: Memory size and number of instruction and data memory accesses for each benchmark on different configurations (unit = 12bits). The values for SSL2Mult and SSL2MAC are reported relative to those of SSL2.

Benchmark	FFT			FIR		
Architecture	SSL2 (base)	SSL2Mult (Relative to Base)	SSL2MAC (Relative to Base)	SSL2 (base)	SSL2Mult (Relative to Base)	SSL2MAC (Relative to Base)
Memory (unit)	240	0.73	0.73	112	0.57	0.43
Number of Instruction Memory Accesses	66157	0.08	0.08	47505	0.08	0.06
Number of Data Memory Accesses	5377	0.52	0.52	4324	0.32	0.29

C. *Performance*

Working frequency for different architectures vs supply voltages is shown in Fig. 9. This figure reveals that the working frequency is the same for the three configurations, that is, the critical path has remained the same.

As mentioned in the previous subsection, the total number of clock cycles needed to execute FFT and FIR benchmarks were reduced in SSL2Mult and SSL2MAC (See Fig. 8).

This fact, with no change in frequency, implies a reduction in total execution time and accordingly an improvement in performance. However, as shown in Table 6 the required clock cycles per single instruction (CPI) has increased due to complex instructions.

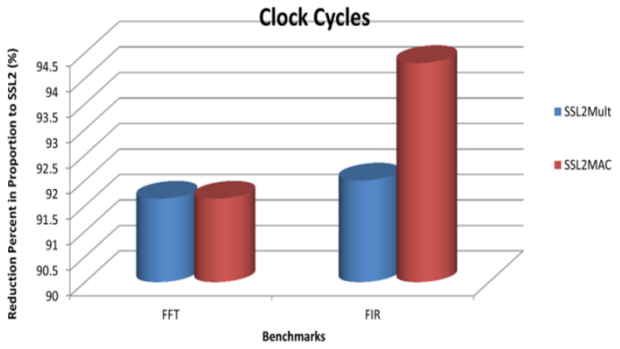

Fig. 8: Number of clock cycles reduction, in proportion to SSL2, for each benchmark running on different configurations.

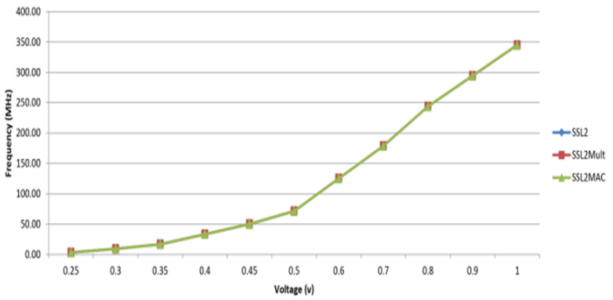

Fig. 9: Working frequency for different architectures vs supply voltage.

Table 6: Clock per instruction for each benchmark running on different configurations

Benchmark	SSL2	SSL2Mult	SSL2MAC
FFT	1.010	1.055	1.055
FIR	1.039	1.088	1.070

D. *Power and Energy Consumption*

Power consumption is estimated through simulation environment and captured VCD files in different supply voltages separately. Figures 10a and 10b depict the average dynamic and static power consumption, respectively, for benchmark applications vs. supply voltages. According to Fig. 10a, modified versions of the instruction set reduce the amount of dynamic power consumption due to memory access reduction (both for instruction and data). Core leakage has a direct relation with core area, increased with the additional units for

the complex instructions, and therefore can increase static power consumption. On the other hand, the added instruction leads to smaller program memory (smaller total area) and then lower static power consumption (see Fig. 10b). The total power consumption depicted in Fig. 10c shows that adding complex custom instructions has improved power efficiency of processor architecture. Figure 10c also shows decreasing of the supply voltage scales down power consumption for all architectures.

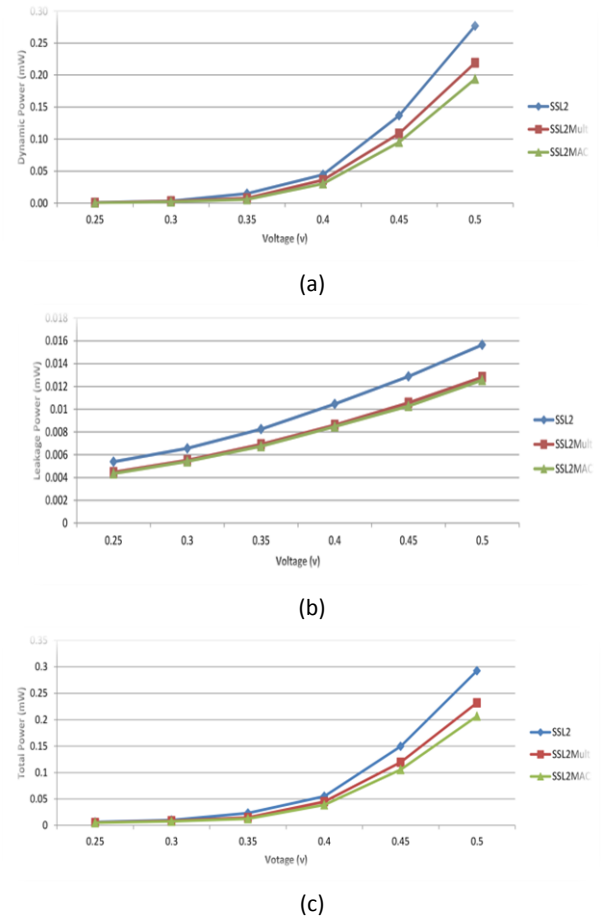

Fig. 10: Power consumption for the three architecture configurations: (a) Average dynamic power consumption; (b) Average static power consumption; (c) Average total power consumption.

The Power-Delay product of a processor is known as energy consumption and indicates the lifetime of battery-powered applications. Dynamic energy consumption depends on dynamic power consumption and on total execution time. Custom instructions improve energy efficiency in FFT and FIR applications due to execution time reduction. Figure 11a shows the average dynamic energy consumption for each configuration vs. supply voltage. Static energy consumption depends on total area and total execution time of applications. Custom instructions improve both total execution time and area, leading to lower static energy consumption for FFT and FIR applications. As shown in Fig. 11b, decreasing the supply voltage increases leakage energy consumption because of delay dominant effect. The Total energy consumption of the processor is the sum of static and dynamic ingredients and is depicted in Fig. 11c for all architectures.

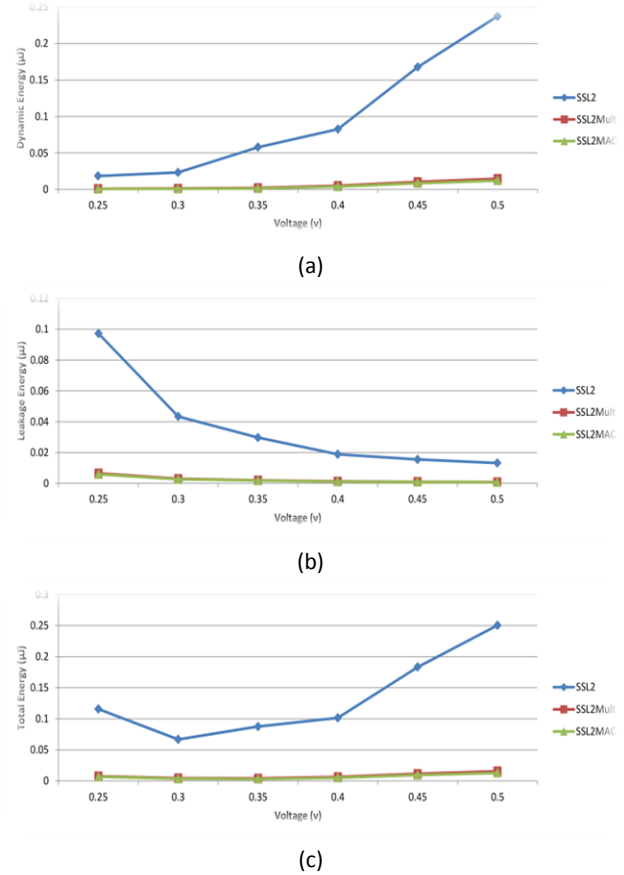

Fig. 11: Energy consumption for the three architecture configurations: (a) Average dynamic energy consumption; (b) Average static energy consumption; (c) Average total energy consumption.

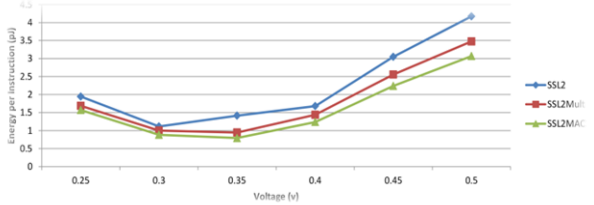

Fig. 11: Energy per instruction consumption for different architectures vs supply voltages.

This curve has an optimal point with maximum energy efficiency known as minimum energy point which is located at 0.3V for SSL2 and 0.35V for SSL2Mult and SSL2MAC. On the right side of this point, dynamic energy is dominant, and on the left side the static part dominates. According to the above results, adding complex instructions, which are commonly used in

applications, reduces energy consumption and improves performance and energy efficiency in sub-threshold region. The average consumed energy per instruction is depicted in Fig. 12.

E. Variations Analysis

Besides performance and power/energy consumption of processor, variability is another important factor needing to be considered at design time. Variation-aware design needs careful analysis based on statistical static timing analysis (SSTA) to prevent timing error occurrence due to process variations [27], [28]. Equation (1) depicts the mean (μ) and standard deviation (σ) of a normal distribution of a critical path:

$$\mu_{critical-path} = \sum_{i=1}^{n} \mu_i, \qquad \sigma^2_{critical-path} = \sum_{i=1}^{n} \sigma_i^2 \tag{1}$$

where n denotes the number of gates, and

$$\mu_{critical-path} + 3\sigma_{critical-path} = delay_{critical-path} \tag{2}$$

We note that the traditional worst-case analysis assumption led to $\sigma_{critical-path} = \sum_{i=1}^{n} \sigma_i$, yielding a much higher $\sigma^2_{critical-path}$.

Analyzing the effects of process variations on processor specifications is accomplished via Monte-Carlo simulations of the critical paths in SPICE environment for different supply voltages. Critical path delays are randomly assigned and simulated for 1000 iterations and the histogram is fitted to normal distribution to get mean (μ) and standard deviation (σ). According to Figures 13 and 14 these parameters are similar for expected architecture configurations with negligible difference. Figure 15 depicts the normal distribution of critical path for different architectures at 0.45V power supply. The results show that adding complex instructions does not change the critical path delay and so does not worsen the variability status of design around minimum working frequency.

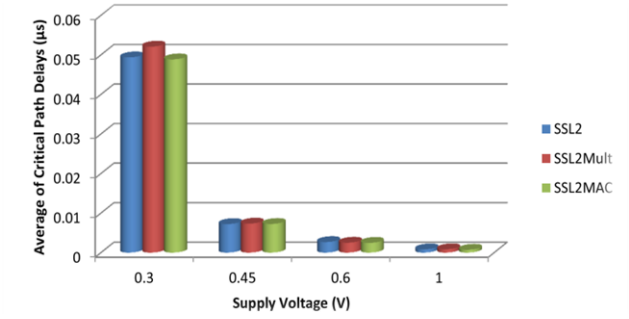

Fig. 2: Average of critical path delays in normal distribution.

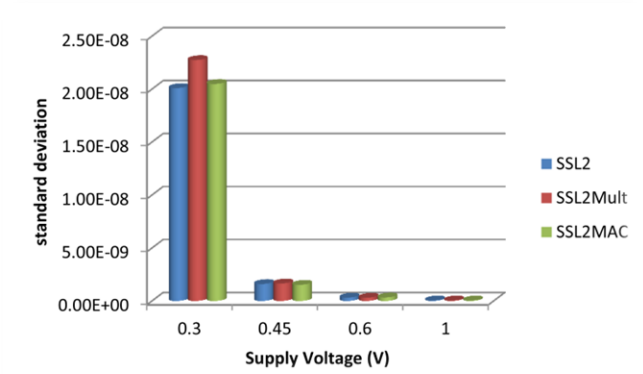

Fig. 13: Standard deviation of critical path delays in normal distribution.

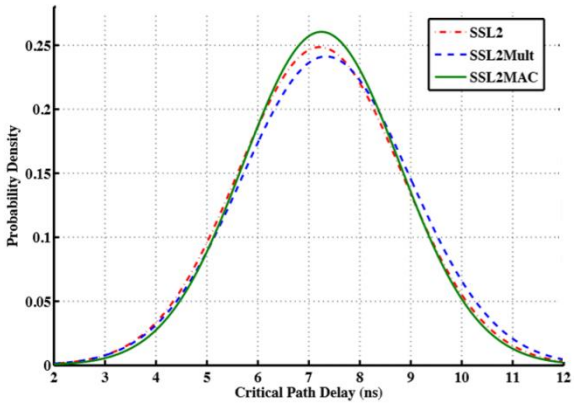

Fig. 14: Normal distribution of critical path for different configurations at 0.45V power supply.

SSL2 (Mult) in Many-Core Architectures

The idea behind many-core architectures is that hundreds to thousands small and simple cores run in parallel to achieve the desired throughput. In this section we propose a new idea: Employing ultra-low power processors as simple cores in many-core architectures. As discussed before, to reduce static energy consumption, designers try to design ultra-low power processors in small area. So the simplicity of these processors made them as good candidates for the cores in many-core architectures.

To show the efficiency of usage of our proposed processor in many-core architectures we select the FFT application in LTE standard [33]. According to this standard, a 2048-point FFT should be calculated in less than 66.6μs [34]. Thus, the desired throughput is 15.02 Ksymbol/sec and each symbol equals to a 2048-point signal. Therefore the many-core structure should provide this throughput. In addition to the existing parallelism in many-core architectures, if a pipeline structure is used, and meanwhile each pipeline stage has delay less than 66.6μs, then the desired throughput will be achieved.

Due to the data memory size of SSL2 and SSL2Mult,

these processors can execute at most a 32-point complex-valued FFT. Therefore, to execute a 2048-point FFT, the SSL2 or SSL2Mult cores should run in parallel. There are 37 ways that a 2048-point FFT can be constructed by 2,4,8,16, and 32-point FFTs. For example, assume an eleven-stage pipeline, in each stage 1024 cores running in parallel and each core executes a 2-point FFT. After 11 stages, a 2048-point FFT wil be calculated. Another example is a three-stage pipeline, in each of the first and the second stage there are 256 cores, each core executes an 8-point FFT and in the third stage, there are 64 cores each of which executes a 32-point FFT. After these three stages a 2048-point FFT will be calculated. We use this notation to represent a way: nS-mC-k + n'S-m'C-k' + ..., where n denotes the number of identical Stages and m is the number of Cores in each stage and each core executes a k-ponit FFT. The next different stages will be shown after plus symbol with the same definition. With this notation, 11S-1024C-2 represents the first mentioned example and the second one is represented by 2S-256C-8 + 1S-64C-32. Another example is shown in Fig. 16 and the corresponding notation is 1S-1024C-2 + 5S-512C-4.

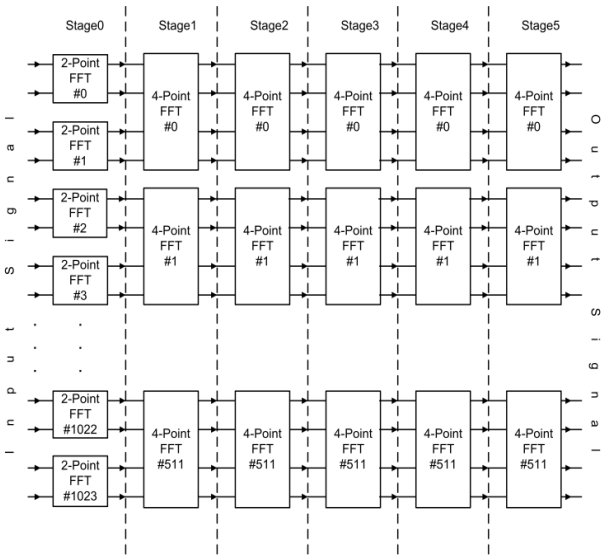

Fig. 15: One of the 37 ways that a 2048-point FFT can be constructed by 2,4,8,16, and 32-point FFTs. The representing notation for this way is 1S-1024C-2 + 5S-512C-4.

Each of the 37 ways has been investigated at 0.25V to 1.0V voltages. Among the investigated cases, those providing the desired throughput (15.02 Ksymbol/sec) are valid for us. For each aforementioned way among the valid cases, the one consuming the minimum power is called a "good case" and has been selected for that way. If we use SSL2 cores in a many-core architecture, among those 37 ways there will be only 6 good cases. On the other hand, if we use SSL2Mult cores instead, there will be 37 good cases implying that each of the 37 ways provides the desired throughput. Figures 17a and 17b show the experimental results of using SSL2 and SSL2Mult cores in a many-core architecture for a 2048-point FFT calculation in LTE standard. The vertical axis in the figure shows the required number of cores, and the power consumption has been labeled in horizontal axis. In Fig. 17a depicting the results of employing SSL2 cores, all 6 good cases providing the desired throughput have been shown. The points possessing the same throughout have been shown by a same marker. Figure 17b shows the results of employing SSL2Mult cores. For simplicity, only the good cases consuming less than 10mW power have been shown. There are 15 points in Fig. 17b. According to restrictions, namely, power or area (number of cores), the desired architecture can be selected. Among the investigated cases, those consuming the minimum power and minimum number of cores are reported in Table 7. According to this table, if the power consumption is the main concern, then the usage of SSL2Mult cores may reduce power consumption and number of cores down to 94.3% and 13.6%, respectively; and also if the main concern is the required number of cores (area), then employing SSL2Mult cores causes 84% and 85.7% reduction in power consumption and number of cores, respectively.

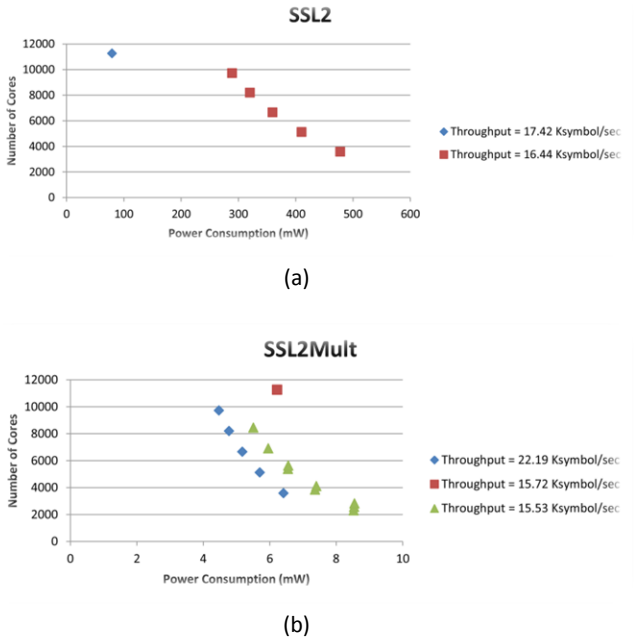

Fig. 16: Power consumption and needed number of cores for employing SSL2(Mult) in many-core architectures to calculate a 2048-point complex-valued FFT: (a) The cores are SSL2; (b) The cores are SSL2Mult.

So far, we have shown that employing SSL2Mult cores rather than SSL2 in a many-core architecture can improve power and energy efficiency. Now we show the results of employing SSL2Mult cores in a many-core

architecture and also the other implementations in literature, that are designed to calculate a 2048-point FFT in LTE standard, in order to compare the power consumption and to propose a new idea, namely, sub-threshold many-core architecture for future researches. Note that we are not proposing a many-core architecture for calculating FFT in LTE standard. Rather, we are suggesting many-core architecture with sub-threshold cores for parallel applications such as FFTs. We also show that, for example, the sub-threshold many-core architecture can reduce power consumption to about 50% or even more to calculate a 2048-point FFT in LTE standard; see Table 8.

Table7:The experimental results of usage SSL2(Mult) in a many-core architecture to calculate a 2048-point complex-valued FFT

Goal	Cores	Representing Notation of Way	Number of Cores	Supply Voltage (V)	Throughput (Ksymbol/sec)	Power Consumption (mW)
Minimum Power Consumption	SSL2	11S-1024C-2	11264	0.4	17.42	79.35
	SSL2Mult	9S-1024C-2 + 1S-512C-4	9728	0.35	22.19	4.47
Minimum Number of Cores	SSL2	1S-1024C-2 + 5S-512C-4	3584	0.6	16.43	477.68
	SSL2Mult	1S-256C-8 + 2S-128C-16	512	0.6	22.39	76.36

Table8: The Power Consumption Comparison

	Patyk[33]	Peng[34]	Yang[35]	Our Many-Core Architecture
Technology (nm)	130	180	65	90
Supply Voltage (V)	1.1	1.8	0.45	0.35
FFT Size	1024	2048	2048	2048
Throughput (Msymbol/sec)	140	35	20	0.022
Power Consumption (mW)	29.8	11.29	8.55	4.47
Energy Consumption (μJ)	1.09	2.65	0.103	2.01
Energy Consumption (nJ) / FFT Size	1.07	1.29	0.050	0.98

Conclusion

Due to advances in technology and the importance of power consumption, specially in energy constrained applications, it is necessary to make appropriate considerations in design time. In this work, we compared available ultra-low-power processors and selected the one with lower energy per instruction as our base and made some modifications in processor pipeline to achieve lower power consumption with higher throughput. Afterwards, based on our benchmark composition, we made two modified versions by adding two different custom complex instructions (Multiply and Multiply-Accumulate) as new candidates. These modifications increased the core area in one hand and also yielded smaller memory footprint for the code. In future deep sub-micron technologies, especially in sub-threshold region, due to the dominance of leakage, area efficiency implies energy efficiency. Higher density programs and smaller memory sizes improve performance and energy consumption simultaneously. Summary and analysis of results show that adding complex custom instructions to processor architecture and keeping the frequency constant will improve performance as well as energy efficiency of design without intensifying variation effects.

The results show that adding complex instructions in SSL2MAC reduce the program memory size and data memory access about 42% and 60% in average, respectively, relative to the baseline processor. The improvements in total execution time and power consumption, leads to 95% lower energy consumption in average.

Moreover, in the proposed processor, SSL2MAC, which, to the best of our knowledge, is the first sub-threshold DSP processor, the minimum energy per instruction has been improved about 29% in average compared to the baseline processor.

These improvements in power and energy consumption in conjunction with our proposed processors' simplicity led us to employ them as simple cores in a many-core architecture. Therefore, in addition to consuming less power, the performance reduction in sub-threshold circuits will be compensated. The results show that to calculate a 2048-point complex-valued FFT in LTE standard, the usage of SSL2Mult cores instead of SSL2 in a many-core architecture made 94% and 14% reduction in power consumption and number of cores, respectively.

Author Contributions

B. Soltani, H. Dorosti, and M. E. Salehi designed the experiments with the guidance of S. M. Fakhraie. B. Soltani collected the data with the help of H. Dorosti through proper simulations, and data analysis is carried out by B. Soltani and H. Dorosti. Finally B. Soltani,H. Dorosti, and M. E. Salehi interpreted the results and wrote the manuscript.

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Conflict of Interest

Authors declare that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

Abbreviations

DSP	Digital Signal Processor
ISA	Insctruction Set Architecture
FFT	Fast Fourier Transform
LTE	Long-Term Evolution
FIR	Finite Impulse Response
RFID	Radio Frequency Identification
OFDM	Orthogonal Frequency-Division Multiplexing
ALU	Arithmetic and Logic Unit
MAC	Multiply and Accumulate
RISC	Reduced Instruction Set Computer
CISC	Complex Instruction Set Computer
CPI	Clock Per Instruction
MIPS	Million Instruction Per Second
MULT	Multiply
VCD	Value Change Dump

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Research paper

A 28-36 GHz Optimized CMOS Distributed Doherty Power Amplifier with A New Wideband Power Divider Structure

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Abstract

Background and Objectives: In this paper, a new design strategy was proposed in order to enhance bandwidth and efficiency of power amplifier.
Methods: To realize the introduced design strategy, a power amplifier was designed using TSMC CMOS 0.18um technology for operating in the Ka band, i.e. the frequency range of 26.5-40GHz. To design the power amplifier, first a power divider (PD) with a very wide bandwidth, i.e. 1-40GHz, was designed to cover the whole Ka band. The designed Doherty power amplifier consisted of two different amplification paths called main and auxiliary. To amplify the signal in each of the two pathways, a cascade distributed power amplifier was used. The main reason for combining the distributed structure and cascade structure was to increase the gain and linearity of the power amplifier.
Results: Measurements results for designed power divider are in good agreement with simulations results. The simulation results for the introduced structure of power amplifier indicated that the gain of proposed power amplifier at the frequency of 26-35GHz was more than 30dB. The diagram of return loss at the input and output of power amplifier in the whole Ka band was less than -8dB. The maximum Power Added Efficiency (PAE) of the designed power amplifier was 80%. The output P_{1dB} of the introduced structure was 36dB, and the output power of power amplifier was 36dBm. Finally, the IP3 value of power amplifier was about 17dB.
Conclusion: The strategy presented in this paper is based on usage of Doherty and distributed structures and a new wideband power divider to benefit from their advantages simultaneously.

Introduction

Recently, owing to the fact that high-speed communication systems with high speed and high data rate have wide variety of applications, the transmission of data is going to be done by using modern structures, in which one of the initial necessities would be low power consumption and high efficiency. Battery life is one of the main problems related to the new wireless systems [1]. One of the main specifications between power amplifiers is that the highest value for efficiency is obtained only at its maximum output power. Efficiency significantly diminishes with reducing the output power [1]. Under normal circumstances, the power transmission of power amplifier (PA) is less than the maximum output power. Thus, the effective efficiency is far lower than the maximum value. Increasing the efficiency of the amplifier leads to a direct reduction in power consumption [2]. Doherty amplifier improves the

power efficiency for a linear power amplifier over a wide range of output powers [3].

On the other hand, the fifth generation (5G) mobile network scenario is very different from the current mobile standards (ex. LTE) in terms of both frequency band and hardware infrastructure [4],[5]. This network consist of higher cell density, and hence, lower maximum power, carrier frequency in Ka band, broadband, new access methods such as Beam Division Multiple Access (BDMA) and Massive multi-input and multi-output (MIMO) [6]. In addition, in complex modulation schemes, the maximum to average power ratio is greater than 12dB [7]. Such a scenario would definitely apply more strict requirements on the transmitter system, especially for the power amplifier, which is widely known as responsible for the linear efficiency of the entire radio [7]. Thus, the power amplifier efficiency is very significant in 5G, since it is closely related to the base station operating costs and phone battery life. Indeed, the renowned Doherty architecture obtains a high average efficiency in a wide range of RF output powers through active load modulation [8].

Another important issue in telecommunication systems is bandwidth. The most common way to design amplifier in broadband systems is distributed amplifier structure. The bandwidth and performance which are two major challenges have been the focus of power amplifier designers in recent years. Thus, in this paper, using both distributed and Doherty structures simultaneously and benefiting from the proposed wideband power divider (PD), we have been able to obtain these two important factors concurrently with acceptable values. The introduced structure was designed and simulated for a frequency range of 26 to 40GHz, using TSMC CMOS 0.18um process. All simulations have been performed in Advanced Designed System (ADS) software.

Power Divider

A. Design Principle

Commonly, the amount of power that can be achieved from the output of a single solid-state device is not enough for high frequency applications. As a result, combining the output power of several devices seems to be necessary to achieve demanded power value [9]. Different methods have been proposed for millimeter-wave power combining. One of the most familiar power divider is 3dB-Wilkinson, which is a two-way equal split type. The two-way Wilkinson combiner has applications not only at microwave but also at millimeter-wave frequencies; owing to its low losses [10]. S.B. Cohn modified the primary structure of the two-way Wilkinson in order to increase the bandwidth to one decade [10]. The method is based on substituting the one-step quarter-wave transformer with distributed parts. These parts, containing N pairs of equal-length TLs (transmission line), form the main structure of the two-way multi-stage Wilkinson PD.

Since the most important problem of single-resistor Wilkinson power divider is its very low bandwidth, in the present paper, to increase the bandwidth of the designed PD, we have combined five Wilkinson power dividers. Then, by optimizing its different parts, we have been able to extend the bandwidth very widely. Although many articles have used multistage Wilkinson power divider technique, they have not been able to achieve this broad bandwidth. In this study, all sections are curved, enhancing the bandwidth compared to the previous studies which used rectangular stubs. Indeed, when we use rectangular lines, there are fractures at angular points, which produce resonance and limit the bandwidth. The proposed power divider consists of five single Wilkinson power dividers. Accordingly, there are five resistors in the power divider which are used to isolate the two output ports. Since the introduced PD has a wide band and works up to 40GHz, a Rogers high-frequency substrate (RO5880) with the dielectric constant of 2.2 and a thickness of 0.127mm was used to design and fabricate the PD. The other advantage of the introduced PD is its compactness. The size of the introduced PD is 24.3mm×10mm×0.127mm. The schematic of the designed PD and photograph of the fabricated is shown in Fig. 1 and Fig. 2, respectively.

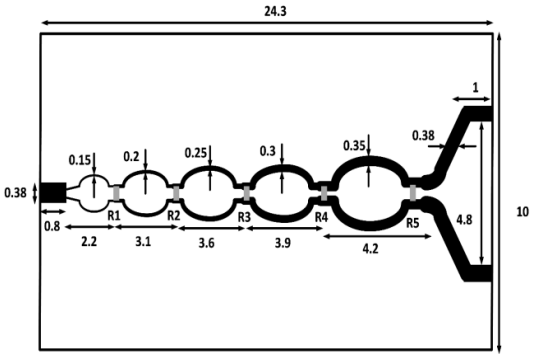

Fig. 1: Structure of introduced PD.

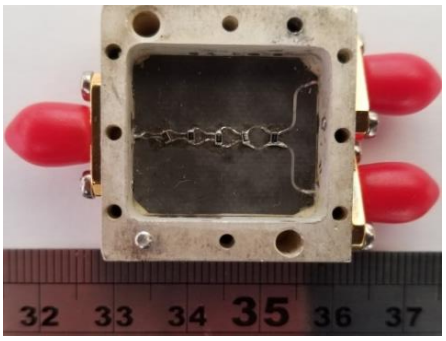

Fig. 2: Manufactured PD.

B. Simulation and measurement Results

The diagram of return losses at the three ports of the PD is shown in Fig. 3. The major advantage of the introduced PD is its wide bandwidth. It is observed in Fig. 3 that the values of return losses of the three ports of the designed PD over the entire Ka band are below -15dB, which is far lower than the benchmark of -10dB.

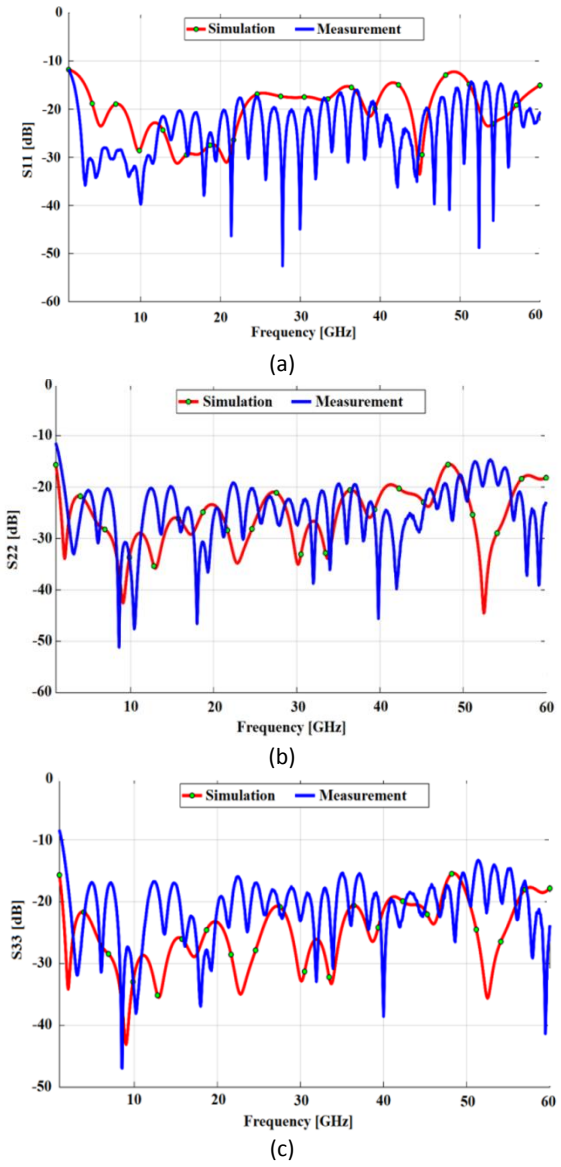

Fig. 3: Return losses at the: a) input port. b) and c) output port.

The transmission diagrams of the proposed PD are depicted in Fig. 4. It can be observed that the ripple rate of each diagram of S_{12} and S_{13} at the frequency of 1-40GHz is less than 0.4dB. Also, the inherent loss of the proposed power divider over the whole band is about 0.1dB. Hence, the sum of the ripples and inherent loss of each of the S_{12} and S_{13} diagrams at the frequency of 1–40GHz is 0.5dB. This means that the S_{12} and S_{13} diagrams, at the frequency range of 1–40GHz, is between -3dB to -3.5dB. This suggests that the inherent loss of the designed PD, at the frequency of 1–40GHz, is lower than 0.5dB.

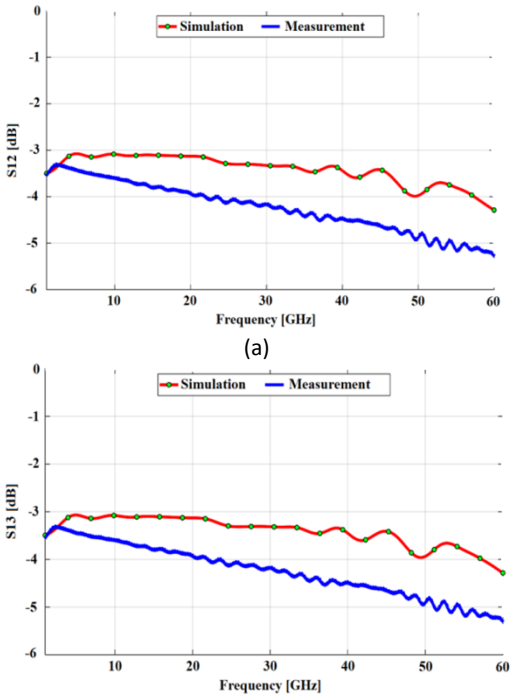

Fig. 4: Transmission diagrams.

It is observed in Fig. 5 that the isolation between the two output ports for the designed PD at 1-40GHz is less than -12dB, indicating that there is a good isolation in the proposed power divider within the entire operating band.

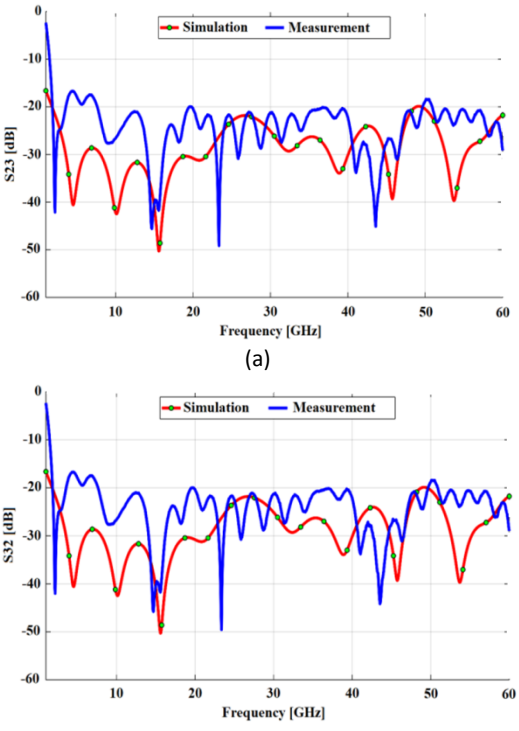

Fig. 5: Isolation of the two output ports.

A review of previous research and its comparison with the current study revealed the advantages of the proposed technique as provided in Table 1.

Table 1: Comparison between operational features of the introduced PD and others developed in previous articles

Reference	Bandwidth percentage compared to Ka band (%)	Return loss at output ports (dB)	Return loss at input port (dB)	Isolation (dB)	Inherent loss (dB)	Size (mm)	Material	Center frequency (GHz)
[10]	60	< 22	< 10	< 15	0.5	25*35	FR4	3.7
[11]	110	< 16.1	< 15.3	< 15	0.46	13*9	-	4
[12]	42	< 10	< 10	< 8	0.8	10.95*10.2	RO5880	38
[13]	100	-	< 15	-	0.6	35*45	RO5880	4
[14]	133	< 15	< 15	< 20	0.5	42*26	RO5880	6
[15]	90	< 15	< 15	< 15	0.4	55*31	FR4	1.1
[16]	109	< 17	< 14.7	< 15.3	0.52	21*4.6	-	6.8
[17]	101	< 10	< 10	< 10	1	-	-	6.3
This work	**190**	**< 22**	**< 14**	**< 12**	**0.45**	**10*24.3**	**RO5880**	**20.5**

Power Amplifier

In power amplifiers, the efficiency is defined as the ratio of the average output power to DC power consumption. Power amplifiers operate mostly on the average power. Indeed, they spend a short time at the maximum power. Thus, their average power efficiency is very important. In conventional amplifiers such as class A, B, and AB power amplifiers, the higher the efficiency at higher powers, the lower the average power efficiency. The high average efficiency is one of the essential parameters for mobile systems, when battery lifetime is considered. To enhance this parameter, a wide variety of solutions have proposed during the history [18]. W. H. Doherty introduced an effective approach in 1936 [19].

The Doherty Power Amplifier (DPA) is according to the modulating the load of an amplifying device. Hence, this process will result in operating of the amplifier at its highest efficiency for a pre-destined value of input and/or output power [20]. As a result, the termination of the amplifying device, Main (or Carrier), is modulated based on load modulation idea [21], [22], by utilizing another active device, Auxiliary (or Peaking). A general structure for Doherty power amplifier is shown in Fig. 6.

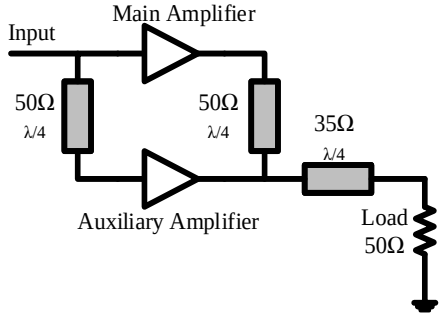

Fig. 6: Typical DPA configuration.

The load modulation circuit operates based on the idea of combining the asymmetric power obtained from the output of both active devices in a current-combining manner. Therefore, the main amplifier functions with maximum performance at a low-power condition and the maximum performance at the higher-power situation [7]. In general, a power amplifier, with certain optimized termination impedance, provides the utmost effectiveness merely at maximum power because the full output voltage and current fluctuations are obtained merely at the maximum of the output power described by the constant load. The dynamically load modulation of DPA will result in the maximum performance at the various power levels specified by the modulated load. In the load modulation process, the carrier amplifier gives the peak effectiveness at one-second of the utmost input voltage, and the utmost effectiveness is kept via this process at a greater power as depicted in Fig. 7.

Fig. 7

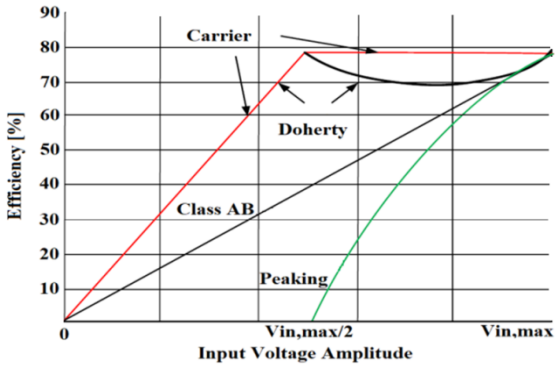

Fig. 7: Efficiencies of DPA vs. input voltage for DPA.

In the low-power area ($0<V_{in}<V_{in,max}/2$), the auxiliary amplifier stays in the cut-off condition, and the load of the main amplifier is twice as large as that of the conventional structure. Therefore, the carrier amplifier achieves the saturation condition at the input voltage of ($V_{in,max}/2$), because the utmost fluctuation of voltage obtains V_{dc} at one-second the current highest level. Consequently, the peak power value is one-second that of main amplifier, and the effectiveness of the DPA is as same as the utmost effectiveness of the main amplifier. In this low-power behavior, merely the main amplifier

with a one-second of the whole power cell generates power, and the effectiveness at a pre-determined power value is double as high as a power cell amplifier [7].

In the higher-power region ($V_{in,max}/2<V_{in}<V_{in,max}$), in which the auxiliary amplifier is ON, the main amplifier produces power with the maximum effectiveness, because the saturated operation is kept owing to the load modulation.

The auxiliary amplifier functions at a large load at the turning on state, and the effectiveness enhances quickly; however, it is still less than the maximum effectiveness. Therefore, the whole effectiveness of the DPA structure is decreased.

However, the next point for effectiveness is obtained when the peaking amplifier with saturated operation generates the utmost effectiveness at the maximum power.

Thus, it has two utmost effectiveness places, improving the effectiveness at the back off output power value as illustrated in

Fig. 7. As a result, the effectiveness of the Doherty structure at the peak point of the input voltage is as same as the utmost effectiveness of the known amplifiers [7].

Hence, the DPA structure generates more effectiveness across the whole power levels in comparison with an ordinary class B amplifier. The obtained structure for DPA can overcome the low efficiency difficulty for amplification of a large peak to average power ratio (PAPR) signal. Thus, DPA structure would be a good choice to increase effectiveness. On the other hand, one of the main concerns about DPA is the limited RF bandwidth.

In Broadband data transmission and receiving systems as well as applications requiring broadband linear phase amplification, there are various approaches to design amplifiers. The most common way is distributed amplifiers structure. Distributed amplifiers (DA) are usually used as a suitable broadband amplifier in telecommunications.

Since they have a stable gain over a wide bandwidth, they prevent the scattering of the received signals [23]. The main idea in the distributed structure is to use multiple cascade transistors to enhance the gain and promote simultaneous absorption of parasitic capacitors into drain and gate transmission lines to acquire a broad bandwidth [24].

The principal form of the distributed amplifier can be seen in Fig. 8, in which a cascade of identical transistors are used, while their gates joined to a TL with a characteristic impedance of Z_{0g} and a length of l_g, and their drains are joined to a TL with a characteristic impedance of Z_{0d}, and a length of l_d [25].

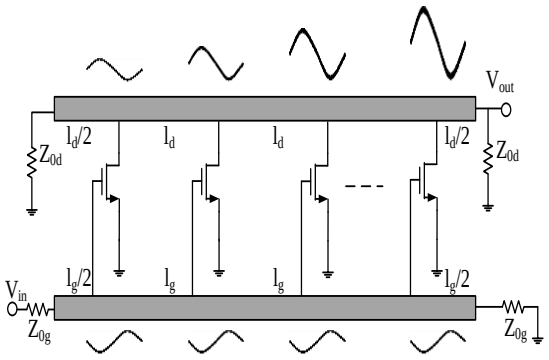

Fig. 8: Basic structure of the distributed amplifier.

The DA structure is based on simultaneous enhancement of the gain and bandwidth of power amplifier [25].

The input voltage wave propagates via the gate line and attains the gate of the transistors with phase shifts. Each transistor increases its gate voltage and produces a drain current via the drain line. If the gate and drain line parts cause same phase shifts, i.e.,

$$\beta_g l_g = \beta_d l_d \quad (1)$$

where β_g and β_d is the propagation constant of the gate and drain line, respectively, the drain current obtains the termination impedance and effective combine. These lines are ended in their termination characteristic impedance at the other end to attract waves moving in the opposite ways [25]. It is assumed that, the transconductance gain of each element is G_m and the output impedance can be observed by transistors, is one-second of the characteristic impedance of the TL, the gain of the voltage is as (2):

$$A_v = \frac{1}{2} n G_m Z_{0d} \quad (2)$$

Here, n is the number of stages and Z_{0d} is characteristic impedance of the drain line. The gain of the distributed amplifier can be enhanced via utilizing further stages or higher G_m. Z_{0d} is tuned by the condition of output impedance matching. It should be considered that (2) is obtained supposing lossless TLs. Due to the existence of loss in TLs, the voltage amplitude weakens as it propagates the gate and drain lines. This result cause the degradation of voltage gain in case further stages are utilized [25]. Hence, there would be an optimized number of gain stages that causes the voltage gain enhancement. The circuit schematic of Fig. 8 assumes that parasitic capacitances of the transistors are evenly propagated along the TLs. The model presented in Fig. 8 cannot propose a realistic evaluation of the DA bandwidth. Moreover, the distributed amplifier could be introduced by lumped-element artificial TLs as depicted in Fig. 9.

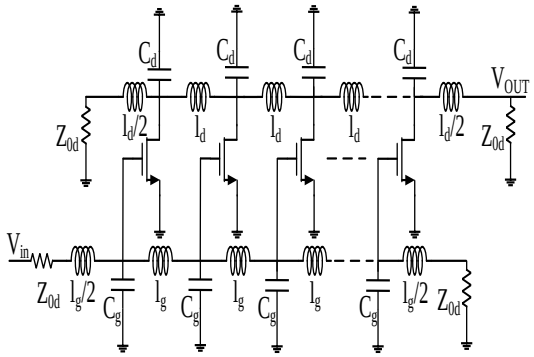

Fig. 9: Distributed amplifier structure constructed by lumped-element artificial transmission lines.

The condition (1) is changed as

$$l_g C_g = l_d C_d \quad (3)$$

Here, C_g and C_d are capacitances at the gate and drain of each transistor, whereas L_g and L_d indicate the inductance of the gate and drain lines, respectively. The bandwidth of the distributed amplifier is restricted by the cut-off frequency of the gate and drain lines. The cut-off frequency can be obtained as follow [25]:

$$\omega_C = \frac{2}{\sqrt{LC}} \quad (4)$$

Here, L and C are the inductance and capacitance of the lumped-element line, supposing that gate and drain lines have equal cut-off frequencies. The wave crossing via the lumped-element line is significantly attenuated over the cut-off frequency. Transistors in small size should be used to obtain higher bandwidth that will decrease the gain of distributed amplifiers. Since the characteristic impedance of the lines is specified by the ratio of L/C, inductance L would not be small to obtain more bandwidth. Therefore, there exists a trade-off between gain and bandwidth in distributed amplifiers. The input capacitance of transistors is the main parasitic capacitance that confines bandwidth of distributed amplifiers. Coupling by using capacitor is an introduced way to reduce the loading result of the gate-source capacitance on the gate line [25]. A capacitor is put in series with the gate of transistors to decrease the capacitance to $C_{gs}=(1 + C_{gs}/C_c)$ [Fig. 10 (a)].

A large resistor in parallel with C_C makes a way for the gate bias. It is worth mentioning that the gain of voltage is decreased by the factor $1 + C_{gs}/C_C$ owing to the splitting of voltage at the input of transistors. The method is generally applied in distributed amplifiers in which the gate-source capacitance of large transistors can confine bandwidth and gain is not the initial priority in design procedure. Other method proposed to decrease the loading result of the input impedance of transistors is utilizing a common-source amplifier with R_C degeneration Fig. 10 (b) as the gain stage. The impedance can be seen at the input of the amplifier is obtained as a series resistance and capacitance. i.e. $Z_{in} = R_{in} + 1/j\omega C_{in}$. With appropriate adjustment of the circuit elements, the parameters of the amplifier are achieved as $R_{in} = 0$, $C_{in} = C_{gs}=(1 + g_m R_s)$, and $G_m = g_m=(1 + g_m R_s)$. Therefore, the input capacitance is declined, that will result in transconductance degradation. In fact, the elements of the circuit are adjusted to obtain negative input resistance. This method is utilized to minimize the loss impact of the gate TL and input parasitic resistance of the transistor. The cascode amplifier depicted in Fig. 10 (c) is a popular structure can be utilized to make high isolation between input and output of the distributed amplifier. The inter-stage inductance transfers the pole related to the inter-stage parasitic capacitance to higher frequencies, and thus, enhances bandwidth [26].

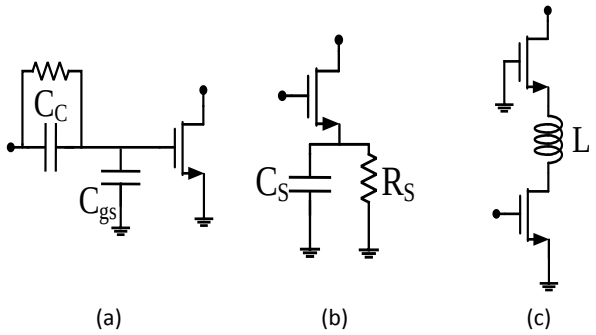

Fig. 10: The conventional structures can be utilized as gain stage of distributed amplifiers. (a) Capacitive coupling, (b) Source RC degeneration, (c) Bandwidth-improved cascode amplifier

To enhance the gain of the distributed amplifier, multi-stage amplifiers are used as the gain stage. Bandwidth improvement methods can be applied to prevent bandwidth constraints by inter-stage parasitic capacitances. The amplifier stages have a bit different 3-dB bandwidths and gain enhancement near the cut-off frequency. The amplifier stages are accurately set to propose a flat gain response [26]. Multiple distributed amplifiers can work in cascade way in order to acquire more gain. The cascaded single-stage DA (CSSDA) is a structure established to obtain high gain and wide bandwidth [27]. The structure presented in this paper is based on simultaneous usage of Doherty and distributed structures in a power amplifier to benefit from their advantages simultaneously. The power divider designed in the previous section, which has a very wide bandwidth, is also used to divide the input power to achieve a wider bandwidth. To combine the power at the output of proposed amplifier, the power divider designed in the previous section is also used in reverse. Fig. 11 depicts the block diagram of the proposed power amplifier.

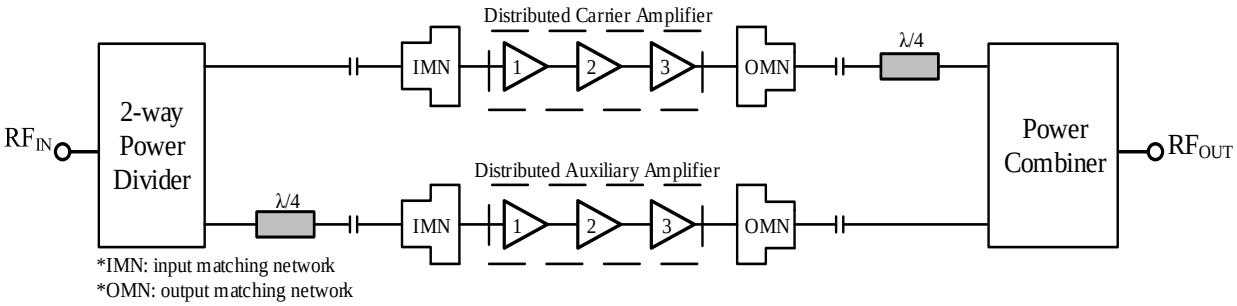

Fig. 11: Introduced structure for PA.

In Fig. 11, the main and auxiliary amplifiers are based on a distributed structure. Based on Fig. 11, each of the main and auxiliary distributed amplifiers is composed of three different parts, represented by 1, 2, and 3, all of which are connected to each other in a cascade manner.

Since the traditional power amplifiers have a high bandwidth but low gain, the tapered cascaded multistage distributed amplifier (T-CMSDA) method was used to improve the gain in the proposed power amplifier (as in reference [28]). Section 1 in Fig. 11 of both main and auxiliary amplifiers has two major tasks: i) matching at the input; and ii) improving the saturation status of the amplifier. In other words, this section functions like a pre-amplifier. Section 1 which is displayed in Fig. 12, is a three-stage distributed amplifier consisting of 6 transistors.

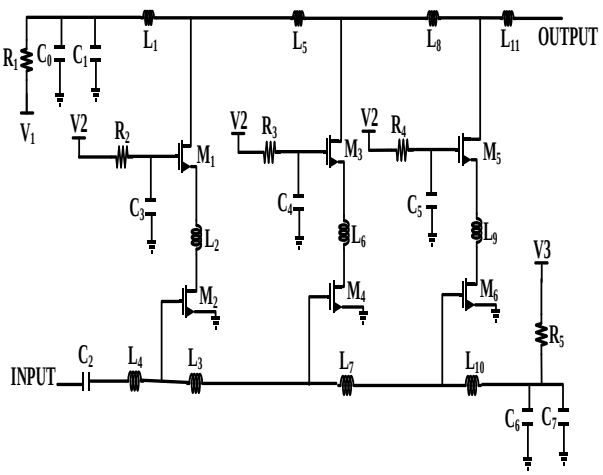

Fig. 12: Schematic view of Section 1.

Section 2 shown in Fig. 13 consists of four transistors, responsible for matching the two sections 1 and 3 and increasing the gain.

Section 3 in

Fig. 14 consists of six transistors linked in a distributed manner functioning as the main amplifier. The amplification job is mainly performed in Section 3 and a small part in Section 2.

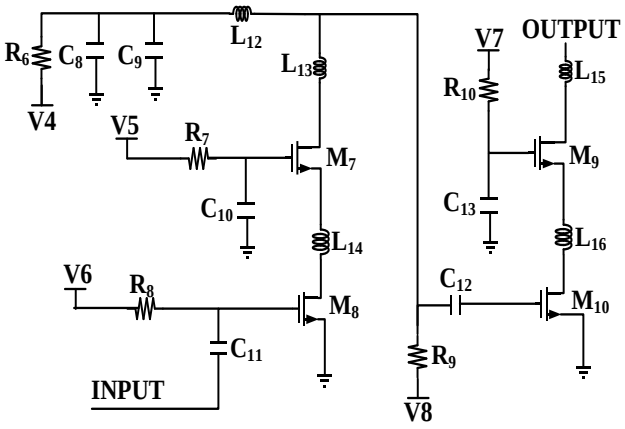

Fig. 13: Schematic view of Section 2

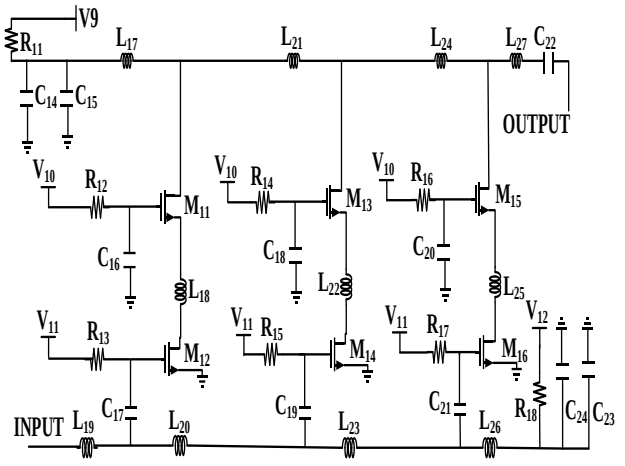

Fig. 14: Schematic view of Section 3.

Simulation Results

A. Scattering Parameters

Fig. 15 illustrates the parameter S_{21} for the introduced PA.

It can be observed in Fig. 15 that the proposed circuit gain in this state is 32dB at 30GHz. Over a wide area of the Ka band, i.e. from 26-34GHz, the gain is more than

30dB. The S_{11} or input return losses diagram of designed power amplifier is indicated in Fig. 16.

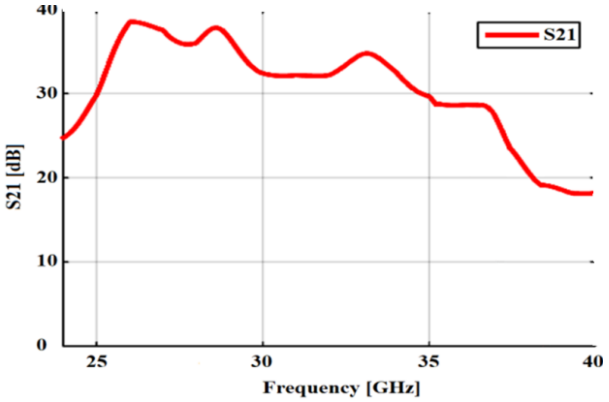

Fig. 15: The S_{21} parameter for the introduced PA.

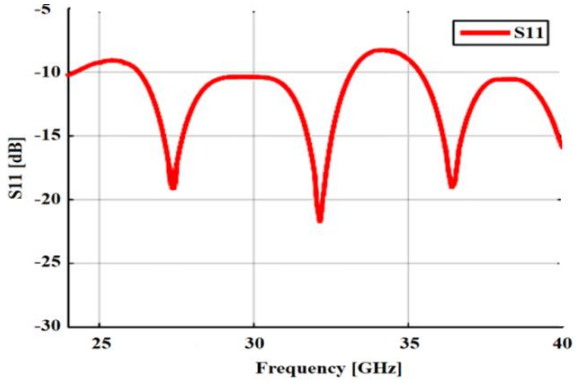

Fig. 16: Input return loss of the proposed PA.

Fig. 16 displays that over the frequency range of 26-40GHz, the parameter S_{11} is below the -8dB. Hence, there is acceptable approximate matching in the input within this frequency range at the input terminal.

The S_{22} or output return loss diagram for the proposed power amplifier is shown in Fig. 17.

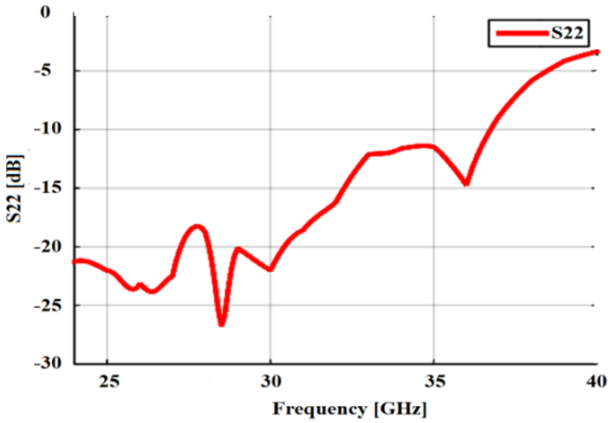

Fig. 17: Output return loss of the introduced PA.

It could be observed in Fig. 17 that over the frequency range of 26-37GHz, the S_{22} parameter is below -10dB; thus, there is acceptable approximate matching within this frequency range at the output terminal.

The S_{12} parameter indicates isolation whose smaller values are more desirable. The S_{12} diagram is shown in Fig. 18 for the designed PA.

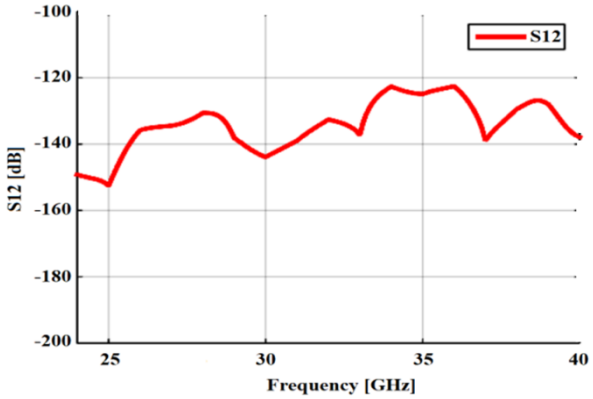

Fig. 18: S_{12} parameter for the introduced PA.

It is observed in Fig. 18 that the isolation in the proposed circuit is less than -120dB for the entire Ka band, which is very good.

B. Power Added Efficiency (PAE)

Power Added Efficiency is generally used to analyze the efficiency of a PA under high gain conditions, and is a determining parameter for the RF power amplifiers. The PAE is demonstrated in Fig. 19 in terms of input power, i.e. P_{IN} for designed power amplifier at 26, 30, and 34GHz.

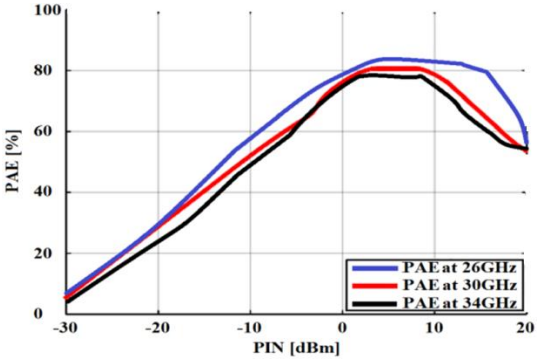

Fig. 19: PAE in terms of input power.

Fig. 19 reveals that at the P_{IN} of 5dB, the power efficiency is at its maximum, about 80%, twice as much as the previous amplifiers.

C. Gain

For an ideal linear amplifier, the output power in terms of the input power is a straight line with a slope of 1, where the amplifier gain equals the output to the input power ratio. At a specific range, the amplifier response follows a linear response and then begins to saturate, leading to diminished gain. To determine the range of the linear performance of the amplifier, the 1dB

compression point is defined, at which, changes in the output power are decreased by 1dB compared to the input power. In order to calculate the P_{1dB} point, the gain should be considered for different values of the input power. The point at which the gain is 1dB lower than the primary value, that is the linear gain of the amplifier at low powers, is specified as the 1dB compression point of input power, or P_{1dB} input point. On the other hand, the P_{1dB} output point could be calculated independently of the input P_{1dB} and considering the 1dB compression gain. For this purpose, the gain value should be investigated similarly for different output power values. The point at which the gain is 1dB lower than the primary value, that is the linear gain of the amplifier at low powers, is specified as the 1dB compression point of the output power, or P_{1dB} output point. The gain diagram of the designed power amplifier in terms of input power at 26, 30, and 34GHz is indicated in Fig. 20.

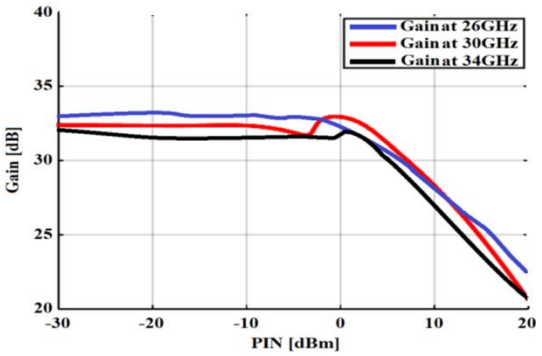

Fig. 20: Gain graph in terms of input power.

It could be observed in Fig. 20 that the P_{1dB} input point of the proposed amplifier is 4dBm at a frequency of 30GHz. Also, the gain value of the proposed amplifier is 32dB at 30GHz.

The diagram of output P_{1dB} point for the introduced PA is illustrated in Fig. 21.

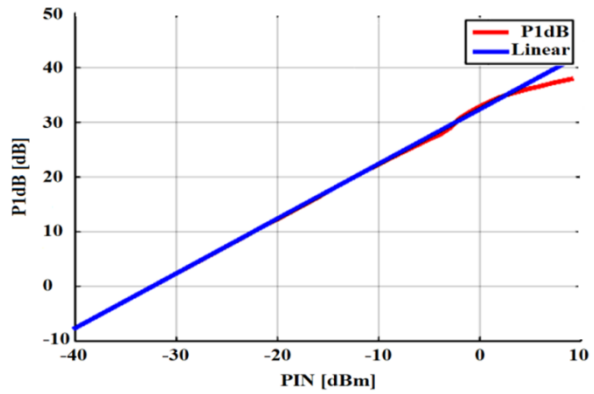

Fig. 21: Output P1dB for the introduced PA.

Fig. 21 depicts the value of P_{1dB} in the introduced PA for the output power of about 35.9dB, which is far greater than that of previous articles.

D. Output Power

The output power of the designed PA in terms of the input power at 26, 30, and 34GHz is shown in Fig. 22.

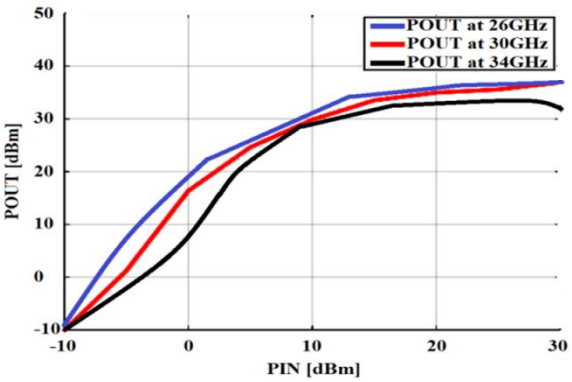

Fig. 22: Output power in terms of input power.

It can be observed in Fig. 22 that the output power of the introduced PA is about 35dBm, which is higher than that of previous articles.

E. Stability

With feedback coming from the output to the input, the amplifiers may become unstable. Stability can be achieved through S parameters. The most commonly used definition for stability is the Stern stability factor, which is given as (2):

$$K = \frac{1 + |\Delta| - |S_{11}|^2 - |S_{22}|^2}{2|S_{11}||S_{22}|} \quad (5)$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (6)$$

If the following condition is met, stability is called unconditional. In other words, for each input and output impedance, the PA is stable:

$$K > 1\,, \Delta < 1 \quad (7)$$

Fig. 23 reveals a graph of K drawn based on the Stern stability factor as a criterion for evaluating the stability of the proposed structure.

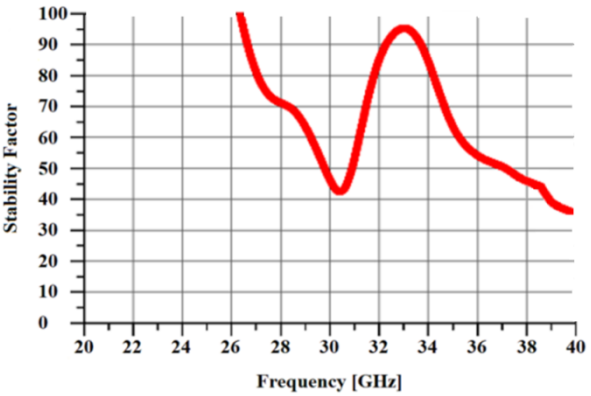

Fig. 23: Graph of K based on the Stern stability factor.

It can be observed in Fig. 23 that the value of K (Stern stability factor) for all frequencies within the range of 26-40GHz is greater than 30. In addition, the value of Δ has calculated using (3) at 26, 30, and 34GHz. The obtained value for Δ in all three mentioned frequencies is less than 1.

Therefore, the proposed power amplifier is unconditionally stable.

F. IP3

The relationship between P_{1dB} and IP3 is useful for the third-order nonlinear property, as follows:

$$P_{1dB}=IP3-9.6dB \quad (8)$$

For an amplifier or receiver in the linear performance region, IP3 has a constant value and does not change with increasing input power.

The IP3 for the introduced PA at 30GHz is depicted in Fig. 24.

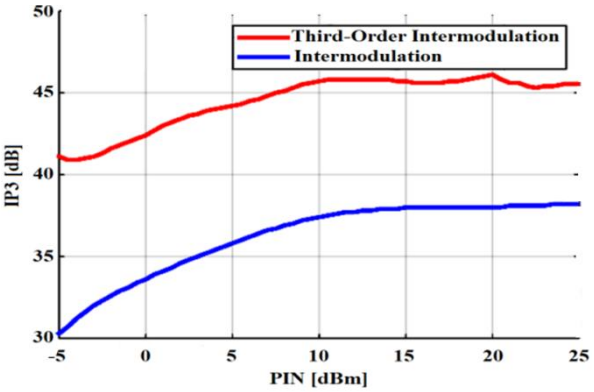

Fig. 24: IP3 for the introduced PA at 30GHz.

It is seen in Fig. 24 that the IP3 value of the proposed amplifier is about 17dB.

A review of the previous articles and their comparison with the current study indicated the advantages of the proposed technique over others as in Table 2.

Table 1: Comparison between the proposed power amplifier with previous articles

Reference	Frequency (GHz)	Gain (dB)	PAE (%)	Biasing Voltage (Volt)	Technology
[27]	40	23.4	28.5	-	SiGe
[28]	28.5	15	37	8	GaAs
[29]	29.5	10.5	38	4	GaAs
[30]	42	7	23	2.5	SOI-CMOS
[31]	32	22	21	1	Bulk CMOS
[32]	70	20	14	1.5	CMOS
[33]	30	15.7	35.5	1	CMOS
[34]	28/37/39	18.2	20.3	1.5	SiGe
[35]	28	11.8	42	4	GaAs
[36]	1.6-2.6	7.6-9.6	53-66	26	GaN
This work	**30**	**32**	**80**	**3.8**	**CMOS 0.18um**

Conclusion

This paper introduced a new structure for power amplifiers for operating in Ka band based on applying Doherty and distributed methods in order to benefit from their advantages simultaneously. To design the Doherty power amplifier, first a power divider with a very wide bandwidth, i.e. 1-40GHz, was designed, to cover the entire Ka band. The power amplifier structure presented in this paper was based on Doherty method, which consists of two signal amplification paths, known as main and auxiliary. To amplify the signal in each of the two pathways, a cascade distributed power amplifier was used. The gain of the proposed power amplifier at the frequency of 26-35GHz was more than 30dB. The return losses at the input and output of PA in the entire Ka band was less than -8dB. The maximum PAE of Doherty power amplifier was 80%. The P_{1dB} output point of the proposed power amplifier was 36dB, and the output power of designed power amplifier was also 36dBm.

Author Contributions

M. S. Mirzajani Darestani introduced all the new structures in the paper and has done all the simulations. In addition, he has done the laboratory tests and prepared the current version of the paper. M. B. Tavakoli and P. Amiri provided scientific and technical advices to the first author and they corrected mistakes during the simulation, laboratory tests, and preparation of the paper process.

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Conflict of Interest

The authors declare that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism,

informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy, have been completely observed by the authors.

Abbreviations

PAE	Power Added Efficiency
DPA	Doherty Power Amplifier
DA	Distributed Amplifier
PD	Power Divider
IMN	Input Matching Network
OMN	Output Matching Network

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Research Paper

Link Prediction Using Network Embedding Based on Global Similarity

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Abstract

Background: The link prediction issue is one of the most widely used problems in complex network analysis. Link prediction requires knowing the background of previous link connections and combining them with available information. The link prediction local approaches with node structure objectives are fast in case of speed but are not accurate enough. On the other hand, the global link prediction methods identify all path structures in a network and can determine the similarity degree between graph-extracted entities with high accuracy but are time-consuming instead. Most existing algorithms are only using one type of feature (global or local) to represent data, which not well described due to the large scale and heterogeneity of complex networks.

Methods: In this paper, a new method presented for Link Prediction using node embedding due to the high dimensions of real-world networks. The proposed method extracts a smaller model of the input network by getting help from the deep neural network and combining global and local nodes in a way to preserve the network's information and features to the desired extent. First, the feature vector is being extracted by an encoder-decoder for each node, which is a suitable tool for modeling complex nonlinear phenomena. Secondly, both global and local information concurrently used to improve the loss function. More obvious, the clustering similarity threshold considered as the local criterion and the transitive node similarity measure used to exploit the global features. To the end, the accuracy of the link prediction algorithm increased by designing the optimization operation accurately.

Results: The proposed method applied to 4 datasets named Cora, Wikipedia, Blog catalog, Drug-drug-interaction, and the results are compared with laplacian, Node2vec, and GAE methods. Experimental results show an average accuracy achievement of 0.620, 0.723, 0.875, and 0.845 on the mentioned datasets, and confirm that the link prediction can effectively improve the prediction performance using network embedding based on global similarity.

Introduction

Graphs are one of the most widely used data structures in computer science and related fields. Social networks, protein-protein interactions, and recommender networks are the data structures modeled on the graph. In recent years, due to the widespread networks used in the real world, the analysis of graphs has attracted more consideration. Node classification [1], link prediction [2], community detection [3], and recommender system [4] are widely used in the field of graph analysis [5] which

link prediction has been considered in this paper. For more insight, your next connection on Facebook can be distinguished, using link prediction. The application of link predictions is not limited to social networks; For example, in the bioinformatics field, link predictions are used to detect protein-protein interactions [6]. In the field of e-commerce, link prediction is applicable to create a suggestion system [7]; and in security, it can help to find hidden terrorist groups [8]. As shown in Fig. 1, link predictions can be used to identify improper links and remove them from the network and also the investigation of the links to predict potential relationships between users and a social network [9].

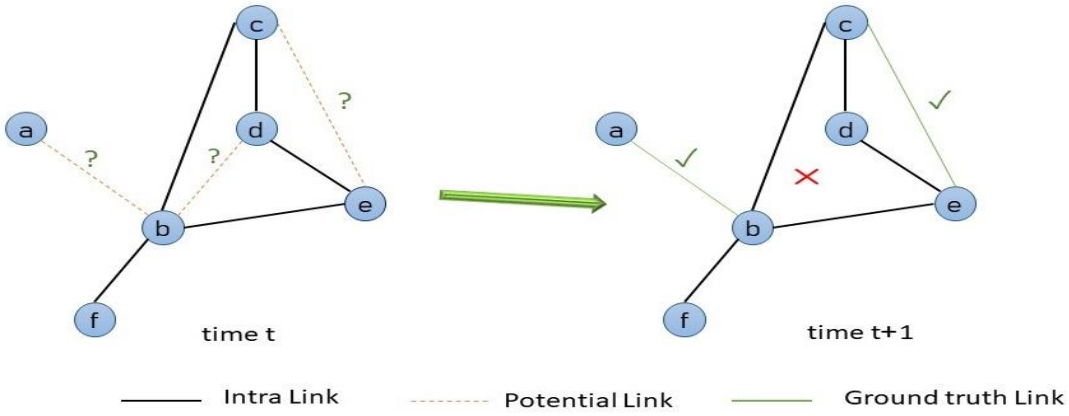

Fig. 1: An example of a bond prediction on a 6-node test graph.

So far, a variety of methods have been proposed for Link Prediction which includes, similarity-based methods [10,11], the maximum likelihood estimations (local and global) [12,13], and probabilistic methods [14,15]. Also, in recent years, we have seen an increment of approaches that automatically learn to encrypt the graph structure in nonlinear and low dimensional vectors. The idea of such methods is learning a data conversion function that attributes nodes to points in a vector space with low dimensions associated as embedding a node. The goal is to achieve a map of nodes in the whole network that represents all their structural features in the main graph. The node embedding techniques have led to advanced developments in network science [16]. As shown in Fig. 2, a node embedded on a small graph with 6 vertices; Every node, like u, is automatically converted to a numerical representative vector in the d-dimensional space, which d << n and n is the number of vertices in the graph.

Finally, the initial graph converts to n vectors which, has shown on the right side of Fig. 2.

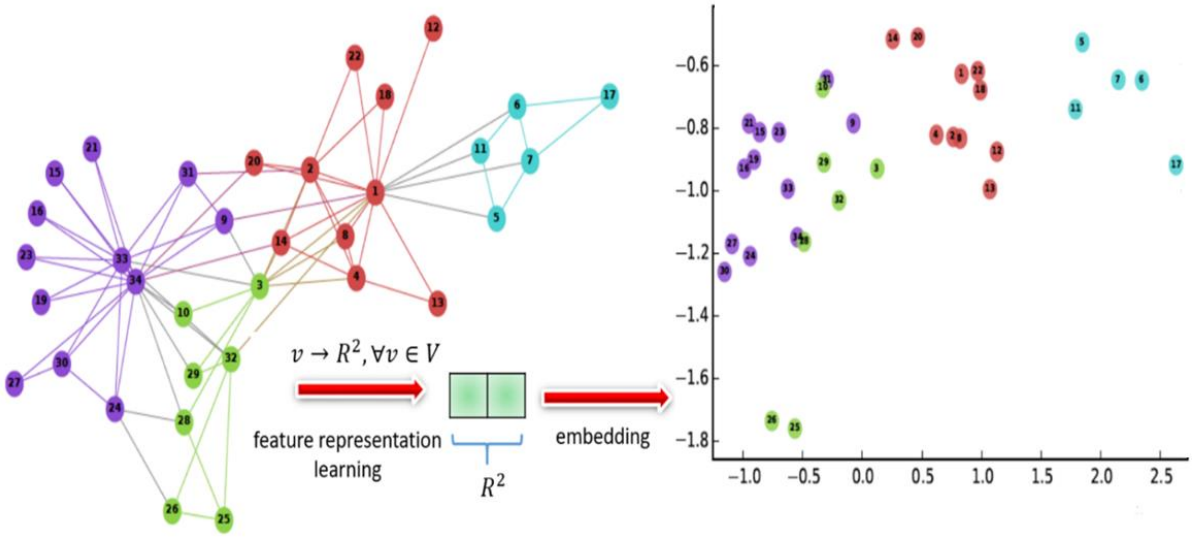

Fig. 2: left is, Graph structure of the Zachary Karate Club social network, where nodes are connected if the corresponding individuals are friends. The nodes are colored according to the different communities that exist in the network. right is, two dimensional visualization of node embedding generated from this graph using the DeepWalk method. The distances between nodes in the embedding space reflect similarity in the original graph, and the node embedding are spatially clustered according to the different color-coded communities [17].

The main challenge of using graphs in machine learning and link prediction is finding a way to extract information about the interaction between nodes, and integrate them into a machine learning model. To extract this information from networks, older approaches often use limited statistical information (such as vertices degree or clustering coefficients) or computational features to measure local neighbors. These classic approaches have limitations because these features are not flexible. They

often do not generalize to networks derived from other organisms, tissues, and experimental technologies, and only operate in a set of data with low experimental coverage [17].

In the following paper, a new node embedding approach presented for link prediction in the network to solve the existing challenge. Because depthless or superficial embedding methods are not able to use node features when encrypting. The proposed method designs a cryptographic-decoder that uses local and global attributes to identify information about the structure and characteristics of the graph. Therefore, the attribute vector extracted for any nodes, using a deep neural network, which is a suitable tool for modeling nonlinear-complex phenomena. Also, the link prediction accuracy has improved simultaneously, using global and structural information. In related work section, we will review the related works in the link prediction field. The proposed method to solve the problem of link prediction and the experiment results and their analysis have been presented in proposed method section and evaluation section, respectively. Finally, in conclusion section, we conclude and consider this issue related research path.

Related Work

Graph embedding methods can be divide into three groups: 1-Matrix factorization-based methods, 2-Random walk-based methods, 3-Neural network-based methods [18]. The characteristics of each above categories briefly provided in Table 1.

A. Matrix factorization-based methods

Matrix factorization-based methods represent the relationship between nodes in the form of a matrix. The purpose is to convert the data matrix into lower-dimensional matrices in a way that the main matrix's topological specification, structure, and characteristics be preserved [18]. To show the relationship among nodes, the node adjacency matrix, laplacian matrix, or Node transition probability matrix are applicable. Approaches to determining the matrix factor vary based on the matrix characteristics.

If the resulting matrix includes zeros and ones, as instance, For the Laplace matrix, eigenvalue decomposition, and for the unstructured matrices, gradient descent methods can be picking to obtain linear time embedding [16].

Table 1: List of graphs embedding methods [16]

Type	Similarity	Method	Year
Based on matrix factoring	1st degree neighbors	Laplacian Eigen maps [32]	**2001**
Based on matrix factoring	1st degree neighbors	Graph Factorization[19]	**2013**
Based on matrix factoring	Neighbors up to K distance	GraRep [21]	**2015**
Based on matrix factoring	Neighbors up to K distance	HOPE [22]	**2016**
Random walk-based	Neighbors up to K distance	DeepWalk [23]	**2014**
Random walk-based	Neighbors up to K distance	Node2vec [24]	**2016**
Based on the neural network	1st degree neighbors & 2nd degree neighbors	SDNE [20]	**2016**
Based on the neural network	Neighbors up to K distance	GCN [28]	**2017**
Based on the neural network	1st degree neighbors & 2nd degree neighbors	LINE [26]	**2015**

GraRep and HOPE algorithms are working based on matrix factorization. Due to the review of all pairs of nodes, time complexity in these methods is O (V^2), so high computational costs are one of the challenges in these algorithms. Also, there is a possibility of happening errors due to manual similarity measurement.

■ In GraRep [21], a method introduced for learning node indicator vectors in the weighted graph. Unlike the previous methods, this one has used the global information of graph structure by applying logarithmic conversion log-transformed, and node transition probability matrices to calculate latent vector matrices. This matrix constructed with neighbors at different distances, then the resulting matrices are added together.

■ Another way to measure multi-step similarity is to calculate the overlap rate of a node's neighbors. This method is known as HOPE, and the score of the k-step similarity is calculated using the neighbor overlap rate. The Katz Index function and Adamic-Adar scores are applicable for the overlap calculation [22].

B. Random walk-based methods

Random walk-based methods first select one of the

node's neighbors randomly and then move toward that neighbor, and repeating this process to obtain the node sequence. Then the word2vec model is used to learn the nodes sequence embedding, which the local similarities and structural information can be maintained. The Node2vec and DeepWalk algorithms are two cases of Random walk-based methods algorithms. This method employs a direct neighborhood method or second neighborhood relations ultimately and not able to reflect all the structural and global information of the graph, so a complete representation will not be provided for all graph nodes. Inefficiency for sparse graphs is another disadvantage of this method [18].

■ Bryan Peruzzi and his colleagues proposed the DeepWalk algorithm graph embedding [23]. In this method, the random walking algorithm is executed firstly on the input graph and produces several series of node sequences; this is repeated for all graph nodes so that a set of consecutive sequences is obtained for each node. Then, the Skip-gram algorithm is executed, using the sequences. This model is used to learn random walking on the graph, and a vector is generated for each node. The resulting vectors are used as feature vectors and guide the classifier, and finally evaluates.

■ The Node2Walk algorithm is based on the Skip-gram algorithm and works similarly to DeepWalk with the difference that the Biased Random Walk algorithm has replaced with a simple Random Walk algorithm. This algorithm has a deviation parameter and behaves more flexibly to collect node information. This method has high scalability because it uses the first surface and first depth search and also uses the direct and second-degree neighborhood relations of the node. Therefore, it attains two local and global views of nodes and adjusts the search space by defining different parameters, and makes the node sampling operation more varied than previous algorithms [24].

C. Neural network-based methods

The main issue in the network embedding approach is learning a function to map network space to one space with a tinier size. Some methods, such as matrix factoring, assume mapping performance is linear. However, the process of network formation is complex and nonlinear, so a linear function may not be sufficient to map the main network in the embedded space [25]. Deep neural networks have been very successful in modeling complex nonlinear phenomena in various fields, such as speech recognition and computer vision. Therefore, the use of deep neural networks is an efficient solution in cases where complex information is available. However, in the field of network representation learning, a small number of users have used deep neural networks.

■ In 2015, a method was proposed that is mainly applicable for learning features in large-scale network embedding information graphs [26]. The Line operation algorithm is performed in two steps; primarily, the first-order and second-order proximities are calculated, and in the second step, minimizing the first and second step Closeness. The proximity of the first-order is calculated similarly to the graph factoring that keeps the proximity matrix and multiplies a point close to each other is their both goals, except that the graph factoring does so by minimizing the difference between the proximity matrix and the point multiplication, but This algorithm uses two common probability distributions for each pair of vertices, one uses the proximity matrix and the other uses node embedding. The difference between this algorithm and the Node2Walk and DeepWalk algorithm is in extracting sample nodes. Other methods of embedding the node based on the deep neural network consider the global neighbors of each node as the node input; so, for scattered large-scale sparse graph g, calculations are costly and Non-optimal.

■ The Convolution Algorithm solves this problem by defining a Convolution operator in the graph. This model collects the Neighborhoods embedding of a node and uses the embedding function and the previous embed to achieve the new embedment. Embedding aggregation with the help of a local neighbors causes beneficial effects in scalability and provides the description of neighboring neighbors for multiple iterations. In this method, embedding is achievable without supervision by setting up unique tags for each node. The filter creation approaches like spatial and spectral filters are completely different in such categories. Spatial filters work directly on the main graph and the adjacent matrix; While spectral filters work in the Laplacian Graph spectrum [27].

Proposed Method

In the present paper, a decoder-encoder is designed based on deep neural networks to recognize the information about the structure and the graph characteristics.

In this method, a powerful threshold presented to evaluate the loss rate of the encoder-decoder by combining local and global characteristics. Therefore, the efficiency of the link prediction algorithm has increased with the loss function improvement in the encoder-decoder.

Fig. 3 shows the steps of the proposed algorithm. The whole process consists of three main steps: 1- Feature extraction 2- loss function, 3- Optimization. Before introducing the proposed method.

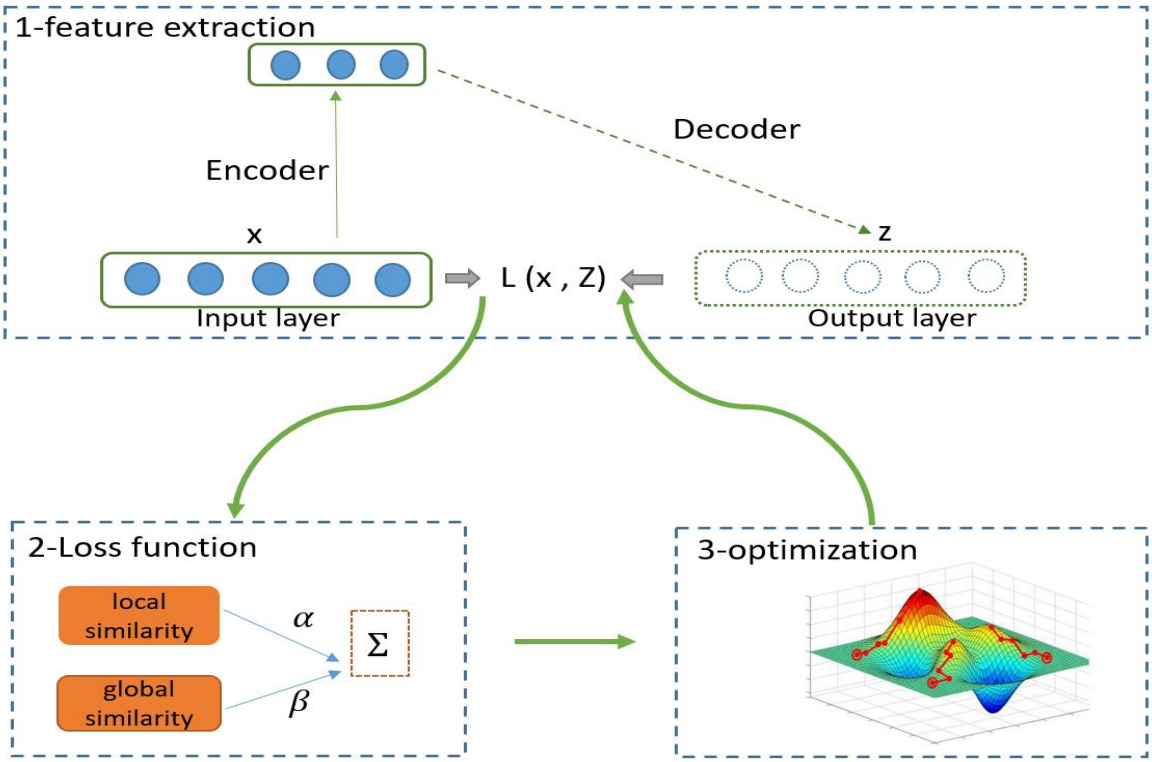

Fig. 3: The steps of performing the proposed method.

D. Feature extraction

Extracting the feature is the most important part of the proposed model, which is done by an encryption-decoder. Encryptions-decoders play an essential role in unsupervised learning and deep networks. The purpose of using encoders is to represent data in a way that to be used in classification. The best advantage of password-decoders is the automatic selection of features [28].

As can be seen in Fig. 4, the encoder is a neural network that receives a set of data without labels and encrypts them and tries to re-represent the inputs at the output so that they have the least possible difference with the input value. In encoding, the input data is mapped to the attribute space, and in decoding, space is converted from the attribute space back to its original state. The main part of an encryption-decoder is the intermediate hidden layer that is used as the extracted property for categorization.

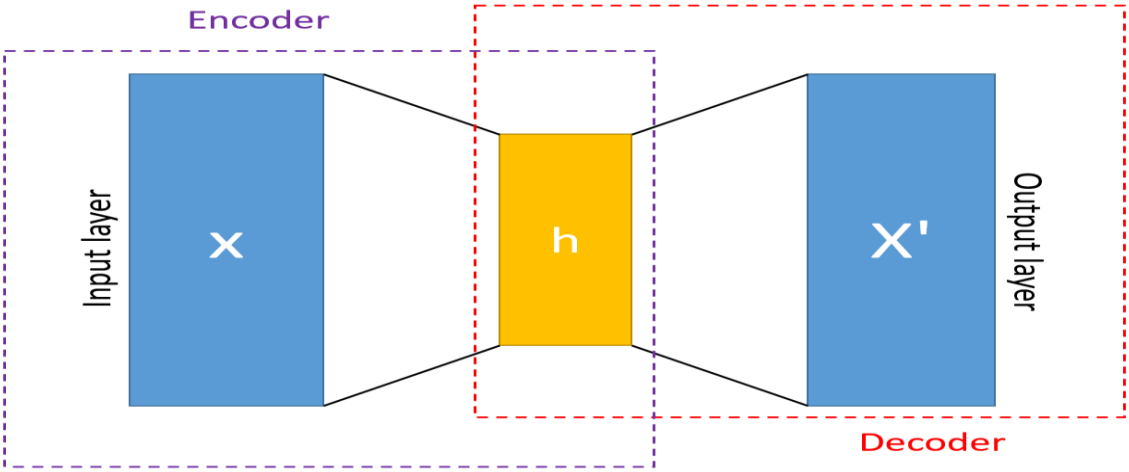

Fig. 4: General autoencoders view.

The encryption section is a feature extraction function that calculates the feature vector considering the inputs.

Therefore, if we display the feature vector with h, the encoder with f_θ and the data set with X_i, the (1) is established.

$$h^t = f_\theta(x^t). \qquad x^t = \{x^1. \ldots . x^T\} \tag{1}$$

The h vector is the calculated property of x. The decryption section is a function that displays it with $g_\theta$and according to the equation (2) mapping maps of the space characteristic of latent features or The latent space makes its way into the entrance space.

$$r = g_\theta(h) \tag{2}$$

Auto encoders attempt to minimize the reconstruction loss $L(x.r)$ between the original data and the reconstructed data. This is done by reconstructing r from x with pre-training and measuring the difference between x and r.

E. Loss Function

As we know, using global information in loss calculation leads to high accuracy, but it takes a lot of time to be calculated. On the other hand, actions based on local information are generally faster but provide less accuracy. Because the network type is large-scale, irregular, and heterogeneous real-world networks, both local and global structures are important [29]. In the proposed method, by combining local and global features, the accuracy of the loss function has improved.

i. local similarity

The proposed method considers the Integrated degree-related clustering similarity as a local index. Studies have shown that the combination of some structural features can lead to a strong threshold to show the nodes similarity level. Integrated degree-related clustering is one of the combinational thresholds on link prediction scope with high performance which is defined as below [30]:

$$DC_{ij} = \sum_{v_z \in \Gamma(v_i) \cap \Gamma(v_j)} dc(V_z) \tag{3}$$

$\Gamma(v_i) \cap \Gamma(v_j)$ indicates the number of common neighbors between the nodes v_i and v_j, and $dc(v_z)$represents the clustering related to the degree and is defined as the following equation :

$$dc = \frac{1}{N}\sum_{i=1}^{N} C(k_v)(k_v)^r \tag{4}$$

In (4) N indicates the number of nodes in the network. $C(k_v)$ represents the clustering coefficient of node v with a degree of k and r indicates the set coefficient of the network.

Therefore, in order to achieve local characteristics, the loss function is defined as (5).

People who share their connections on social media tend to form associations or clusters. The tendency of nodes to form clusters in a graph is called the clustering coefficient, which is the ratio of existing edges between neighbors, to the maximum possible edges between neighbors of a vertex. The network clustering mechanism plays a critical role in edge formation, but in most cases, the networks are incomplete due to data loss, so the clustering coefficient cannot be accurate enough. Hence, by applying the corrections, the Integrated degree-related clustering criterion obtained. Using the average clustering coefficient $\frac{1}{N}\sum_{i=1}^{N} C(k_v)$ instead of the clustering coefficient $C(k_v)$ increases the scalability of the Integrated degree-related clustering threshold. Besides, according to the preferential attachment mechanism, the probability of forming a new connection from another node to node i is proportional to the degree of node i; this means that neighbors with a higher degree may link with each other with higher possibility. Therefore, the mean degree of neighbor's node $(k_v)^r$ applied to merge the clustering coefficient into the degree related clustering threshold. Finally, the combination of neighbors mean degree and the two nodes common neighbors threshold $\sum_{v_z \in \Gamma(v_i) \cap \Gamma(v_j)} dc(V_z)$ has been used to increase the threshold accuracy. According to the improvements, using three indicators of node degree, common neighbors of the two nodes, and the average clustering coefficient results in realizing the clustering threshold related to the first degree as a fused criterion to calculate the similarity between two nodes.

$$L_{local} = \sum_{i=1}^{|v|}\sum_{j=1}^{|v|} DC_{ij}\left\|h_i^k - h_j^k\right\|_2^2 = \sum_{i=1}^{|v|}\sum_{j=1}^{|v|} DC_{ij}\left\|h_i - h_j\right\|_2^2 \tag{5}$$

As h_i indicates the $v_i$node feature vector and DC represents the local Similarity network, theL_{local} can also be displayed as follows:

$$L_{local} = \sum_{i=1}^{|v|}\sum_{j=1}^{|v|} DC_{ij}\left\|h_i - h_j\right\|_2^2 = Tr(H^T L_{DC} H) \tag{6}$$

In (6) $H \in R^{|v| \times d_i}$ indicates matrix network embedding representation. L is a loss function such as the Euclidean distance and Tr represents the trace of a matrix. Besides, $L_{DC} = D - DC_{ij}$ is the graph regularization matrix (Laplacian matrix) of the similarity matrix and $D = [d_{ij}] \in R^{|v| \times |v|}$ |is a diagonal matrix, thus $D_{i.i} = \sum_j DC_{ij}$is calculated.

ii. global similarity

In the proposed method, the Transitive Node Similarity Measure used to exploit the global feature [31]. Global methods, identify all path structures that are very difficult to be calculated for large social networks, while this model follows the shortest path between two nodes in the network, so it takes less time and complexity compared to global algorithms.

In the Transitive Node Similarity Measure, the length of the shortest path between the nodes and the nodes similarity in the neighborhood that make up that path are considered to calculate the similarity of the two

nodes in the network. The (7) and (8) shows the transfer node's similarity index method of calculation:

$$\mathrm{TNS_{ij}} = \begin{cases} 0. & \text{if there is no path between } \mathrm{v_i}.\mathrm{v_j} \\ \mathrm{sim}(\mathrm{v_i}.\mathrm{v_j}). & \text{if } \mathrm{v_i}.\mathrm{v_j} \text{ are nighborse} \\ \prod_{\mathrm{h=1}}^{\mathrm{k}} \mathrm{sim}(\mathrm{v_{p_h}}.\mathrm{v_{p_{h+1}}}). & \text{otherwise} \end{cases} \quad (7)$$

The global threshold between the two nodes is achievable through (7); in such a way that, if there is no path between the nodes i and j, the threshold value is zero.

If the two nodes i and j are also direct neighbors, the global threshold value is calculated through the (8) and (9). Finally, if there exists a path between two nodes i and j but they are not directly in the neighborhood, the nodes located in the path between i and j are determined primarily, then the similarity of the two neighboring nodes in the path is calculated using the (8). Finally, the global threshold has resulted from the product of the similarities between the neighboring nodes that construct the path.

$$Sim(v_i.v_j) = \begin{cases} 0. if (v_i.v_j) \notin \varepsilon \wedge (v_i.v_j) \notin \varepsilon \\ \frac{1}{\deg(v_i)+\deg(v_j)-1}. otherwise \end{cases} \quad (8)$$

The path between two nodes in the network affects the information about their connection. Also, the shorter path results in the greater probability of a link creation between the two nodes.

Therefore, the shortest path between two nodes is a good threshold for describing two nodes similarity. On the other hand, most pairs of nodes are separated by a small number of nodes in the network due to the theory of small world (both arbitrary persons on the planet are connected by 6 or fewer intermediaries).

For this reason, sometimes the shortest path between two nodes does not perform well. Therefore, the transitive node similarity threshold was used. This criterion calculates the similarity of the node $\frac{1}{\deg(v_i)+\deg(v_j)-1}$ in our shortest path between the nodes by considering the degree of the node $Sim(v_i.v_j)$, so it has higher accuracy. According to equation (8), if two nodes are neighbors, the sum of nodes degree is calculated and reversed, and if they are not, the similarity degree is zero. Therefore, in order to achieve the global characteristics, the loss function is defined as (9).

$$L_{global} = \sum_{i=1}^{|v|}\sum_{j=1}^{|v|} TNS_{ij}\left\|h_i^k - h_j^k\right\|_2^2 = \sum_{i=1}^{|v|}\sum_{j=1}^{|v|} TNS_{ij}\left\|h_i - h_j\right\|_2^2 \quad (9)$$

As h_i indicates the $v_i$node feature vector and TNS represents Transitive Node Similarity Measure, the L_{global} can also be displayed as follows:

$$L_{global} = \sum_{i=1}^{|v|}\sum_{j=1}^{|v|} TNS_{ij}\left\|h_i - h_j\right\|_2^2 = Tr(H^T L_{TNS} H) \quad (10)$$

In (10) $H \in R^{|v|\times d_i}$ indicates Adjacency matrix of embedded network. L is a loss function such as the Euclidean distance and Tr represents the trace of matrix(the elements positioned on matrices main diagonal).

Besides, $L_{DC} = D - TNS_{ij}$ is the graph regularization matrix (Laplacian matrix) of the similarity matrix and $D = [d_{ij}] \in R^{|v|\times|v|}$ |is a diagonal matrix, thus $D_{i.i} = \sum_j TNS_{ij}$ is calculated. Finally, both optimization goals are combined, and the overall optimization goal is defined as expressed in (11).

$$L_{mix} = (\alpha L_{local} + \beta L_{global}) \quad (11)$$

The α and β are hyper parameters that are responsible to control the balance between the two global similarity and local similarity thresholds. In fact, the α hyper parameter determines the effectiveness of the local criterion.

If α = 0, the predictive function is performed only through the global threshold. The β hyper parameter indicates the effect of the global standard effect on the prediction operation.

F. Optimization

After calculating the similarity between the two nodes, the loss function is optimized during a process to correct and update the neural network weights to achieve the minimum loss. Therefore, in this section, minimizing the L_{mix}function is the desire. The main step of calculating the partial derivative who's mathematically described in details, is shown in (12):

$$\frac{\partial L_{mix}}{\partial w^k} = \alpha\frac{\partial L_{local}}{\partial w^k} + \beta\frac{\partial L_{global}}{\partial w^k} \quad i = 1.2. \ldots .K \quad (12)$$

In (12), the K parameter indicates the number of layers. Also w^k describe the K - layer's weight.

$$\frac{\partial L_{local}}{\partial \theta^k} = \frac{\partial L_{local}}{\partial H^k}\cdot\frac{\partial H^k}{\partial \theta^k} = 2[(L + L^T)\cdot H^k]\cdot\frac{\partial H^k}{\partial \theta^k} \quad (13)$$

Equation (13) represents the partial derivative of L_{local} so that $\theta^k \in (w^k.b^k)$ is defined as follows. The b^kalso represents the K-layer bias. H represents the adjacency matrix of the embedded network, and each layer's H according to the values of weight, bias, and H of the previous layer with the help of the back-propagation neural network is calculated as $H^k = (H^{k-1}W^k + b^k)$. Also, the partial derivative of L_{local} is also calculated in (14).

$$\frac{\partial L_{global}}{\partial \theta^k} = \frac{\partial L_{global}}{\partial H^k} \cdot \frac{\partial H^k}{\partial \theta^k}$$
$$= 2[(L + L^T) \cdot H^k] \cdot \frac{\partial H^k}{\partial \theta^k} \quad (14)$$

Evaluation

In evaluation part, 4 data sets have been tested using our proposed method to verify its validity. The result of the experiments has been compared with Laplacian, Node2vec, and GAE methods. Laplacian Method [32] is a non-linear dimensionality reduction algorithm, introduced based on spectral techniques and manifold learning.

Manifold learning is a powerful tool for reducing nonlinear dimension. The inherent parameters of the system, which are the main factor in distinguishing data from each other, are identified using this tool, and the entire set is placed on a manifold that represents the actual relationship of the parameters. In this way, the relationship between data is expressed in a space with a low-dimensional.

Node2vec [24] is a more advanced version of Deep Walk. The DeepWalk algorithm has limitations and cannot control the path. Instead of walking randomly, this algorithm searches for Breadth-first Sampling (BFS) and Depth-first Sampling (DFS). Adds to the description of the network structure in random paths.

GAE Method [33] is based on the Convolutional Neural Networks, it also uses a cryptographic and decoder to make nodes embedded. Its satisfactory results in reducing the dimensional reduction indicate the success of the convolutional neural network for obtaining graphical structural information.

A. Data Set

In this study, the proposed method was tested on 4 data sets. The general characteristics of this data set are summarized in Table 2.

Blog catalog [34]: A social network with 10312 bloggers and 333983 social relationships. Each node is represented by a blogger, and each edge indicates a relationship between two bloggers. The network has 39 different tags and shows the bloggers' interest in different topics. A blogger may have different tags.

Wikipedia Data Collection [35]: A common network of words. This network has 4,777 nodes, 184,812 edges and 40 different tags.

Cora Data Collection [36]: A subset of the entire citation data set. It consists of 7 sub-categories with 2708 scientific articles on machine learning and 5429 citation links between them.

Drug-drug interaction [37]: A comprehensive and accessible online database that contains accurate information about drugs and drug targets. This data set consists of 2191 drugs and includes 242027 drug-to-drug interactions.

Table 2: Specifications of the data set used in the experiment

Data collection name	Number of edges	Number of nodes
Blog catalog	333983	10312
Wikipedia	12765	2405
Cora	5278	2708
Drug-drug interaction	242027	2191

B. Performance evaluation

In order to evaluate the proposed method, the performance accuracy rate threshold and Fmeasure measurement rate and the area below the operational curve of Area under curve (AUC) receiver, have been used.

The Accuracy indicates the number of correctly categorized samples in relational form equation (15):

$$\text{Accuracy} = \frac{TP+TN}{TP+FP+FN+TN} \quad (15)$$

The Fmeasure Measurement Rate, which is designed to establish a balanced relationship between Precision validity and recall, is defined according to equation (16):

$$\text{Fmeasure} = 2\left(\frac{Precision \cdot Recall}{Precision+Recall}\right) \quad (16)$$

TP and TF are examples that have been correctly identified by the model during the evaluation phase; TP represents the interaction patterns and TF represents the non-interaction patterns.

FNs are non-interactive pairs that are mistakenly known as interactions, and FPs are data that are incorrectly known as non-interactions. The AUC threshold indicates the desperation of positive and negative values. A high value means that the model separates the positive and negative values of the negative sample well, and the low value means that the model has randomly worked.

C. Experimental tests

The proposed method is applied to Cora, Wikipedia, Blog catalog, Drug-drug interaction separately and its results are compared with Laplacian, Node2vec and GAE methods. The relevant tables show the threshold performance, ACC accuracy rate, F1 measurement rate, and AUC operational sub-area . Also, in order to make the specific assessment possible, the best results are displayed in bold. The results of applying the proposed method on the Cora data set are shown in Table 2.

As obviously shown Table 3, the ACC and AUC threshold values are higher than the other three proposed methods, while the F1 GAE method is higher than the other methods.

Table 3: Cora data evaluation results

Type	Method	F1	ACC	AUC
Based on matrix factoring	Laplacian	0.589	0.588	0.621
Random walk-based	Node2vec	0.555	0.557	0.584
Neural network	GAE	**0.611**	0.568	0.606
Neural network	Proposed method	0.562	**0.620**	**0.645**

Table 4 shows the evaluation results on the Wikipedia data set. The accuracy of the proposed method on the Wikipedia data set has increased by about 7% compared to the best method, the Node2vec method, and the highest values of the two F1 and AUC thresholds on this dataset belong to the proposed method.

Table 4: Wikipedia data evaluation results

Type	Method	F1	ACC	AUC
Based on matrix factoring	Laplacian	0.785	0.790	0.664
Random walk-based	Node2vec	0.857	0.860	0.932
Neural network	GAE	0.779	0.744	0.816
Neural network	Proposed method	**0.875**	**0.875**	**0.943**

The evaluation of the proposed method is reported on the Blog catalog data set according to Table 5. As can be seen, the results reported on the Blog catalog data collection shows an improvement in the performance of the proposed method compared to the other three methods, and as can be seen, all three performance criteria have increased significantly.

Table 5: Blog catalog data evaluation results

Type	Method	F1	ACC	AUC
Based on matrix factoring	Laplacian	0.785	0.790	0.864
Random walk-based	Node2vec	0.857	0.860	0.932
Neural network	GAE	0.779	0.744	0.816
Neural network	Proposed method	**0.875**	**0.875**	**0.943**

The fourth experimental dataset is Drug-drug interaction, the results of which are given in Table 6. The values in Table 6 show an increase in all three performance measurement criteria. The proposed method has been able to increase the accuracy rate by about 6% compared to the best method on the Drug-drug interaction dataset.

Table 6: Drug-drug interaction data evaluation results

Type	Method	F1	ACC	AUC
Based on matrix factoring	Laplacian	0.727	0.718	0.797
Random walk-based	Node2vec	0.814	0.814	0.898
Neural network	GAE	0.784	0.740	0.835
Neural network	Proposed method	**0.847**	**0.845**	**0.923**

Results and Discussion

In this section, we further examine the superiority of the proposed method towards the other baselines on experimental networks. From the differences among four algorithms summarized in Table 7, we can see that the proposed method has used all three techniques of local similarity, global similarity, and deep neural network to describe the nodes similarity. Therefore, it presents better performance than other compared algorithms.

Table 7: A summary of the differences among four algorithms

Type	Laplacian	Node2vec	GAE	Proposed method
Local similarity	✓	✓		✓
global similarity		✓	✓	✓
Deep neural network			✓	✓

■ Local similarities are using a small part of the network, so they have high speed and scalability. In the proposed method, the degree-related clustering used as a local threshold, which is a compound criterion of several structural features and able to improve the low accuracy weakness that exists in the local criteria.

■ Global similarities exploit the entire network structure, thus provides a more comprehensive and accurate description of network nodes. The similarity index of the transfer node, used as the global similarity

in the proposed method, which is calculated based on the shortest path between the two nodes. So this threshold could improve the weakness of the high computational complexity in the global similarity.

■ The depthless or superficial embedding methods often have a linear function for mapping the main network in the embedding functional space and have limitations. The proposed method uses an encoder-decoder, so it uses neural networks for data representation. Generally, deep neural networks are fitting in modeling complex nonlinear phenomena.

Also, the implementation results of the proposed method on Drug-drug interaction, Blogcatalog, Cora, and Wikipedia datasets indicate better performance on more solid or complete datasets. The highest accuracy resulted in the Blogcatalog dataset, and the lowest accuracy belonged to the Cora dataset.

Conclusion

A dataset contains tens to hundreds of features. However, not all features are meaningful for predictive linking algorithms. To this end, this paper presents a method of embedding a node based on a deep learning model to automatically extract useful information about the structure and characteristics of the graph. So far, similar solutions have been proposed, but most of them use only direct neighbors and second-class neighbors as related nodes. In the real world, however, networks are large-scale, irregular, and heterogeneous, so both the local structure and their global structure are important, as is the case with the proposed method. The proposed method could successfully provide a strong threshold for evaluating the similarity of nodes, by coupling local and global network characteristics that resulted in the accuracy improvement of the algorithm. The combination of global and local similarity thresholds makes the proposed algorithm applicable to a large dataset. Also, choosing the right global standard has made it possible for the algorithm to remain acceptable while increasing the accuracy, speed, and complexity, and ultimately preventing the loss of important information due to the use of a deep neural network approach.

Author Contributions

This paper is the result of F. Mirmousavi's MSc thesis supervised by S. kianian.

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Conflict of Interest

There is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

Abbreviations

$\boldsymbol{x^t}$	the input data
$\boldsymbol{h^t}$	reconstructed data
$\boldsymbol{K}$	number of layers
$\boldsymbol{w^k}$	the k-th layer weight matrix
$\boldsymbol{\theta^k}$	the overall parameter
$\boldsymbol{b^k}$	the k-th layer biases
$\boldsymbol{L_{local}}$	local loss function
$\boldsymbol{DC_{ij}}$	Integrated degree-related clustering
$\boldsymbol{dc}$	clustering related to the degree
N	number of vertexes
$\boldsymbol{C(k_v)}$	clustering coefficient of node v with a degree of k
$\boldsymbol{k_v}$	degree of node v's
$\boldsymbol{r}$	assortative coefficient
$\boldsymbol{Tr}$	represents the trace of a matrix
$\boldsymbol{L_{DC}}$	Laplacian matrix DC
D	diagonal matrix
$\boldsymbol{L_{global}}$	global loss function
$\boldsymbol{TNS}$	Transitive Node Similarity
$\boldsymbol{deg(v_i)}$	degree of node v's
$\boldsymbol{H}$	network embedding representation matrix
$\boldsymbol{\alpha}$	tradeoff factors among the objective functionL_{local}
$\boldsymbol{\beta}$	tradeoff factors among the objective L_{global}
ACC	accuracy rate
$F1$	Assessment rate
AUC	operational sub-are.

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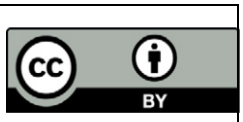

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Research paper

Bidirectional Buck-Boost Integrated Converter for Plug-in Hybrid Electric Vehicles

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Abstract

Background and Objectives: Power electronics infrastructures play an important role in charging different types of electric vehicles (EVs) especially Plug-in Hybrid EVs (PHEVs). Designing appropriate power converters is the topic of various studies.

Method: In this paper, a novel bidirectional buck-boost multifunctional integrated converter is presented which is capable of handling battery and fuel cell stack in plug-in hybrid electric vehicles. The proposed converter has the ability to work in five different operating modes (Charging/Propulsion (only battery)/ Propulsion (battery and FC)/ Regenerative braking/ V2G). The introduced multifunctional two-stage converter has the ability to work in all the above-mentioned modes in buck- boost condition, the feature that does not exist in the previous works. It is possible to control active and reactive power by using the effective dual-loop PI control method which is introduced in this paper. Working as an on-board charger and DC-DC converter (which interfaced between power sources and motor drive system) causes a decrease in the counts of the total components and an increase in system efficiency.

Results: Operation principle and steady-state analysis of each stage of the proposed converter in all operating modes are provided in detail and in order to design an appropriate applicable converter, the design considerations and procedure are also explained for capacitive and inductive components. The proposed converter is simulated in MATLAB/SIMULAIN environment and results are provided. Voltage and current waveforms in all operating conditions are provided with their transient. FFT analysis of the input current (in the operating modes in which the converter absorb or deliver power from/to the grid) is also mentioned. A reduced-scale setup of the presented converter is built and tested and experimental results confirm simulation ones.

Conclusion: A bidirectional buck-boost integrated converter in PHEVs applications is introduced in this paper. The design procedure of the presented converter is provided and also an effective control method to control active and reactive power during charging and V2G modes is introduced. A comparison study of the proposed converter with other similar converters introduced in recent years in terms of the number of high-frequency switches in each mode is also done. Simulation and experimental results are also provided.

Introduction

Different attempts to find practical solutions for increasing environmental problems during recent years have caused significant developments in different types

of electric vehicles [1], [2].

Fully electric vehicles (EVs) or plug-in EVs (PEVs) and hybrid electric vehicles (HEVs) or plug-in hybrid EVs (PHEVs) are the main categories of non-fossil fuels vehicles. There are some limitations in using the PEVs, which receive their energy entirely from the electricity grid because of their battery pack, which is used to store needed energy such as performance degradation because of high current dischargers and low life [3], [4]. Hybridization of EVs' powertrain, which leads to the plug-in hybrid electric vehicles (PHEVs), is a beneficial solution for battery pack challenges that usually is done by adding fuel cell stack to the power train. Additionally, PHEVs do not have disadvantages of the fuel cell vehicles (FCVs), which receive their needed power entirely from FC stacks, such as slow transient response and degradation effects. Multi-source powertrains need special DC-DC converters, which are interfaced between the power sources and motor drive system [5]-[7]. Working in battery charging, regenerative braking, and propulsion (battery discharging) operating modes intensifies the need for a bidirectional converter on the battery side. On the other hand, using charge equalizer circuits (CECs) causes the battery port voltage to change over a wide range by bypassing and adding battery cells according to their state of charge (SOC). In addition, the induced voltage of the motor changes in a wide range during regenerative braking, depending on the car speed. So the bidirectional DC-DC converter adopted on the battery side should be able to work as a buck-boost converter in both directions.

In addition to the above-mentioned DC-DC converter, an AC-DC converter is also required in charging (charging the battery with the AC grid voltage) and discharging (V2G) modes. Exploiting an appropriate bidirectional buck-boost converter enables the PHEV to be charged and discharged by universal voltage supply (90-260V [8], [9]) and improves the input current waveform by making it feasible to select the DC-link voltage of the AC-DC converter in a wide range.

In conventional powertrains, two separated converters are utilized for charging and propulsion modes. This fact increases the entire system losses and decreases system reliability. A very effective way to improve system reliability and efficiency is to merge these converters. This integration enables the designer to utilize different components, especially semiconductor devices and passive components, in more than one operating mode, so the components' count can be reduced. This integrated converter should have all the features mentioned above in addition to the ability to manage the used energy of each power source.

In [10], a bidirectional DC-DC converter is proposed, which can be used in PEVs as the converter interfaced between the energy storage system (ESS) and the motor drive system. Although it has high voltage ratio and low voltage stress on semiconductor devices, it cannot work as a buck-boost converter in both directions and also needs extra circuits for charging the battery and handling other power sources. In [11], a bidirectional DC-DC converter with a wide voltage gain ratio is presented. In addition to its disability to increase and decrease voltage level in both directions, one converter is needed for each power source in PHEVs, so the entire system efficiency and reliability can be decreased because of the components numbers. The DC-DC converters proposed in [12], [13] are capable of handling more than one power source in PHEVs. The converter introduced in [12] cannot work in regenerative braking mode and is able to work only as a boost converter. Although the converter considered in [13] has the ability to return the regenerative braking energy to the battery, it cannot act as a buck-boost converter in different modes. Authors in [14], [15] have proposed two multi-port bidirectional DC-DC converters that are suitable for hybrid powertrains and work in different operating modes, which is an outstanding feature, but an extra charger circuit is needed to charge the battery by the grid. The integrated converters proposed in [16], [17] can work in charging and propulsion modes. Although the converter proposed in [16] can increase/decrease the voltage in propulsion and regenerative braking modes, it is not suitable for PHEVs, which have more than one power source and cannot work in V2G mode. The converter presented in [17] is an efficient reduced-part integrated converter that can used in the BEVs. The main drawback of the proposed converter is that it can only work in the charging mode when the battery voltage is higher than the peak of the grid voltage. Additionally, it is not suitable for PHEVs and cannot work in V2G mode. The integrated charger introduced in [18] is applicable in PEVs with one power source and can work in the buck-boost condition in charging mode only. A very high performance integrated converter is considered in [19], which can work in charging, propulsion, and regenerative braking modes, but it is not suitable for PHEVs. The switching bidirectional buck-boost converter presented in [20] is suitable for the Li-battery/super-capacitor hybrid ESS of EVs, which can only work in charging and V2G modes and needs extra circuits for handling propulsion and regenerative braking modes.

Introducing an appropriate integrated converter suitable for PHEVs, which is capable of doing all the aforementioned tasks (battery charging by grid, hybrid propulsion, regenerative braking, and vehicle to grid) in the buck-boost condition (in all operating modes), the feature that is not exist in the reviewed converters, is the motivation of this work.

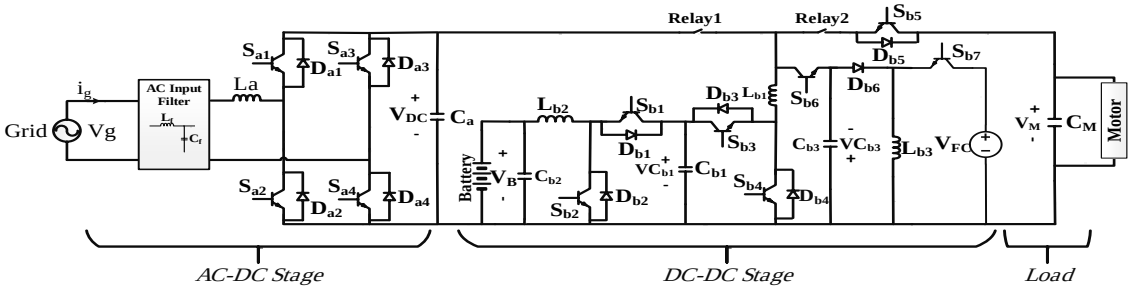


Fig. 1: Topology of proposed converter.

In this paper a bidirectional buck-boost integrated converter is presented which is capable of handling battery and FC stack in PHEVs. The presented converter has the ability to work in five operating modes and paly the roles of an on-board bidirectional buck-boost charger and a bidirectional DC-DC converter, which interfaced between power sources and motor drive system, without any need for additional power circuit. An effective control method is also explained which enables the proposed converter to control active and reactive power during charging and V2G modes and improves input current waveform in terms of total harmonic distortion (THD).

Proposed Converter; System Description and Analysis

Topology and Modes of Operation

Fig. 1 shows the topology of the proposed converter, where V_g, V_B, V_{FC}, and V_M represent the grid voltage, battery port voltage, fuel cell stack output voltage, and DC-link of motor drive system voltage, respectively. The presented converter structure can be divided into two stages. First stage: a bidirectional AC-DC converter which can work as a controllable rectifier and inerter in each direction. Second stage: a four-port DC-DC converter which can be controlled according to the converter operating mode. As shown in

Fig. 2, the proposed converter has the ability to work in five different operating modes:

1- Mode1 (Battery charging from the grid): in this mode the battery of PHEV is charged by the grid with controllable active and reactive power and pure sinusoidal input current waveform. The ability to increase and decrease the voltage on the battery side enables the proposed converter to be used in the PHEVs with wide range of battery voltage and be charged with universal voltage supply.

2- Mode2 (Propulsion; Only Battery): when the EV starts accelerating or when FC stack is not able to work because of the slow dynamic response of FC stack or its efficiency problems, the PHEV can receive its needed power from the battery by working the proposed converter in the second mode.

3- Mode3 (Propulsion; FC and Battery): when the converter is operated in this mode, both battery and FC provide the needed power. The capability of working in buck-boost condition enables the central control unit to manage energy of each power source better.

4- Mode4 (Regenerative braking): during EV braking condition, the energy of regenerative braking can be returned and stored in the battery. During different braking conditions with different speeds and different induced voltage levels, the returning energy process can be done properly because of the buck-boost structure of the proposed converter.

5- Mode5 (Vehicle-to-Grid (V2G)): the ability to work in this mode enables the PHEVs to handle V2G mode and return their surplus energy to the grid with controllable active and reactive power according to the commands of the smart grid or costumer.

As mentioned above, the proposed converter operates in five operating modes depending on the vehicle and power sources' conditions. As long as the vehicle is parked and connected to the grid the relay1 is ON and relay2 is OFF and converter works in charging and V2G modes (Mode1 and Mode5). When the vehicle is disconnected from the grid and is used by driver the relay1 is turned OFF and relay2 is turned ON and converter is allowed to work in propulsion and regenerative braking modes.

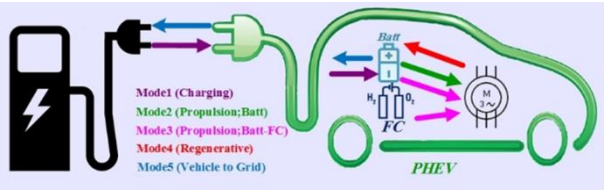


Fig. 2: Operating modes of proposed converter.

Operation Principle and Steady State Analysis

A. Mode1: Charging battery by grid

In this operating mode, the battery of the connected PHEV is charged by utility grid. Because of the ability of

converter to work as buck-boost converter in this mode, various battery packs with wide range of voltage can be charged by a wide range of utility grid. Additionally the controlling active and reactive power and input current waveform can be done better. The first stage rectifies and boosts the grid voltage and charges the DC-link capacitor (C_a). Then the DC-DC stage regulates the voltage level and charges the battery.

➢ **AC-DC Stage**

The first stage should control active and reactive power and input current waveform which can be done by the different control methods and switching patterns. In this paper a high efficiency and low conducting loss switching method explained in [21] and the effective control method introduced in "Control Method" section are adopted for the AC-DC stage. The proposed switching method controls the switches Sa1 and Sa2 depending on the sign of the grid voltage. It is worth mentioning that the switches Sa3 and Sa4 are OFF in this mode.

Vg>0: when the grid voltage is in its positive half-cycle, the Sa2 has high frequency operation and Sa1 is OFF.

State1 (0<t<DTs): as shown in Fig. 3 (a), in this state Sa2 is ON and L_a is magnetized via utility grid (V_g).

State2 (DTs<t<Ts): at t=DTs Sa2 is turned OFF and L_a is demagnetized with (V_g-V_{DC}) so C_a is charged [Fig. 3(b)].

Vg<0: in this condition Sa1 has high frequency operation.

State1 (0<t<DTs): in this state Sa1 is ON and L_a is magnetized via utility grid [Fig. 3(c)].

State2 (DTs<t<Ts): in this state Sa1 is in OFF-state and L_a is demagnetized so C_a is charged [Fig. 3(d)].

In order to calculate the voltage gain of the AC-DC stage the operation of this stage in the positive half-cycle of grid voltage should be analyzed. As shown in Fig. 3(a), the voltage of the L_a in the first state is obtained as:

$$\begin{cases} V_{La} = V_g & 0 < t < DT_s \\ V_{La} = V_g - V_{DC} & DT_s < t < T_s \end{cases} \quad (1)$$

The volt-sec balance of this inductor can be written as:

$$\langle i_{La} \rangle = 0 \rightarrow \frac{1}{T_s}\left[\int_0^{DTs}(V_g)dt + \int_{DTs}^{Ts}(V_g - V_{DC})\,dt\right] = 0 \quad (2)$$

By solving above equation the voltage gain of boost rectifier can be achieved as (3):

$$\frac{V_{DC}}{V_g} = \frac{1}{1-D} \quad (3)$$

➢ **DC-DC Stage**

In this mode the DC-DC stage charges the battery by controlling Sb1 and Sb4. The operation of this stage is divided into two states in this mode.

State1 (0<t<DTs): in this time interval Sb1 and Sb4 are ON so L_{b1} and L_{b2} are magnetized by (V_{DC}) and (V_{Cb1}-V_B), respectively. The energy of capacitor C_{b1} is released to L_{b2} so C_{b1} is discharged [Fig. 4(a)].

State2 (DTs<t<Ts): at t=DTs the both Sb1 and Sb4 are turned OFF so anti-parallel diodes D_{b2} and D_{b3} are forward-biased. As a result L_{b1} and L_{b2} are demagnetized by (V_{DC}-V_{Cb1}) and (-V_B), respectively. C_{b1} is charged in this state [Fig. 4 (b)].

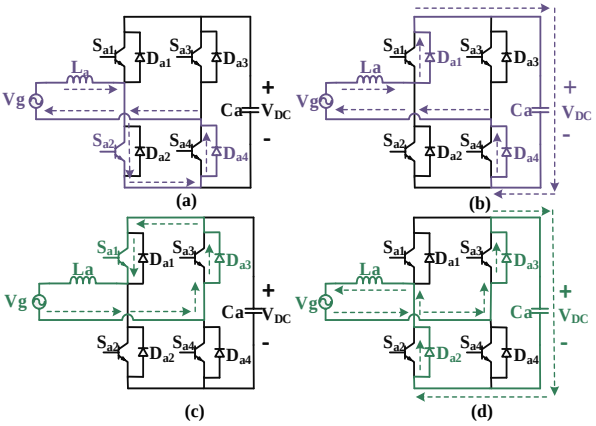


Fig. 3: Current paths of AC-DC stage in mode1.

As mentioned above, voltage across Lb1 and Lb2 are: For 0<t<DTs:

$$\begin{cases} V_{Lb1} = V_{DC} \\ V_{Lb2} = V_{Cb1} - V_B \end{cases} \quad (4)$$

and for DTs<t<Ts:

$$\begin{cases} V_{Lb1} = V_{DC} - V_{Cb1} \\ V_{Lb2} = -V_B \end{cases} \quad (5)$$

So the volt-sec principle for each inductor can be written as:

$$\langle i_{Lb1} \rangle = 0 \rightarrow \frac{1}{T_s}\left[\int_0^{DTs}(V_{DC})dt + \int_{DTs}^{Ts}(V_{DC} - V_{Cb1})\,dt\right] = 0 \quad (6)$$

$$\langle i_{Lb2} \rangle = 0 \rightarrow \frac{1}{T_s}\left[\int_0^{DTs}(V_{Cb1} - V_B)dt + \int_{DTs}^{Ts}(-V_B)\,dt\right] = 0 \quad (7)$$

By solving above equations, the volt-sec balance can be rewritten as:

$$D(V_{DC}) + (1-D)(V_{DC} - V_{Cb1}) = 0 \quad (8)$$

$$D(V_{Cb1} - V_B) + (1-D)(-V_B) = 0 \quad (9)$$

By manipulating (8), the voltage of Cb1 can be found as yields:

$$V_{Cb1} = \frac{1}{1-D}V_{DC} \quad (10)$$

Substituting (10) into (9) leads to obtaining the ideal voltage gain of mode1 as:

$$\frac{V_B}{V_{DC}} = \frac{D}{1-D} \tag{11}$$

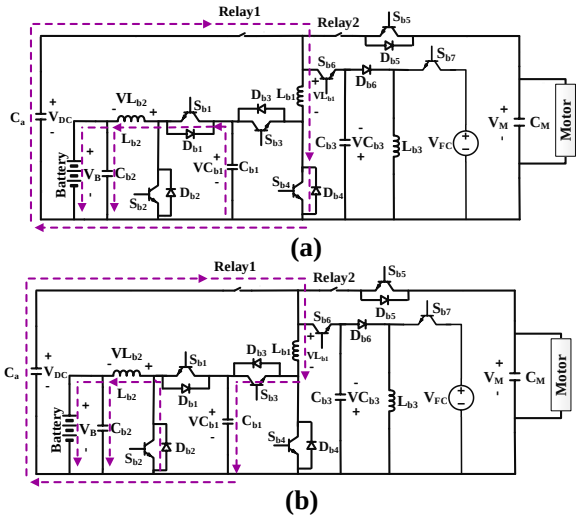


Fig. 4: Current paths of DC-DC stage in mode1.

B. Mode2: Propulsion (Battery)

In this operating mode the battery is supplying the energy to the motor drive system so the first stage does not have any task in this mode. For this purpose the relay1 is OFF and relay2 is in ON-state. The DC-DC stage operates as follows:

State1 (0<t<DTs): at first Sb2 and Sb3 are turned ON, simultaneously, so anti-parallel diodes D_{b1} and D_{b4} are reverse biased. As a result, L_{b1} and L_{b2} are magnetized with (V_{Cb1}-V_M) and V_B, respectively [Fig. 5 (a)].

State2 (DTs<t<Ts): in this state all switches of DC-DC stage are turned OFF so anti-parallel diodes Db1 and Db2 are forward-biased. In this condition L_{b1} and L_{b2} are demagnetized with (-V_M) and (V_B-V_{Cb1}), respectively [Fig. 5 (b)].

As shown in Fig. 5, the voltage across inductors L_{b1} and L_{b2} can be written as:

For 0<t<DTs:

$$\begin{cases} V_{Lb1} = V_{Cb1} - V_M \\ V_{Lb2} = V_B \end{cases} \tag{12}$$

and for DTs<t<Ts:

$$\begin{cases} V_{Lb1} = -V_M \\ V_{Lb2} = V_B - V_{Cb1} \end{cases} \tag{13}$$

So the zero average inductors voltages over one switching cycle are:

$$\langle i_{Lb1} \rangle = 0 \rightarrow \frac{1}{T_s}\left[\int_0^{DTs} (V_{Cb1} - V_M)dt + \int_{DTs}^{Ts} (-V_M)\,dt\right] = 0 \tag{14}$$

$$\langle i_{Lb2} \rangle = 0 \rightarrow \frac{1}{T_s}\left[\int_0^{DTs} (V_B)dt + \int_{DTs}^{Ts} (V_B - V_{Cb1})\,dt\right] = 0 \tag{15}$$

Solving above equations leads to:

$$D(V_{Cb1} - V_M) + (1-D)(-V_M) = 0 \tag{16}$$

$$D(V_B) + (1-D)(V_B - V_{Cb1}) = 0 \tag{17}$$

From (16) the voltage of C_{b1} can be obtained as:

$$V_{Cb1} = DV_M \tag{18}$$

By substituting (18) into (17), the ideal voltage gain of mode2 is obtained as:

$$\frac{V_M}{V_B} = \frac{D}{1-D} \tag{19}$$

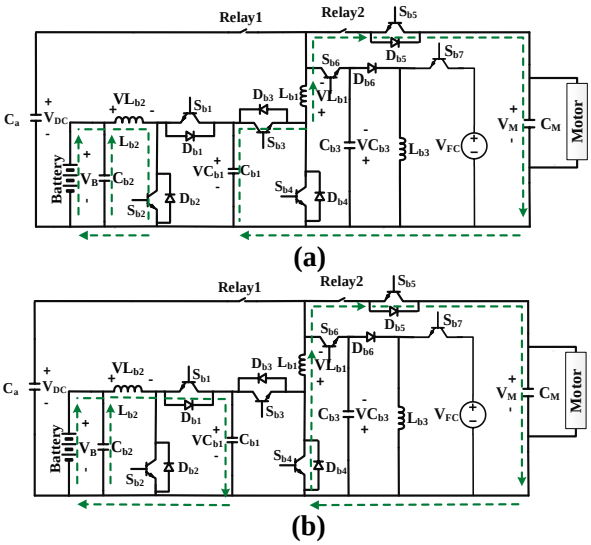


Fig. 5: Current paths of DC-DC stage in mode2.

C. Mode3: Propulsion (Battery + Fuel cell)

When the fuel cell stack has the ability to participate in providing needed energy, the central control system sends Sb6 and Sb7 gate signals and converter delivers the energy of the battery and fuel cell to the motor drive system, simultaneously. Fig. 6 shows the operation principle of the converter in this mode. Because of the converter ability to regulate battery voltage in wide range, the battery cells with less SOCs can be bypassed in order to equalize discharging process.

State1 (0<t<DTs): this state begins when the Sb6 and Sb7 receive gate signals. In this state Sb2, Sb3, Sb6 and Sb7 are turned ON. The Db5 is reverse biased so L_{b1} is magnetized by C_{b1} and C_{b3} which are charged in the previous time interval. L_{b2} and L_{b3} are also magnetized by (V_B) and (V_{FC}), respectively [Fig. 6 (a)].

State2 (DTs<t<Ts): during this state, all switches of the DC-DC stage are turned OFF so diodes D_{b1}, D_{b4}, D_{b5}, and D_{b6} are forward-biased. In this condition L_{b1} and L_{b2} are demagnetized by (-V_M) and (V_B-V_{Cb1}), respectively. The C_{b3} starts charging through L_{b3} which is magnetized in previous state [Fig. 6 (b)].

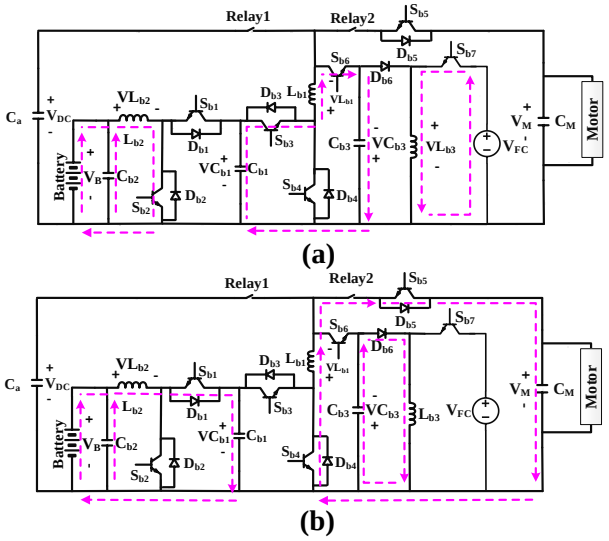


Fig. 6: Current paths of DC-DC stage in mode3.

By using KVL, the voltage across inductors in each state are obtained as:

For 0<t<DTs:

$$\begin{cases} V_{Lb1} = V_{Cb1} + V_{Cb3} \\ V_{Lb2} = V_B \\ V_{Lb3} = V_{FC} \end{cases} \quad (20)$$

and for DTs<t<Ts:

$$\begin{cases} V_{Lb1} = -V_M \\ V_{Lb2} = V_B - V_{Cb1} \\ V_{Lb3} = -V_{Cb3} \end{cases} \quad (21)$$

The volt-sec balance can be written as:

$$\langle i_{Lb1} \rangle = 0 \rightarrow \frac{1}{T_s}\left[\int_0^{DTs} (V_{Cb1} + V_{Cb3})dt + \int_{DTs}^{Ts} (-V_M)\,dt\right] = 0 \quad (22)$$

$$\langle i_{Lb2} \rangle = 0 \rightarrow \frac{1}{T_s}\left[\int_0^{DTs} (V_B)dt + \int_{DTs}^{Ts} (V_B - V_{Cb1})\,dt\right] = 0 \quad (23)$$

$$\langle i_{Lb3} \rangle = 0 \rightarrow \frac{1}{T_s}\left[\int_0^{DTs} (V_{FC})dt + \int_{DTs}^{Ts} (-V_{Cb3})\,dt\right] = 0 \quad (24)$$

Solving above equations leads to:

$$D(V_{Cb1} + V_{Cb3}) + (1-D)(-V_M) = 0 \quad (25)$$

$$D(V_B) + (1-D)(V_B - V_{Cb1}) = 0 \quad (26)$$

$$D(V_{FC}) + (1-D)(-V_{Cb3}) = 0 \quad (27)$$

From (26) the voltage of C_{b1} can be obtained as:

$$V_{Cb1} = \frac{1}{1-D} V_B \quad (28)$$

and From (27) the voltage of Cb3 can be obtained as:

$$V_{Cb3} = \frac{D}{1-D} V_{FC} \quad (29)$$

By substituting (28) and (29) into (25) the voltage of motor drive system can be calculated as:

$$V_M = \frac{D^2}{(1-D)^2} V_{FC} + \frac{D}{(1-D)^2} V_B \quad (30)$$

D. *Mode4: Regenerative Braking*

As soon as the vehicle brakes, the switch Sb5 is turned ON and Sb6 and Sb7 are turned OFF so the energy flows from motor drive system to the battery. Due to the buck-boost structure of the converter, the energy returning process can be done properly with a wide variation of the vehicle speed.

State1 (0<t<DTs): during this state Sb1, Sb4, and Sb5 are in ON-state so L_{b1} and L_{b2} are magnetized by (V_M) and ($V_{Cb1} - V_B$), respectively [Fig. 8(a)].

State2 (DTs<t<Ts): in this time interval all switches are turned OFF except Sb5 so Db2 and Db3 are direct biased. In this condition L_{b1} and L_{b2} are demagnetized by (V_M-V_{Cb1}) and ($-V_B$), respectively, and C_{b1} starts charging [Fig. 8(b)].

The same approach as the mode1 can be used for calculating voltage gain of mode4. The volt-sec principle can be written as:

$$\langle i_{Lb1} \rangle = 0 \rightarrow \frac{1}{T_s}\left[\int_0^{DTs} (V_M)dt + \int_{DTs}^{Ts} (V_M - V_{Cb1})\,dt\right] = 0 \quad (31)$$

$$\langle i_{Lb2} \rangle = 0 \rightarrow \frac{1}{T_s}\left[\int_0^{DTs} (V_{Cb1} - V_B)dt + \int_{DTs}^{Ts} (-V_B)\,dt\right] = 0 \quad (32)$$

By solving above equations, similar to mode1, the voltage gain of mode4 is obtain as:

$$\frac{V_B}{V_M} = \frac{D}{1-D} \quad (33)$$

E. *Mode 5: Vehicle to Grid*

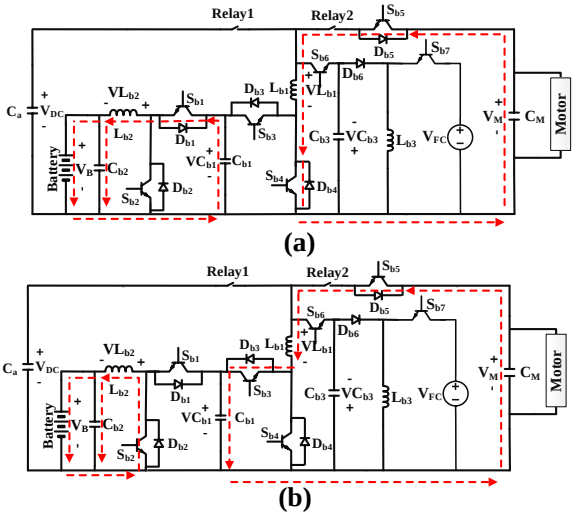


Fig. 7: Current paths of DC-DC stage in mode4.

It is possible to return surplus EV energy to grid for different reasons by operating the proposed converter in the mode5. Peak shaving is a very important task which can be done by using electric vehicles as mobile power sources. The proposed converter can return parked EV's energy to utility grid by controllable active and reactive power according to the processed commands of smart grid or customer. At first the DC-DC stage increase or decrease the voltage of battery according to the DC-link voltage reference and then the AC-DC stage works as single-phase full-bridge inverter and delivers the energy of DC-link capacitor to the grid.

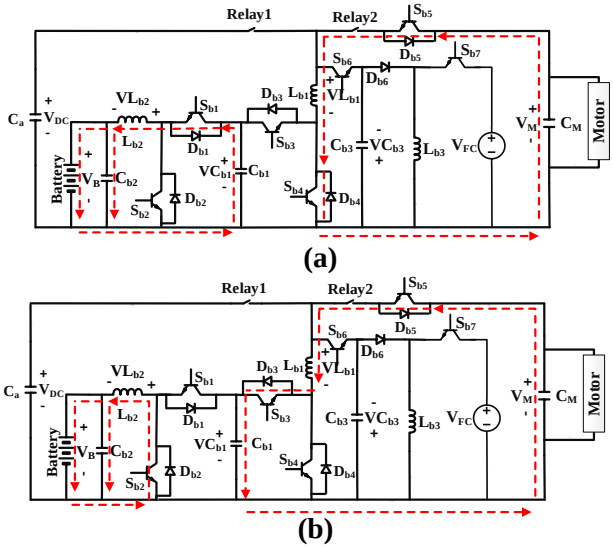


Fig. 8: Current paths of DC-DC stage in mode4

➢ **AC-DC Stage**

In order to invert the DC voltage of DC-link into AC, the AC-DC stage uses the switching pattern which is explained in [21] and detailed here. Similar to the mode1, the operation of this stage depends on the sign of the voltage grid as follows:

Vg>0: in this condition, during first state (0<t<DTs) Sa1 and Sa4 are turned ON so the L_a is magnetized with (V_{DC}-V_g) [Fig. 9 (a)]. In the next state (DTs<t<Ts) the Sa1 is turned OFF and L_a demagnetized via Da2 and Sa4 [Fig. 9 (b)].

Vg<0: when V_g is in its negative half-cycle, Sa2 has high frequency operation and Sa3 operates with grid frequency. This switching pattern causes L_a to magnetize and demagnetize as shown in Fig. 9 (c)-(d).

Using the same approach as the mode1, the voltage gain of AC-DC stage can be calculated in this mode. The voltage across L_a can be written as follows:

$$\begin{cases} V_{La} = V_{DC} - V_g & 0 < t < DT_s \\ V_{La} = -V_g & DT_s < t < T_s \end{cases} \quad (34)$$

By applying the volt-sec balance law, the voltage gain of buck inverter can be achieved as (35):

$$\frac{V_g}{V_{DC}} = D \quad (35)$$

➢ **DC-DC Stage**

As mentioned above, since the vehicle is connected to grid relay1 is ON and relay2 is OFF. Operation of the converter in this mode is divided into two states:

State1 (0<t<DTs): as depicted in Fig. 10 (a), in this state Sb2 and Sb3 are in ON-state so L_{b1} and L_{b2} are magnetized by (V_{Cb1}-V_{DC}) and (V_B), respectively.

State2 (DTs<t<Ts): by turning OFF both Sb2 and Sb3, the C_{b1} starts charging through the charged inductor (L_{b2}) so L_{b2} demagnetized by (V_B-V_{Cb1}). The L_{b1} is also demagnetized by (-V_{DC}) [Fig. 10 (b)].

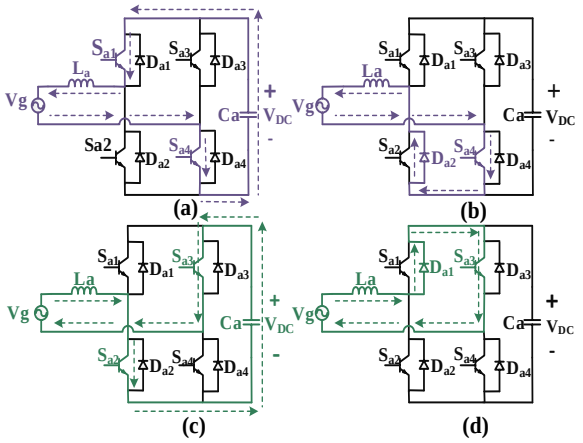


Fig. 9: Current paths of AC-DC stage in mode5.

In this mode, the volt-sec balance can be written as:

$$\langle i_{Lb1} \rangle = 0 \rightarrow \frac{1}{T_s}\left[\int_0^{DTs} (V_{Cb1} - V_{DC})dt + \int_{DTs}^{Ts} (-V_{DC})dt\right] = 0 \quad (36)$$

$$\langle i_{Lb2} \rangle = 0 \rightarrow \frac{1}{T_s}\left[\int_0^{DTs} (V_B)dt + \int_{DTs}^{Ts} (V_B - V_{Cb1})dt\right] = 0 \quad (37)$$

By using same approach as mode2, the voltage gain of mode5 can be obtained as:

$$\frac{V_{DC}}{V_B} = \frac{D}{1-D} \quad (38)$$

As studied in (11), (19), (30), (33), and (38), the converter works as a buck-boost which is an outstanding feature of that.

Design Considerations

The design considerations and procedure of inductive and capacitive components of proposed converter are detailed in this section. The total value of the inductive component of the AC input filter can be obtained as:

$$L_f = L_{req} + L_g \quad (39)$$

where L_{req} is the value of the required inductor which should be added and L_g is the grid impedance which is considered 4-5% of the base impedance [22]. So the

value of the required inductor that should be added to circuit can be calculated as:

$$L_{req} = \frac{1}{4\pi^2 f_c^2 C_f} - 4\times10^{-2} \times \left[\frac{1}{\omega_L}\right] \times \left[\frac{V_g^2}{P_{out}}\right] \quad (40)$$

where f_c is the cut-off frequency. Maximum value of the capacitive component of the filter can be calculate as [23]:

$$C_{f\,\max} = \frac{I_m}{\omega V_m}\tan(\theta) = \frac{\sqrt{2}P_{\max}}{\omega_L V_m V_g}\tan(\theta) \quad (41)$$

where, V_m, I_m, and θ are the peak value of grid voltage, peak value of input current, and displacement angle between grid voltage and input current, respectively.

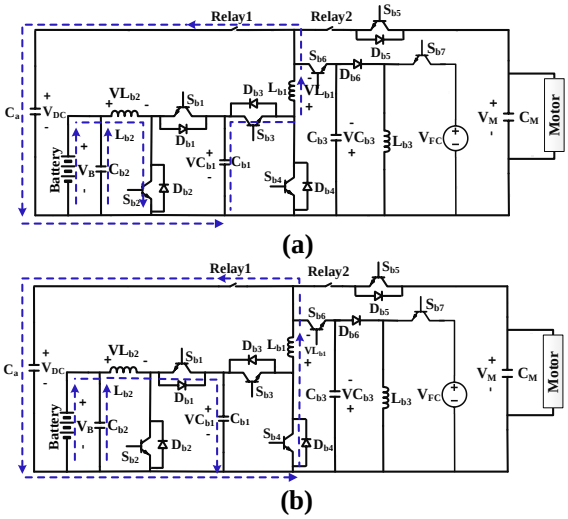


Fig. 10: Current paths of DC-DC stage in mode5

Reaching to a proper input current waveform entirely depends on the values of the inductor and capacitor of the AC-DC stage (L_a and C_a). In order to calculate minimum value of the inductor the magnetizing time of that should be analyzed. The voltage of L_a can be written as:

$$V_{La} = L_a\frac{di_{La}}{dt} \rightarrow V_{La} = L_a\frac{\Delta i_{La}}{\Delta t} \xrightarrow[\Delta t = DTs]{\Delta i_{La} = \Delta ig} \quad (42)$$

$$\Delta i_g = \frac{V_{La} * DTs}{L_a}$$

As shown in Fig. 3 (a), in the magnetizing time the voltage of L_a can be written as:

$$V_{La} = V_g \quad (43)$$

And as calculated in (3), the grid voltage can be rewritten as follows:

$$V_g = (1-D) * V_{DC} \quad (44)$$

By substituting (43) and (44) into (42) and manipulating it, the value of the L_a is obtained as:

$$L_a = \frac{V_{DC} * D * (1-D)}{\Delta i_g * f_s} \quad (45)$$

where f_s is the switching frequency. The worst case occurred in the maximum value of the D(1-D) term which is equal to 0.25 so:

$$L_a = \frac{V_{DC}}{4 * \Delta i_g * f_s} \quad (46)$$

Using an appropriate capacitor in the DC-link is the only way to deliver constant power to the battery by the single-phase grid. The value of this component affects the ripple of the voltage and current of the battery during charging mode. So it should be designed properly. The instantaneous power of the grid can be written as:

$$p(t) = V * I * \cos\varphi + 2 * V * I * \cos(2\omega t + \varphi) \quad (47)$$

which consists of an average and oscillating value of the power, respectively. The oscillating term affects the oscillating voltage amplitude of the DC-link voltage (Δv_{DC}) so:

$$\frac{1}{2}\cdot C_a \cdot v_{DC}^{\,2} = \int \tilde{p}dt \quad (48)$$

By substituting oscillating term of (47) into (48), the required value of C_a is obtained as:

$$C_a = \frac{2V_g I_g}{\omega \Delta v_{DC} V_{DC}} \quad (49)$$

Designing the L_{b1} and L_{b2} can be done similar to the L_a. For both inductors the below general equation can be used:

$$V_L = L\frac{di_L}{dt} \rightarrow V_L = L\frac{\Delta i_L}{\Delta t} \quad (50)$$

Since each inductor have different voltages in each mode, all modes should be considered and the worst case should be selected. The value of L_{b1} and L_{b2} are calculated in each mode as:

$$L_{b1} = \begin{cases} Mode1: & \frac{D\times V_{DC}}{\Delta i_{Lb1}\times f_s} \\ Mode2\&3: & \frac{(1-D)\times V_M}{\Delta i_{Lb1}\times f_s} \\ Mode4: & \frac{D\times V_M}{\Delta i_{Lb1}\times f_s} \\ Mode5: & \frac{(1-D)\times V_{DC}}{\Delta i_{Lb1}\times f_s} \end{cases} \quad (51)$$

$$L_{b2} = \begin{cases} Mode1\&4: & \frac{(1-D)\times V_B}{\Delta i_{Lb2}\times f_s} \\ Mode2\&3\&5: & \frac{D\times V_B}{\Delta i_{Lb2}\times f_s} \end{cases} \quad (52)$$

where Δi_{Lb1} and Δi_{Lb2} are the desired current ripple of L_{b1} and L_{b2}, respectively. According to the converter specifications the value of inductors in each operating mode should be calculated and the maximum of them should be selected. The value of the Lb3 can be calculated using below equation too:

$$L_{b3} = \frac{V_{FC} * D}{\Delta i_{Lb3} * f_s} \quad (53)$$

The C_{b1} can be sized using average current of L_{b2} (i_{Lb2}) as follows:

$$C_{b1} = \frac{i_{Lb2} \times (1-D)}{\Delta v_{Cb1} \times f_s} \quad (54)$$

where Δv_{Cb1} is the voltage ripple of the C_{b1}. The same approach can be used in order to obtain the value of C_{b3}.

Control Method

Since the proposed converter charges the battery via the grid in mode1 and returns the battery energy to grid during mode5, the power quality issues should be considered. The input current waveform in terms of THD and the power factor, are the main factors of a grid-connected converters which should be designed correctly. The proposed converter has the ability to work as a converter with power factor correction (PFC) and a converter with controllable absorbed and generated active and reactive power during mode1 and mode5, respectively, according to the processed smart grid commands or costumer requirements. This feature enables the grid operator to control connected converters during peak hours. In both aforementioned conditions an appropriate control method is needed to control the AC-DC stage and input current THD, simultaneously. Since the proposed converter is a two-stage one, each stage needs separated controllers which can work dependently or independently. For controlling both active and reactive power the controllers should work dependently in order to have constant voltage in the battery port. Proportional-Integral (PI) control is a very simple and robust method for controlling power converters. A very effective dual-loop PI controller is designed and adopted for the AC-DC stage in this paper. The first loop of the proposed controller consists of active and reactive control loops (P and Q loops) which control the used or injected P and Q powers according to the commands which are defined by costumer or smart grid by calculating reference input current. The second loop controls the input current according to the reference calculated by the previous loop by generating Sa1~Sa4 gate pulses. The operation of the proposed five-step dual-loop control method is detailed in this section. In the first step two delay blocks are used to generate the quadrature signals of the grid voltage and input current Fig. 12.

If the sampling frequency assumed 20kHz, one quarter delay leads to 100 samples (1/4*50). In the next step, the instantaneous pq theory introduced in [24] is used to calculate the single-phase P and Q power as illustrated in Fig. 12. In the third step, the calculated active and reactive power are used in the P and Q loops, respectively, in order to obtain references of active and reactive power. As depicted in Fig. 13, the P-loop controls active power by controlling DC-link voltage. At first, the error signal between calculated active power (P) and active power command (P_c) is fed to the primary PI controller which generates DC-link voltage reference ($V_{DC,ref}$). The secondary PI controller is used to calculate active power reference (P_{ref}) using error signal between measured and reference of the DC-link voltage. In the Q-loop, a PI controller is used to calculate reactive power reference according to the reactive power command (Q_c). It is worth mentioning that it is possible to control the DC-link voltage directly by defining $V_{DC,ref}$ by the costumer according to the grid and converter properties and battery voltage. Clearly in this condition only the reactive power can be controlled. In order to clarify the charging and discharging strategy, the control method selection process is illustrated in Fig. 14.

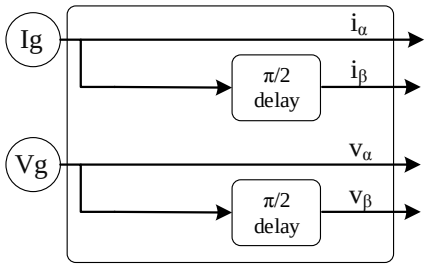


Fig. 11: First step of control method: calculating quadrature signals.

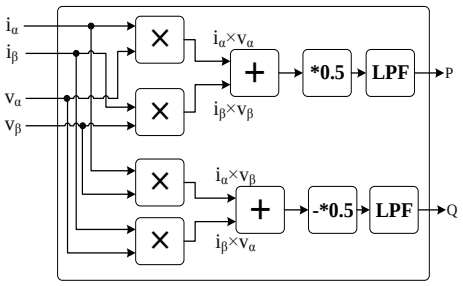


Fig. 12: Second step of control method: calculating active and reactive power.

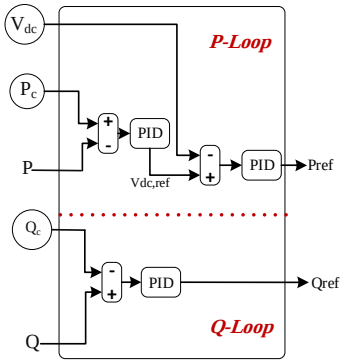


Fig. 13: third step of control method: calculating active and reactive power references.

In the fourth step, the input current reference (I_{ref}) is

obtained by using the generated active and reactive power references and (55)-(57) equations as follows:

$$\theta = \tan^{-1}\left(\frac{Q_{ref}}{P_{r\,ef}}\right) \quad (55)$$

$$I_{ref} = \frac{P_{r\,ef}}{V_g \cos(\theta)} \quad (56)$$

$$i_{ref}^{*} = \sqrt{2} I_{ref} \sin(w_t - \theta) \quad (57)$$

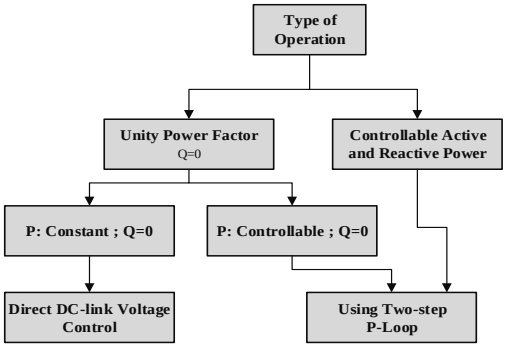


Fig. 14: Procedure of controller method selection.

In the last step the Sa1~Sa4 gate pulses are generated by using a PI controller, a comparator, and logic functions as shown in Fig. 15. At first error signal between measured and reference of input current signal is fed to a PI controller and then the output of that is compared with a high frequency (20-30 kHz) triangular wave. Finally logic functions are used to generate gate pulses.

Comparison Study

The proposed converter is compared with similar converters introduced in recent years in term of operating modes that they can work in and high frequency switches in each mode and results are provided in Table 1. At first blush, existence of 4 switches in the AC-DC stage and 7 switches in the DC-DC stage might come across as a cause of significant power loss in the circuit, but it is notable that there are not more than 4 high frequency switches in each mode.

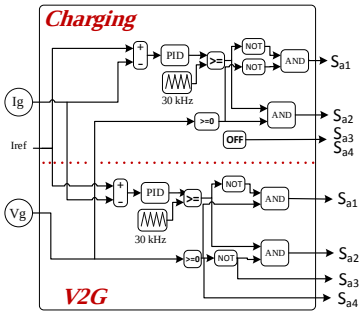


Fig. 15: last step of control method: generating gate pulses.

As explained in Table 1, the proposed converter is capable of working in five operating modes in buck-boost condition with less or equal number of high frequency switches in comparison of other converters, which is an impressive feature of that. The capacity of each component and cost analysis of the presented converter is indicated in Table 2. Two converters with 2kW and 5kW power are assumed and model and cost of each element are analyzed. Like other two-stage converters, DC-link capacitor increases the cost and volume of the converter. It should be noted that the analyzed converter is the main and only power circuit in a PHEV and there is no need for additional power circuit.

Simulation Results

The simulation of the proposed converter has been done in MATLAB/SIMULINK environment and results are provided in this section. The properties of the simulated system are tabulated in Table 3. The minimum values of passive components can be calculated according to the above-mentioned design considerations. The values of L_a, L_{b1}, L_{b2}, and L_{b3} can be obtained by using (46), (51), (52), and (53), respectively. (49) and (54) are used to calculate the minimum values of capacitors. The second control method (V_{DC} direct control) with unity power factor is selected for controlling AC-DC stage and the DC-DC stage is simulated open loop. Different DC-link, battery port, and motor voltages are selected during simulation in order to emphasize the buck-boost operation of the proposed converter. The power of battery and motor are assumed 5kW.

Table 1: Operating modes comparison of proposed converter with other presented converters

Reference	Number of high frequency switch(s) in :				
	Mode1	Mode2	Mode3	Mode4	Mode5
[10]	×	6 (Boost)	×	6 (Buck)	×
[11]	×	4 (Boost)	×	4 (Buck)	×
[12]	×	×	4 (Boost)	×	×
[13]	×	×	4 (Boost)	4 (Buck)	×
[14]	×	2 BB	4 BB	4 BB	×
[15]	×	2 BB	4 BB	4 BB	×
[16]	2 (Boost)	3 BB	×	3 BB	×
[17]	4 BB	1 (Boost)	×	1 (Buck)	×
[18]	4 BB	×	×	×	×
[19]	2 BB	2 BB	×	2 BB	×
[20]	3 (Buck)	×	×	×	5 (Boost)
Proposed Converter	4 BB	2 BB	4 BB	2 BB	4 BB

- BB: Buck-Boost

Table 2: Cost Analysis of the proposed converter

Component	2kW	5kW	2kW	5kw
	Parameters	Parameters	Cost	Cost
AC-DC Stage Switches	4*TTKK2837 (24A;500V)	4*FGW40N120HD (40A;1200V)	4*(1.01$)=4.05$	4*(0.86$)=3.46$
DC-DC Stage Switches	5*KF13N60(13A;600V) 2*FGW40N120HD (40A;1200V)	3*FGW40N120HD(40A;1200V) 3*GT30J122A(30A;600V) 1*KF130N60(13A;600V)	5*(0.36$)+ 2*(0.86$)=3.52$	3*(0.86$)+ 3*(0.8$)+ 1*(0.36$)=5.34$
Diode (Db6)	30eth06(30a;600v)		0.62$	
Inductors	core and wire		11.5$	13$
DC-Link Capacitor (Ca)	6*(1360µF;450V)		6*(2.72$)=16.3$	
Cb1	4*(470µF;450V)		4*1.5$=6$	
Cb2	1*(470µF;250V)		0.95$	
Cb3	1*(470µF;250V)		0.78$	
CM	4*(560µF;450V)		4*1.5$=6$	

The presented converter is simulated in mode1 with VB=240V and input current and grid voltage are shown in Fig. 15 and as can be seen the power factor is more than 0.99. Fig. 16 shows the FFT analysis of the input current over 3 cycles which is 4.43%. The perfect ability of the converter to track the reference input current generated by the controller is illustrated in Fig. 17.

Table 3: The Proposed Converter Specifications

	Simulation	**Experimental**
AC Input Voltage	220 (RMS)	36 (RMS)
DC –Link Voltage	350 V	110,90 V
FC Voltage	150 V	20 V
L_a	6 mH	4 mH
L_{b1},L_{b2}	5 mH	1.5 mH
L_{b3}	1.2 mH	1.5 mH
C_a	10 mF	4 mF
C_{b1}	500 uF	1000 uF
C_{b2}	470 uF	680 uF
C_{b3}	120 uF	1000 uF
C_M	470 uF	680 uF
AC Input Frequency	50 Hz	50 Hz
Switching Frequency	30 kHz	25-30 kHz
Power Factor	0.99	0.99
Controller	-	ARMSTM32F103RET
Mosfet	-	KF13N60
Current Sensor	-	ACS712

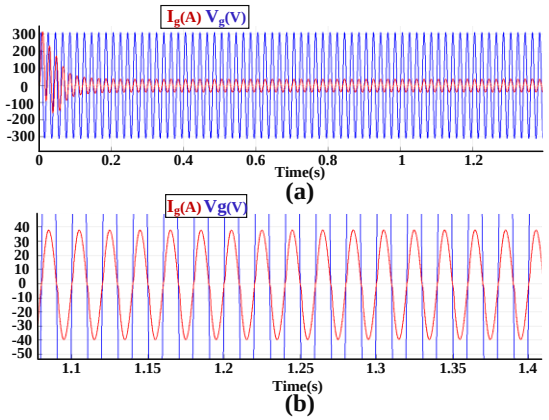


Fig. 16: (a) grid voltage and input current in mode1 (b) enlarged version

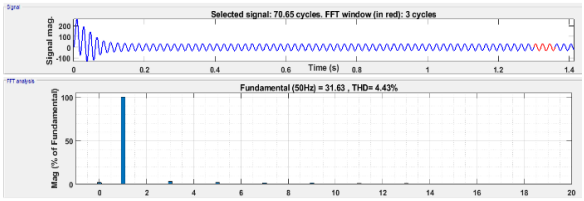


Fig. 17: FFT analysis of input current in mode1

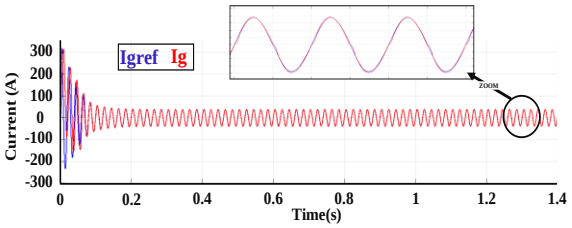


Fig. 18: Reference and measured input current in mode1.

As shown in Fig. 19, the DC-link and battery port voltages have very fast transient and acceptable steady-state ripple.

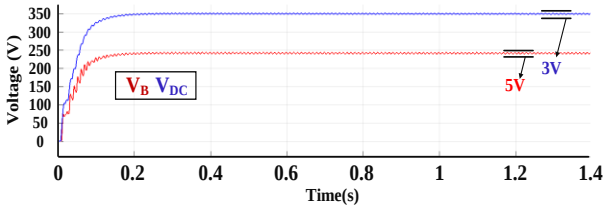


Fig. 19: DC-link and battery port voltages in mode1.

Voltage and current of L_{b1}, L_{b2}, and C_{b1} in each time intervals are shown Fig. 20 through Fig. 22, respectively.

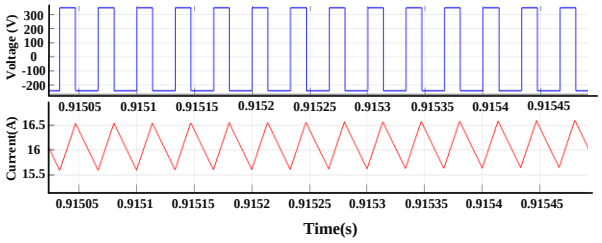


Fig. 20: voltage and current of Lb1 in mode1.

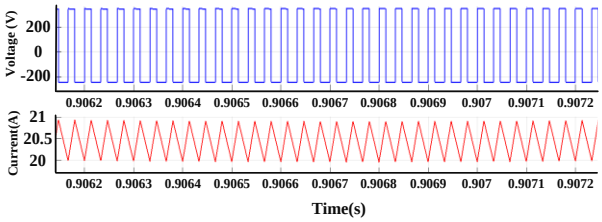


Fig. 21: voltage and current of Lb2 in mode1.

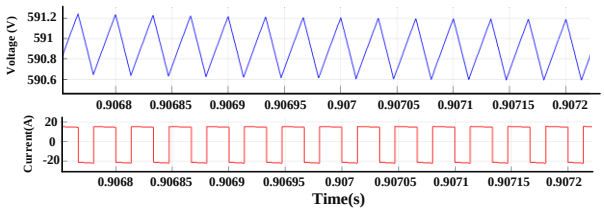


Fig. 22: voltage and current of Cb1 in mode1.

The second mode is simulated with V_B=240V and V_M=600V and results are shown in Fig. 23.

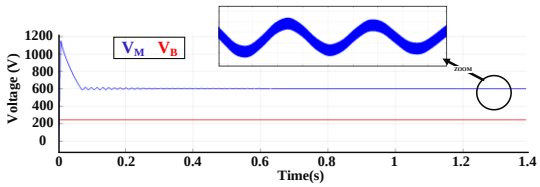


Fig. 23: Battery port and motor voltages in mode2.

The motor voltage in different conditions (in terms of battery and FC voltage) for various duty cycles is illustrated in Fig. 24.

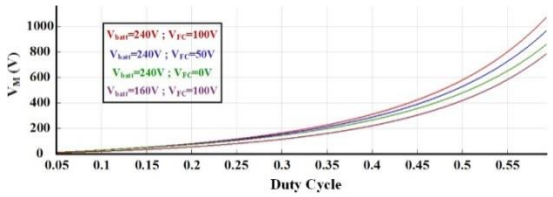


Fig. 24: Motor voltage in different conditions

Fig. 25 shows the transient of the motor voltage during switching between mode2 and mode3. At t=0.6s FC starts working and at t=1.5s finishes. As can be seen, the V_M is fixed on 600V in its steady-state. The gate pulses of Sb2, Sb3, Sb6, and Sb7 are shown in Fig. 26.

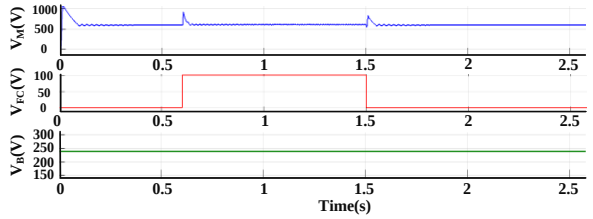


Fig. 25: VM, VFC, and VB during switching between mode2 and mode3.

Fig. 27 shows the motor voltage and battery port voltage during braking condition (Mode4). In order to validate buck-boost operation of the proposed converter the motor voltage is decreased in three steps but battery port voltage is fixed on 240V.

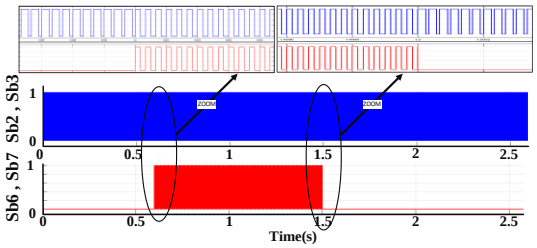


Fig. 26: Gate pulses of Sb2, Sb3, Sb6, and Sb7 during switching between mode2 and mode3.

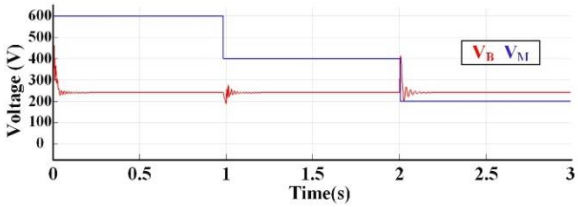


Fig. 27: motor and battery port voltage in mode4.

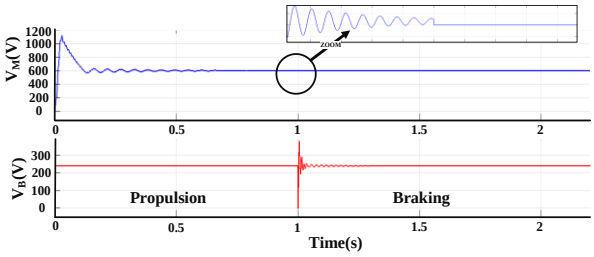


Fig. 28: Battery and motor voltages during switching between propulsion and braking modes.

In order to analyze the dynamic response of the converter during braking times, the proposed converter is simulated during switching between propulsion and braking modes and results are shown in Fig. 28. It is assumed that the vehicle starts braking at t=1s.

The V2G mode (Mode5) is also simulated. Fig. 29 shows grid voltage and input current in mode5 and FFT analysis of input current is depicted in Fig. 30.

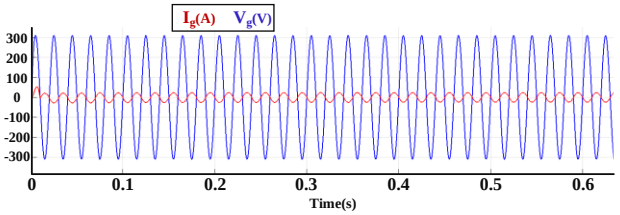


Fig. 29: grid voltage and input current in mode5.

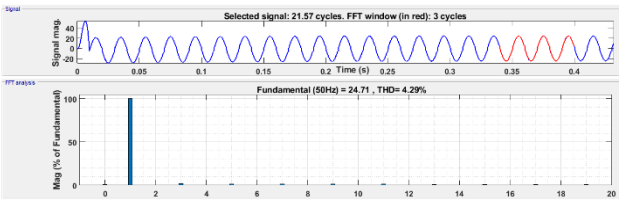
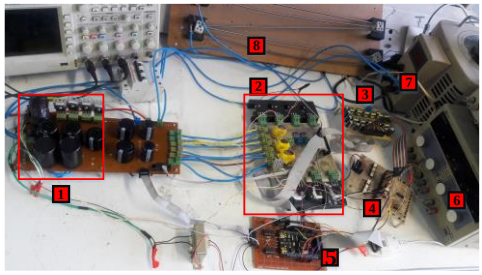


Fig. 30: FFT analysis of input current in mode5

Experimental Verification

A reduced-scale prototype of proposed converter has been built and experimental results are provided in order to verify simulation ones. Fig. 31 shows the experimental setup with specifications tabulated in Table 3. It is worth mentioning that the value of parameters are obtained using the aforementioned design considerations. Similar to simulation, the prototype is controlled and tested in UPF condition during mode1. In order to compare experimental results with simulation ones, the proposed converter is simulated again with experimental parameters and result are provided in this section.



1- AC-DC Stage
2- DC-DC Stage
3- Isolated gate drive supply
4- Gate driver board
5- Control board (STM32F103RET)
6- ACS712 and op-amps supply
7- Autotransformer
8- Load

Fig. 31: Implemented system.

Fig. 32 shows grid voltage and input current during mode1 which have unity power factor. Fig. 32 (c) shows converter behavior during battery power changing from 250W to 150W. In order to test buck and boost operation of DC-DC stage, mode1 is tested under two conditions, (V_{DC}=110V, V_B=80V, P_B=250W) and (V_{DC}=90V, V_B=120V, P_B=250W) and results are shown in Fig. 33.

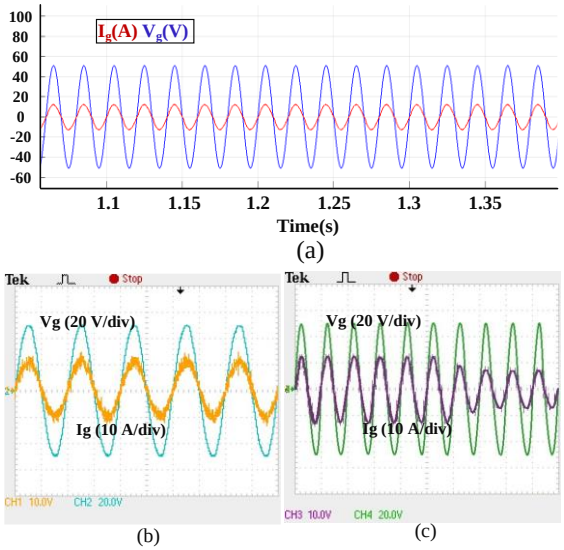


Fig. 32: grid voltage and input current in mode1; Simulation: (a) PB=250W; Experimental: (b) PB=250W (c) PB decreases from 250W to 150W.

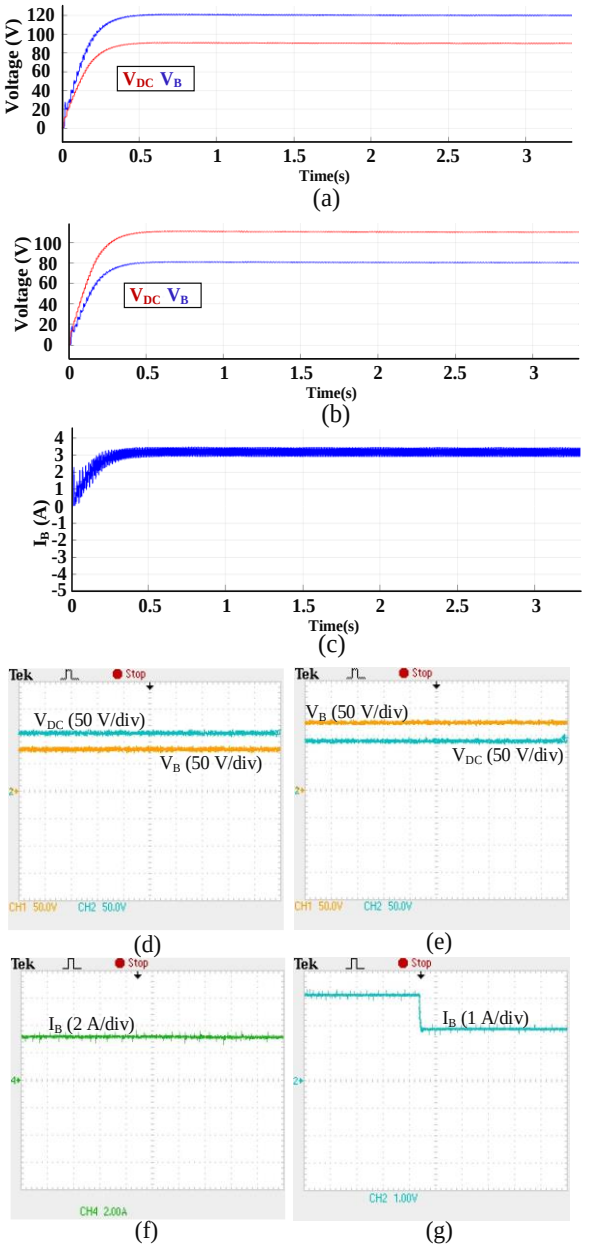


Fig. 33: Simulation: DC-link and battery port voltage during mode1 in (a) boost condition (b) buck condition (c) battery current in buck condition; Experimental: DC-link and battery port voltage during mode1 in (d) buck condition (e) boost condition (f) battery current (PB=250W) (g) battery current (PB decreases from 250W to 150W) in buck condition.

The converter is tested during mode2 with V_B=80V and V_M=120V; P_M=250W. Fig. 34 shows the voltage and current of the battery and motor ports in this mode. Voltage and current of L_{b1} and L_{b2} are depicted in Fig. *35*. The converter is operated in mode3 in order to feed the 250W motor port and Fig. 36 shows the FC, battery, and motor voltage during this mode.

The braking mode (mode4) is tested under two conditions: V_M=120V and V_M=70V with V_B=80V; P_B=250W and results are depicted in Fig. 37.

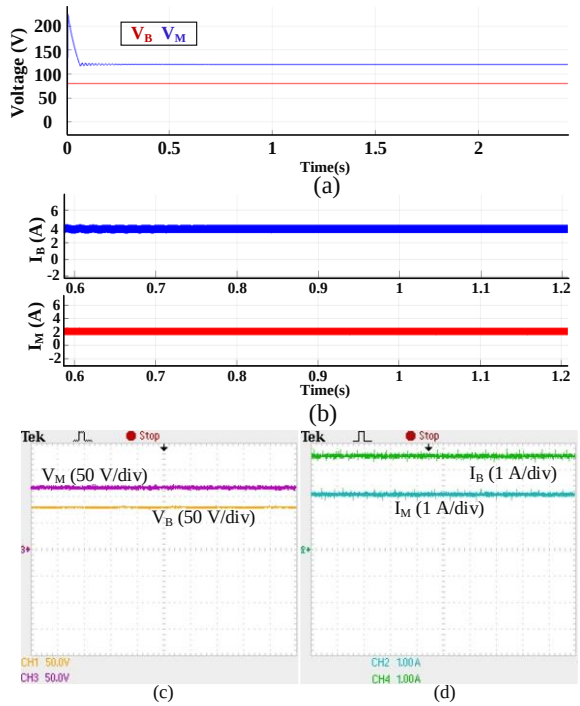


Fig. 34: Simulation: (a) Battery port and motor voltage in mode2 (b) Battery port and motor current in mode2; Experimental: (c) Battery port and motor voltage in mode2 (d) Battery port and motor current in mode2.

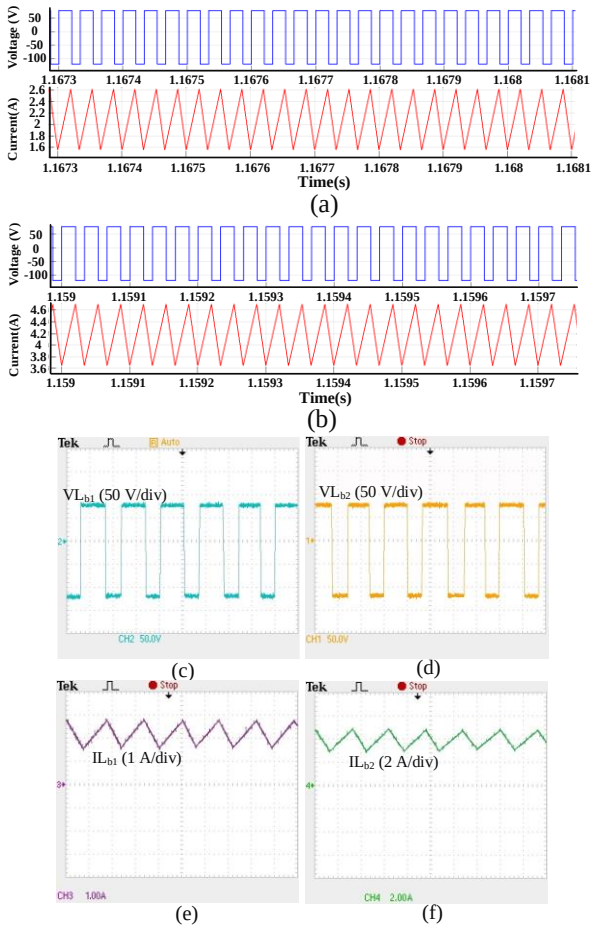


Fig. 35: Simulation: voltage and current of (a) Lb1 (b) Lb2; Experimental: voltage across (c) Lb1 (d) Lb2, current of (e) Lb1 (f) Lb2 during mode2.

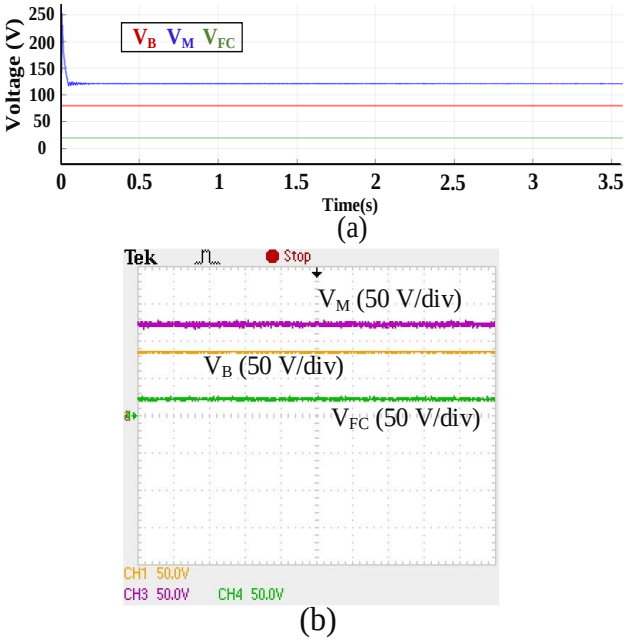


Fig. 36: (a) Simulation results (b) experimental results of FC, battery, and motor voltages during mode3.

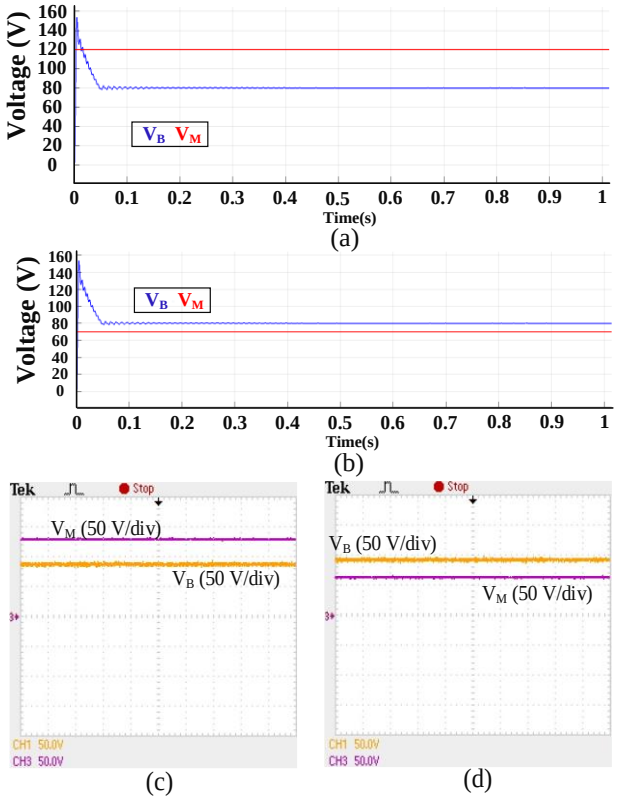


Fig. 37: Simulation: battery and motor voltages (a) buck (b) boost condition; Experimental: battery and motor voltages (c) buck (d) boost condition during mode4

Vehicle to grid mode is also tested and results are shown

in Fig. 38.

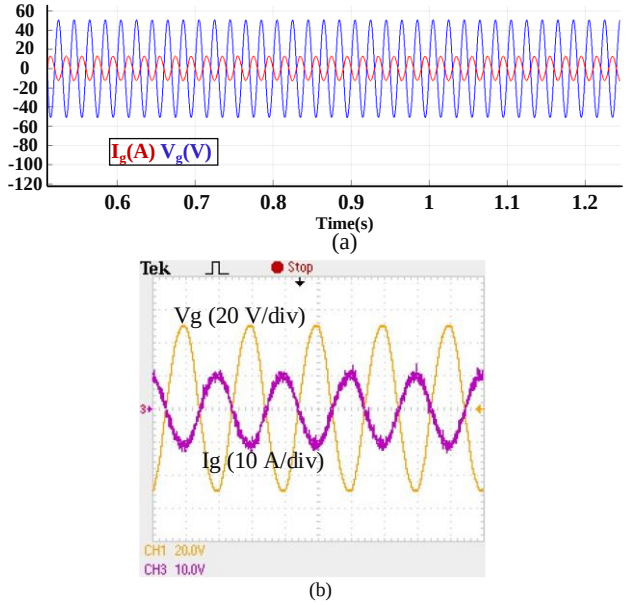


Fig. 38: (a) Simulation (b) Experimental results of grid voltage and input current during mode5.

Results and Discussion

The proposed converter is simulated in MATLAB/SIMULINK software in all operating modes. Current and voltage waveforms with their transient and steady state in all operating conditions are provided in order to confirm its perfect ability to track references (voltage and current) in terms of dynamic response and steady state ripple. The power factor and THD of the input current is also analyzed which shows its unity power factor and acceptable current THD (less than 5%) in the operating modes in which the grid works as a power source. In order to show the converter behavior during modes switching and voltages changing, it is simulated in different conditions. An experimental prototype is also implemented and experimental results are provided in all operating modes. As shown in figures, the input current has acceptable THD (less than 5%) and converter power factor is more than 0.9. In order to compare experimental results with simulation ones, the converter is also simulated with experimental parameters and results are provided.

Conclusion

A bidirectional buck-boost integrated converter has been introduced in this paper. The proposed converter can be used in PHEVs which use battery and FC as power sources and is capable of working in five different operating modes which have been explained and analyzed in detail in this paper. The design procedure of the presented converter is provided and also an effective control method to control active and reactive power during charging and V2G modes is introduced. The proposed converter is also compared with other similar converters introduced in recent years in terms of number of high frequency switches in each mode. The simulation of the presented converter is done in MATLAB/SIMULINK in order to validate system analysis. An experimental prototype of the converter has been built and tested and experimental results are provided.

Author Contributions

H. Soltani Gohari designed, analyzed, simulated, implemented the system, and wrote the manuscript. K. Abbaszadeh carried out the supervision.

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Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

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Research paper

A Preprocessing Technique to Investigate the Stability of Multi-Objective Heuristic Ensemble Classifiers

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Abstract

Background and Objectives: According to the random nature of heuristic algorithms, stability analysis of heuristic ensemble classifiers has particular importance.
Methods: The novelty of this paper is using a statistical method consists of Plackett-Burman design, and Taguchi for the first time to specify not only important parameters, but also optimal levels for them. Minitab and Design Expert software programs are utilized to achieve the stability goals of this research.
Results: The proposed approach is useful as a preprocessing method before employing heuristic ensemble classifiers; i.e., first discover optimal levels of important parameters and then apply these parameters to heuristic ensemble classifiers to attain the best results. Another significant difference between this research and previous works related to stability analysis is the definition of the response variable; an average of three criteria of the Pareto front is used as response variable. Finally, to clarify the performance of this method, obtained optimal levels are applied to a typical multi-objective heuristic ensemble classifier, and its results are compared with the results of using empirical values; obtained results indicate improvements in the proposed method.
Conclusion: This approach can analyze more parameters with less computational costs in comparison with previous works. This capability is one of the advantages of the proposed method.

Introduction

Ensemble classification is a popular model applied to improve the performance of individual classifiers and decrease their weaknesses [1]. Ensemble classifier has been welcomed by many researchers; examples of recent research in this area are [2]-[8]. For example, a new selection ensemble method is proposed in [2] to ameliorate the generalization ability and recognition efficiency of the maritime surveillance radar; this technique is based on k-medoids clustering and random reference classifier. A classification algorithm based on MapReduce and ensemble learning for effectively classifying imbalanced large datasets is introduced in [6]. In [8] a novel integration approach of binary classifiers is proposed for multi-class classification; this method can effectively combine information of several binary classifiers into the multi-class classifier.

Heuristic algorithms have high efficiency to solve optimization problems; [9]-[12] are some researches of different fields such as VLSI circuits, clustering and medicine which used heuristic algorithms to solve their problems. Another field, which can use these algorithms, is ensemble classification, in which several important issues can directly affect the performance of the designed ensemble classifier. In this situation, it is often impossible to find the best solution using trial and error,

because there is a complex search space with high dimensions. Therefore, considering the capability of efficient probing of these algorithms, heuristic ensemble classifiers are proposed, which are designed by heuristic algorithms [13]. Many types of researches have addressed this field, such as [14]-[18]. For instance, in [14] a novel type of the firefly algorithm is introduced for classifier ensemble reduction; these ensemble classifiers have better performance in comparison with full-sized ensemble classifiers. A novel method for classifier ensemble reduction is presented in [16]; this paper employs feature selection techniques to minimize redundancy in an artificial dataset; this dataset is generated by transforming ensemble predictions into training samples, and classifiers are treated as features. The purpose is to further decrease the size of an ensemble, while improving classification efficiency and accuracy. Also, to select a reduced subset of such artificial features, the global heuristic harmony search is utilized. A novel evolutionary multi-objective ensemble classifier is proposed in [18] for performing feature selection and classification problems. This ensemble can improve the performances of classification of neural network models with a smaller number of input features.

Investigating the stability of these ensembles is an important issue due to the stochastic nature of heuristic algorithms; various answers, obtained in different simulation runs, have a severe dependency on the structural parameters of heuristic algorithms [13]. Despite extensive studies on the various aspects of heuristic ensemble classifiers, the stability of them has been neglected; only a few studies like [13] and [19] have been addressed this issue. In [13] a statistical approach termed two-level factorial design is used to investigate the stability of the heuristic ensemble classifier; in this way, the effects of three structural parameters of the multi-objective algorithm i.e., inflation rate, leader selection pressure and deletion selection pressure on the performance of the designed heuristic ensemble classifier are analyzed.

The stability of the heuristic ensemble classifier is investigating in [19] by using statistical method. For this aim, three regression models (linear, quadratic and cubic) are checked by applying F-test to find better model in each case; in this paper, six parameters of the heuristic algorithm are considered as variables for stability analysis.

The values of structural parameters in heuristic algorithms are usually set by trial and error, which is time-consuming and partly difficult. Considering the significance of stability, the aim of this paper is to provide a method for the optimal setting of the important parameters. The proposed method can be applied as a preprocessing step before employing heuristic ensemble classifiers. In this paper, a heuristic ensemble classifier is designed by using Multi-Objective Inclined Planes Optimization (MOIPO) algorithm to achieve this goal.

Then, in order to analyze the stability, the impact of 11 parameters of the employed algorithm on the ensemble classifier is investigated. To this end, the Plackett-Burman Screening method is first used to identify the important parameters. Then, important parameters are considered as input variables of the Taguchi method to optimize these parameters. In this paper, Design Expert software and Minitab software are used to implement the Plackett-Burman and Taguchi method, respectively.

The rest of this article is organized as follows: In section 2, the design of the experiment is presented. Section 3 provides a review of the employed optimization algorithm. The method of stability analysis of ensemble classifiers and optimizing important parameters is described in Section 4. Section 5 is for simulation results. Section 6 provides results and discussion. Finally, conclusion is explained in section 7.

Design of Experiments

"Design of Experiments (DoE) is a method of systematically obtaining and organizing knowledge so that it can be used to amend operations in the most efficient manner possible" [20]. DoE includes experiments in which the rate of the change of output response can be observed by making knowledgeable changes in input variables. In fact, the factors are simultaneously experimented to consider the interactions between factors. This method opposes the classic approach, OFAT; i.e., One Factor At a Time where one variable is varied at a time, and all other variables are kept fixed in the experiment.

OFAT experiments often are unqualified, unreliable, and time-consuming and may lead to false optimum conditions for the process. Statistical approaches play a significant role in analyzing and construing the data from engineering experiments. In DoE, intentional changes in the input variables (or factors) are created, and then the variation of the output performance is determined. It's worth noting that each variable influences the response in a special way; some may have strong impacts, some may have medium impacts, and some may have no impacts. Thus the aim of a DoE is to discover which set of factors in a process affect the performance most (screening step) and then specify the best levels for these factors to obtain satisfactory output performance (optimization step) [21].

In this research, Plackett-Burman and Taguchi methods are used for screening and optimization steps

of DoE, respectively.

These methods are described in the following.

A. Plackett-Burman Design

Plackett–Burman design is the most common screening approach that screens a large number of factors and specifies important one in a minimal number of runs with a good degree of accuracy. The number of runs needed to check the main effects is multiple of 4 in Plackett–Burman designs instead of 2 as in the case of full factorial design [22].

One of the advantages of Plackett–Burman design is to reduce the amount of observation data; this will be more important when the number of variables is large. For example, for screening 11 factors, 12 observations (runs) are adequate, while a full factorial design would require 211 observations.

In this approach, each factor is investigated at two levels; –1 for the low level and +1 for the high level. The result analysis of this method is described in the section named simulation results.

B. Taguchi Design

As stated before, after identifying the important factors, the optimization step starts. In a traditional optimization method, first, the targets for the output responses are specified, and then the related settings for input variables are performed. In these approaches, factors are investigated one by one in order to determine the best settings to optimize response first, and then the best settings of all factors are collected as the optimal design for the system. But, this procedure cannot vouch that the composed best levels of the factors are the actual optimal design. These combined best settings may not be the optimal response for the system if significant interactions exist among the factors. One-factor-at-a-time optimization approaches are not time efficient. In other words, the one-factor-at-a-time method is not really an optimization approach. New procedures based on the robust design (i.e., Taguchi Method) are more efficient than the traditional one-factor-at-a-time optimization method [23].

Taguchi method is a statistical method proposed by Genichi Taguchi to improve the quality of manufactured goods, and more recently, also applied to engineering [24]. The objective of the Taguchi method is to set the design factors to optimal levels, such that the system response is robust [25]. Taguchi method to DoE is easy to be accepted and applied for users with finite information of statistics; thus it has achieved wide popularity in the engineering and scientific community [26].

Signal to Noise Ratio (SNR) is employed in Taguchi design as the quality specification of choice. SNR is used as a measurable value instead of standard deviation due to the fact that, as the mean reduces, the standard deviation also decreases, and vice versa [26]. The purpose of the SNR is to maximize the signal and minimize the impact of noise. The goal is to gain robustness, and higher SNR leads to greater robustness [27].

Multi-Objective Optimization Algorithms

There are four reasons for popularity of the heuristic algorithms; avoidance from local optima, flexibility, simplicity and having a mechanism without derivation [28]. These methods guarantee a greater probability to reach optimal answers because it utilizes a population to search the problem space [29].

In real applications, there are problems that under specific situations are concurrently confronted with several cost functions [30]. These problems can be solved using multi-objective optimization, in which a set of solutions is defined as optimal solutions. Searching operation in multi-objective heuristic algorithms is accomplished in parallel i.e., a set of agents search the problem space. So, they can find Pareto-optimal solutions with a single simulation run.

In general, the following points should be considered in multi-objective optimization:

1- The distance from the non-dominated front to the Pareto-optimal front should be minimized. This measure is known as Generational Distance (GD) and is specified in (1) in which n is the number of non-dominated answers and d_i is the Euclidean distance between each of these answers and the nearest solution in the Pareto-optimal front [31]:

$$GD = \frac{\sqrt{\sum_{i=1}^{n} d_i^2}}{n} \tag{1}$$

2- Discovered solutions should have good distribution. For this reason, Spacing (SP) metric [32] was introduced to measure how evenly the members of a Pareto front are distributed. A value of zero for the spacing metric means that all members of the Pareto front are equally spaced. This metric is specified in (2) in which $\bar{d}$ is the mean of all d_i and n is the number of non-dominated answers:

$$SP = \sqrt{\frac{\sum_{i=1}^{n} (\bar{d} - d_i)^2}{n-1}}$$
$$d_i = \min_j \left(\begin{array}{l} \left| f_1^i(x) - f_1^j(x) \right| + \left| f_2^i(x) - f_2^j(x) \right| \\ + \left| f_3^i(x) - f_3^j(x) \right| \end{array} \right) \tag{2}$$
$$i, j = 1,2,\ldots,n$$

3- Mean Ideal Distance (MID) is used for measuring

the closeness between Pareto solution and an ideal point. In a minimization problem, this metric is formulated as (3) in which f_1^i, f_2^i and f_3^i denote the first, second and third objective value of the i-th non-dominated solution respectively and n is the number of non-dominated answers:

$$MID = \frac{\sum_{i=1}^{n} \sqrt{f_i^i + f_2^i + f_3^i}}{n} \quad (3)$$

It is obvious that less value of this metric is of interest [33].

The multi-objective algorithm used in this paper is described in the following.

A. Multi-Objective Inclined Planes Optimization (MOIPO) Algorithm

The IPO algorithm is inspired by the dynamic movement of spherical objects along a frictionless inclined surface. These objects tend to reach the lowest points. In this algorithm, the agents are some small balls that explore the problem space to discover optimal solutions. The basic idea of IPO is to impute height to each agent, regarding its objective function. This algorithm is fully explained in [34].

The main structure of the IPO algorithm should be reformed to use it in multi-objective problems. The steps of multi-objective IPO are as follows:

1- Initialize the population, a repository for non-dominated solutions, and evaluation.
2- Separate non-dominated members and store them in the repository.
3- Generate the hypercube of the objective space.
4- Movement of each search agent according to the related equations.
5- Update the IPO parameters.
6- Add non-dominated members of the current population to the repository.
7- Delete dominated members from the repository.
8- Delete additional members if the size of the repository is more than the specified capacity.
9- End if the end conditions are established otherwise go back to step 3.

Stability Analysis of Heuristic Ensemble Classifiers and Optimizing Important Parameters

In this paper, to investigate the stability of heuristic ensemble classifiers, the effect of 11 parameters of the employed heuristic algorithm on a typical heuristic ensemble classifier is investigated. To reach this aim, the Plackett–Burman design is first used for recognizing important parameters. Then, important parameters are considered as input variables of the Taguchi design in order to optimize these parameters. It should be noted that Design Expert and Minitab are used for the implementation of Plackett–Burman design and Taguchi design, respectively.

Ensemble classifier studied in this research is an ensemble designed by MOIPO with the aim of minimizing ensemble size and maximizing the average of accuracy and the average of reliability for classifying Glass dataset. Glass dataset is one of the Benchmark data available at UCI machine learning repository. It has 214 samples, 9 features and 2 classes and can be as a good representative of overlapped data.

One of the main differences of this method with previous works is the definition of the response variable; the response variable is defined as the mean of the three criteria of the Pareto front; these measures are GD, SP, and MID, which introduced in the previous section.

Parameters studied in this research have two levels; low and high. The values of these levels are shown in Table 1. *MaxIt*, *npop*, *Alpha*, *Beta*, and *Gamma* are the number of iterations, population size, inflation rate, leader selection pressure, and deletion selection pressure, respectively.

Table 1: Low and high levels of parameters

Parameter	Low Level	High Level
MaxIt	200	600
Npop	20	50
C_1	0.1024	12
C_2	0.2399	3.6577
$Shift_1$	1	740
$Shift_2$	80	798.0776
$Scale_1$	0.0036	0.9999
$Scale_2$	0.0034	0.9002
Alpha	0.1000	0.2000
Beta	4	6
Gamma	2	4

It is worth noting that the levels of IPO parameters i.e., c_1, c_2, $shift_1$, $shift_2$, $scale_1$, and $scale_2$ have been extracted according to [34] which is the main reference of IPO algorithm. Also, *Alpha, Beta,* and *Gamma* are the parameters of multi-objective version and their values have been obtained from usual values used in other works like [13] and [19].

Simulation Results

As stated before, the aim of this paper is to find important parameters of the heuristic algorithm (i.e., finding the parameters which influence on the performance of the designed heuristic ensemble classifier) and also find the optimal levels of the important parameters. To achieve this goal, two steps should be done; the first step is the screening step which employs Plackett–Burman approach to identify important parameters from all supposed parameters.

The next step is optimization step; in this step, the optimal levels of the significant parameters are found using Taguchi method.

Design Expert software is used for the screening step i.e., Plackett–Burman method.

According to the obtained design matrix in Plackett–Burman method, simulations are performed to complete the response column. Table 2 shows the values of the design matrix and the response variable from the simulation. In this table, -1 and 1 represent low and high levels for each factor, respectively.

In fact, for different values of the parameters in design matrix, simulation in Matlab is run and the response value is obtained.

After completing the last column of the table, the outputs of this step are obtained by using this matrix; these outputs are reported in the following.

Table 2: Obtained design matrix from plackett–burman method and response variable

Run	*MaxIt*	*npop*	C_1	C_2	$Shift_1$	$Shift_2$	$Scale_1$	$Scale_2$	*Alpha*	*Beta*	*Gamma*	Response
1	1	1	-1	-1	-1	1	-1	1	1	-1	1	29.0813
2	1	-1	1	1	1	-1	-1	-1	1	-1	1	0.8200
3	1	1	-1	1	1	1	-1	-1	-1	1	-1	0.7154
4	-1	-1	-1	1	-1	1	1	-1	1	1	1	8.5715
5	1	-1	1	1	-1	1	1	1	-1	-1	-1	25.2336
6	-1	1	-1	1	1	-1	1	1	1	-1	-1	33.9415
7	-1	1	1	-1	1	1	1	-1	-1	-1	1	18.1211
8	1	1	1	-1	-1	-1	1	-1	1	1	-1	13.5830
9	1	-1	-1	-1	1	-1	1	1	-1	1	1	12.7499
10	-1	1	1	1	-1	-1	-1	1	-1	1	1	16.3629
11	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	2.0088
12	-1	-1	1	-1	1	1	-1	1	1	1	-1	17.4415

One of the outputs is Pareto chart which is presented in the analysis section; this chart indicates the t-value for all the supposed parameters.

This chart is illustrated in Fig. 1. According to this chart, it is clear that the parameters B, G, H, and K have a high contribution in the response; because only these parameters have been able to pass the threshold of t-value.

The parameter J is close to the threshold, but it has not passed it.

Therefore, in order to obtain the results for the analysis of variance, the five mentioned factors are selected.

As stated in the above, the output of the Pareto chart (parameters with high contribution) is used for analysis of variance. The results for the analysis of variance are reported in Table 3.

Table 3: Results for analysis of variance

Parameter	Sum of Squares	Degrees of Freedom	F-value	P-value	R^2	Adjusted R^2	Evaluation
Model	1231.7300	5	21.1300	0.0010	0.9463	0.9015	Suggested
B-npop	168.6600	1	14.4600	0.0089	-	-	Significant
$G\text{-}Scale_1$	174.6400	1	14.9800	0.0083	-	-	Significant
$H\text{-}Scale_2$	690.0700	1	59.1800	0.0003	-	-	Significant
J-Alpha	66.5300	1	5.7100	0.0541	-	-	Not Significant
K-Beta	131.8300	1	11.3100	0.0152	-	-	Significant

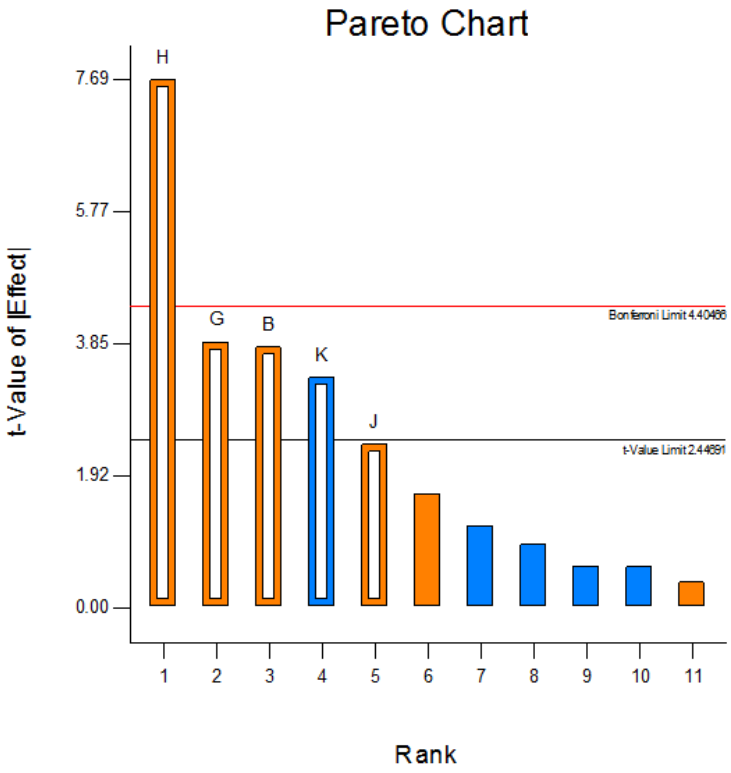

Fig. 1: Pareto chart; the output of Design Expert Software.

Regarding the values of R^2 and adjusted R^2 in the Table 3, it can be concluded that this model i.e., linear is suitable.

Also, obtained p-values indicate that four parameters i.e., *npop*, $Scale_1$, $Scale_2$, and *Beta* are significant. (Level of significance is 0.05)

Now, we know that linear model is specified as a suitable model.

Another outcome of the Plackett–Burman method is the estimated coefficients for each parameter to complete the equation of the model. So, this model can be determined by (4):

$$y = 14.89 + 3.74899 \times npop + 3.81489 \times Scale_1 + 7.58324 \times Scale_2 + 2.35459 \times Alpha - 3.31451 \times Beta \quad (4)$$

Besides the analysis of variance, checking the normality of the data or the residuals is one of the assumptions for the efficiency of the model. In this way, data may need to be transformed (in terms of being normal). To clarify this, the Box-Cox plot, another output of the method, should be checked. If blue and green lines situate near each other and both of them place between red lines, no transform is needed. The Box-Cox plot is shown in Fig. 2. According to the above description and also the report of the plot (left side of the plot), no transform is needed.

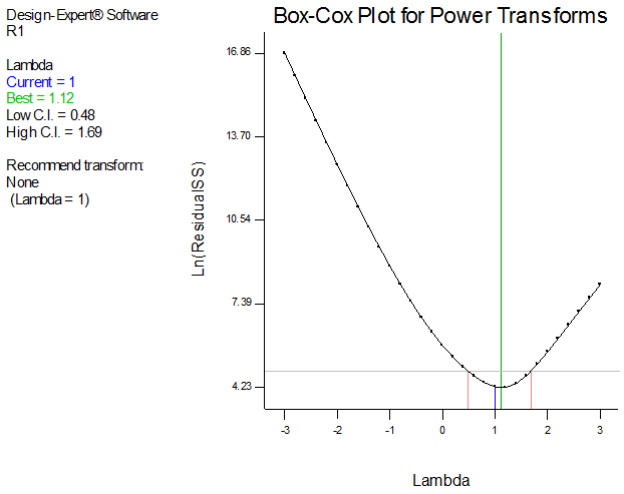

Fig. 2: Box-Cox plot.

Up to now, important parameters are determined by using Plackett–Burman design.

The next step is to optimize these parameters. Taguchi design is used for this step and is implemented in Minitab software. In this method, L12 design is selected considering the number of parameters and related levels. Table 4 indicates the Taguchi design matrix and response in which 1 and 2 demonstrate the low level and high level, respectively. It should be noted that the column of response is obtained by using the related values of parameters in the simulation run in Matlab.

Table 4: Taguchi design matrix and related responses

Run	*npop*	$Scale_1$	$Scale_2$	*Beta*	Response
1	1	1	1	1	2.9060
2	1	1	1	1	1.0439
3	1	1	2	2	19.9259
4	1	2	1	2	6.8677
5	1	2	2	1	1.2943
6	1	2	2	2	17.5981
7	2	1	2	2	16.5677
8	2	1	2	1	2.2139
9	2	1	1	2	12.4842
10	2	2	2	1	6.6250
11	2	2	1	2	1.6371
12	2	2	1	1	9.7931

The following figures, i.e., main effects plot for mean and main effects plot for signal-to-noise ratios, are the outputs of the Taguchi analysis.

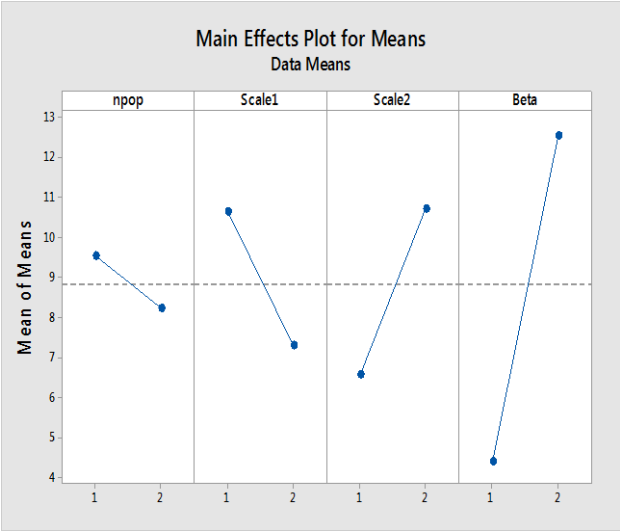

Fig. 3: Main effects plot for means.

According to Fig. 3 and in order to achieve the optimal solution, *npop*, and $Scale_1$ should be at a high level and $Scale_2$, and *Beta* should be at a low level.

These answers are definitive if they match the main effects plot for signal-to-noise ratios. This plot is shown in Fig. 4.

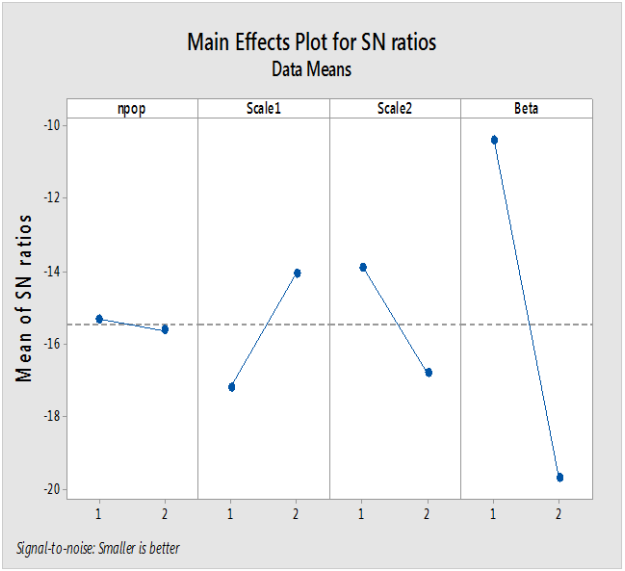

Fig. 4: Main effects plot for signal-to-noise ratios.

Due to the above figure, the results for $Scale_1$, $Scale_2$ and *Beta* parameters are consistent with Fig. 3; the maximum amount of signal-to-noise ratio occurs when $Scale_1$ is at a high level, and $Scale_2$ and *Beta* are at a low level.

But two obtained plots for *npop* do not match because the maximum amount of signal-to-noise ratio happens when this parameter is at a low level. So, the optimal levels for $Scale_1$, $Scale_2$ and *Beta* are the high level of them which are 0.9999, 0.9002 and 6, respectively.

In order to evaluate the performance of the proposed ensemble classifier with optimal levels of parameters, simulations have been done in two modes, i.e., optimal levels mode and empirical values mode. Obtained results are reported in Table 5.

Optimal values used in this part are the high levels of $Scale_1$, $Scale_2$ and *Beta*. Empirical values, which used in the second mode, are as the following:

npop: 20
MaxIt: 200
C_1: 0.7184
C_2: 2.7613
$Shift_1$: 72.4684
$Shift_2$: 188.5077
$Scale_1$: 0.035
$Scale_2$: 0.8245
Alpha: 0.1
Beta: 4
Gamma: 2

Table 5: Obtained comparative results of objective functions in two different modes of parameters values

Data	First Mode (Optimal levels of parameters)			Second Mode (Empirical values of parameters)		
	Ensemble Size	Average of Accuracy	Average of Reliability	Ensemble Size	Average of Accuracy	Average of Reliability
Glass	13	23	20	**8**	29	11
	96.75	**98.07**	97.43	94.48	96.41	94.85
	95.46	96.75	**97.43**	93.87	94.48	94.85

In the above Table, reported values in the columns of ensemble size, average of accuracy, and average of reliability are related to the points of the Pareto front with the best ensemble size, the best average of accuracy, and the best average of reliability. In addition, the values of the first, second, and third rows indicate ensemble size, an average of accuracy, and an average of reliability related to each point of the Pareto front, respectively.

Due to these results, when using optimal levels of parameters, the average of accuracy and the average of reliability have been improved. Only ensemble size has a better amount in the empirical mode, but in this situation, the values for two other objective functions are better with optimal levels of parameters. It should be noted that low differences in two modes relate to the fact that empirical values are extracted with trial and error to achieve the best results, and they are available from previous works. However, this process is time-consuming and has no guarantee to get optimal levels of parameters.

On the other hand, in general, these empirical values are not available.

Results and Discussion

One of the advantages of the proposed approach in comparison with previous works is that more parameters can be analyzed with less computational costs; checking the impact of these 11 parameters by the approaches of [13] or [19] is very complicated and time-consuming. Also, the proposed approach of this paper can optimize the value of the important parameters but the other works cannot do this. However, Plackett–Burman method unlike [13] and [19] don't consider the interactions and only main effects are studied in this method.

Conclusion

One of the important issues in the field of heuristic ensemble classifiers is the stability of these classifiers.

This topic is important due to the random nature of the heuristic algorithms. This paper has reviewed this issue with a statistical perspective; in addition to evaluating stability, important and effective parameters are detected.

Also, by using the Taguchi design in Minitab software, it is possible to determine the optimal levels for important parameters. Using these optimal levels will make the output better than the empirical mode. It should be noted that empirical values are obtained using the trial and error method. Using new methods of stability investigation is one of the suggestions for the future works.

Author Contributions

Z.K. Pourtaheri performed the simulations, interpreted the results and wrote all parts of the manuscript.

Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy have been completely observed by the authors.

Abbreviations

MOIPO	Multi-Objective Inclined Planes Optimization
DoE	Design of Experiments
OFAT	One Factor At a Time
SNR	Signal to Noise Ratio
GD	Generational Distance
SP	Spacing metric
MID	Mean Ideal Distance
IPO	Inclined Planes Optimization

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Biographies

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Research paper

Action Change Detection in Video Based on HOG

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Abstract

Background and Objectives: Action recognition, as the processes of labeling an unknown action of a query video, is a challenging problem, due to the event complexity, variations in imaging conditions, and intra- and inter-individual action-variability. A number of solutions proposed to solve action recognition problem. Many of these frameworks suppose that each video sequence includes only one action class. Therefore, we need to break down a video sequence into sub-sequences, each containing only a single action class.
Methods: In this paper, we develop an unsupervised action change detection method to detect the time of actions change, without classifying the actions. In this method, a silhouette-based framework will be used for action representation. This representation uses xt patterns. The xt pattern is a selected frame of xty volume. This volume is achieved by rotating the traditional space-time volume and displacing its axes. In xty volume, each frame consists of two axes (x) and time (t), and y value specifies the frame number.
Results: To test the performance of the proposed method, we created 105 artificial videos using the Weizmann dataset, as well as time-continuous camera-captured video. The experiments have been conducted on this dataset. The precision of the proposed method was 98.13% and the recall was 100%.
Conclusion: The proposed unsupervised approach can detect action changes with a high precision. Therefore, it can be useful in combination with an action recognition method for designing an integrated action recognition system.

Introduction

Human operators cannot be able to manage the enormous volumes of videos that are generated by network cameras. Therefore, it is important to develop efficient and effectual automatic methods to analyze video data [1].

Action recognition problem is defined as follows: "given a dictionary of annotated training action videos, recognize the unknown action of a query video" [2]. In the other words, first, a dictionary of labeled training data, such as walking, running, and jumping videos are given. After an unknown action video is fed to the system, the action recognition part analyzes the unknown action based on the given videos and declares the action label.

Action recognition has various interesting applications in many areas. Some of these applications are indoor and outdoor video surveillance, wildlife monitoring, human-computer interaction [1], the human health system, sign language, virtual reality, and humanoid robot [3]. Despite a significant effort, the action recognition is still a challenging problem. The main challenges in this area are variety and complexity of the

events that may occur in a video (e.g., clutter, and occlusions), variations in the imaging conditions (e.g., illumination, viewpoint, and resolution) and different appearance from the same action that did by different people [1].

There are two basic components in action recognition: action representation and action classification.

Some successful action representations are based on motion models, shape models, interest point models, dynamic models and Geometric human body models.

In Motion models to distinguish between actions, dynamic characteristics of actions are important and motion features should be extracted. Motion models may be affected by background motion. Weng and Guan [4] proposed stacked trajectory energy image (STEI) method. In this method, trajectories are extracted from motion saliency regions. In their research, a three-stream CNN framework is proposed to simultaneously capture spatial, temporal and global motion information of the action from RGB frames, optical flow, and STEI. Wang et al. [5] proposed a method that utilized dense trajectories to describe actions. The main idea of their research is to densely sample feature points in each frame, and track them in the video based on optical flow.

In shape models, features are extracted from a shape, which is silhouette of the tracked object. A sequence of these silhouettes forms a silhouette tunnel, i.e., a spatiotemporal binary mask that it shows the deformation of the moving object over time. A silhouette tunnel is desirable for action recognition because of being insensitive to color, texture, and contrast changes. Silhouette tunnels are also known as object tunnels [6], [7], activity tubes [8] and space-time volumes (STVs)[9]. Vishwakarma and Kapoor [10] have used space-time volume to action recognition. Amraji et al. [11] presented a method in which the shape represented using Fourier Descriptors (FDs) as features. They used Principal Component Analysis (PCA) to project these features into Eigen-space. Then, the KNN classifier is used. In Bobick and Davis [12] research, the basis of the action representation is a temporal template. They proposed a motion energy image (MEI), that indicating the presence of motion, and motion history image (MHI), that is a scalar field depicting the recency of motion in a sequence. Sharif et al. [13] proposed a human action recognition method based on statistical weighted segmentation (SWS) and feature selection approach. Their proposed technique is comprised of two primary steps: a) Efficient human segmentation from video sequences, and b) Features extraction, fusion and finally selection of most robust features. The authors of [14] presented a method to recognize human actions. They used Histograms of Oriented Gradients (HOG) for human pose representations. In [15], human activities are recognized using background subtraction, HOG features and Back-Propagation Neural Network (BPNN) classifier. In this approach, background estimation is performed at first, using mean filter to obtain the background and areas of the image containing important information. Afterwards, in order to extract features to describe human motion, a histogram of oriented gradients (HOG) descriptor is used, with the idea that local shape information can be completely described by intensity gradients or edge directions. Finally, a BPNN is used to perform the final classification. Khan et al. [16] proposed a framework that primarily consolidated four phases: a) acquisition and preprocessing, b) frame segmentation which incorporates top-hat and bottom-hat filters along with the proposed RGB* color space enhancement, c) features extraction and dimensionality reduction, and d) classification using SVM classifier. Dalal and Triggs [17] used HOG descriptors for extracting feature sets to human detection and linear SVM for classification. The accuracy of shape models is highly related to the quality of silhouettes.

Interest points, e.g., corners, etc., are sufficiently discriminative and are usually far fewer than the number of pixels in a video sequence. Zhu et al. [18], evaluated the spatio-temporal interest point (STIP) based features for depth-based action recognition. Niebles et al. [19] used 2D Gaussian and 1D Gabor filters to find local region of interest in the cuboids of space and time. Zhang et al.[20] , proposed manifold regularized Sparse Representation (MRSR). In this approach, each interest point is represented by its local closest words. MRSR has an analytical solution and is easy to calculate. Khan et al. [21], proposed a new method for action recognition by fusion of deep neural network (DNN) and multi view features. In this method, both types of features are fused in serial approach, and selection of best among them is done through three parameters i.e. relative entropy, mutual information, and strong correlation. Later, all these parameters are combined by employing a mean parallel fusion approach, and help in designing a high probability based threshold function to select the best features. These features are finally provided into Naïve Bayes classifiers for final recognition. Nazar et al. [22] have used CNN based features and classical features in a parallel processing. The best of them were selected before fusion stage. At the end, the labeled data is returned as an output by using classifier. Arshad et al. [23] proposed a technique that works in two phases: a) two pre-trained CNN models are applied and their information is fused via a parallel approach. In the proposed parallel fusion approach, both feature vectors are compared with each other and a strongly correlated

feature is added into a fused matrix. b) Entropy and skewness vectors are calculated from the fused matrix. The best subsets of picked features are finally fed to multiple classifiers and finest one is chosen based on accuracy value.

Dynamic model's general idea is to define each static posture of an action as a state, and describe the dynamics (temporal variations) of the action by using a state-space transition model. An action is modeled as a set of states and connections in the state space using a Dynamic Bayesian Network (DBN). Hidden Markov Model (HMM) is proven to be a special type of DBN with a fixed structure of inference graph to model time variations of data features [2] directly. The basic human interactions are modeled by coupled hidden Markov models (CHMMs) [24]. In this model, multiple state variables of CHMMs are temporally corresponded to the conditional probabilities of one chain given the other chain. The interval temporal Bayesian network (ITBN), a graphical model has been proposed by Zhang et al. [25] to model the temporal dependencies over time intervals. This model has been developed the Bayesian network by the interval algebra.

In geometric human body model, the pose of human body must first be estimated to recognize human action using this approach. Although all these techniques have promising results, but they have a huge limitation, and it is the extraction of human body model and body joint points. The recent advanced cost-effective depth cameras help in the extraction of human body joint points, but depth cameras also have some limitations. First, the range of the depth sensor is limited; Second, skeleton tracking and the estimated 3D joint positions are noisy and can produce inaccurate results or even fails when serious occlusion occurs [26]. The human body modeling is done in 3D and 2D methods. The 3D methods [27, 28] generally perform better than 2D methods, because the 3D methods exploit all the views to evaluate a query action, unlike the reported 2D methods which are limited to a single-view testing. 3D methods usually have higher computational complexities than 2D models and they are not suitable for real-time applications [29]. Das et al. [30] have achieved good results by combining skeleton information and apparent features. Liu and Wang [31] proposed an action representation method named Part Movement Model (PMM), which captures the spatial-temporal structure of human actions and divides the actions into discriminative part movements.

The algorithms used to classify human action so far, are generally be categorized as dynamic time warping (DTW), generative models, discriminative models and others such as Kalman filter, binary tree, Kernel-based and k-nearest neighbors (KNN). The dynamic time warping (DTW) [32] is a method for similarity measure in order to compare two temporal sequences. DTW is simple, but it is not appropriate for a large number of classes with many variations. Some generative models (dynamic classifiers) are proposed such as Hidden Markov Models (HMM) [3]. Shian-Ru Ke [33] uses three-dimensional modeling of the body and HMM classification algorithm. The discriminative models (static classifications) such as SVMs and artificial neural networks (ANNs) [34] can also be used at the action classification. Hoai et al. [35] proposed a method that simultaneously performs video segmentation and action recognition using a multi-class SVM framework and the dynamic programming. Vishwakarma and Rajiv [10] recognized actions using space-time and SVM-NN classification algorithms.

The performance of both generative and discriminative models relies on extensive training dataset. Therefore, other methods such as Kalman filter, binary tree, multidimensional indexing, and k-nearest neighbors (KNN) were proposed to comprise this problem [3]. As the result, different classification algorithms usually require different sets of suitable feature representations [2].

Many of frameworks that proposed to solve action recognition problem, suppose that each video sequence includes only one action class. Therefore, we need to break down a video sequence into sub-sequences, each containing only a single action class. In this paper, we focus on the specific problem of action change detection, i.e., identifying when one action stops and another action begin. Even if action representation is established and even if action comparison metric is known, it is still unclear to what segment of a video should both be applied? Action change detection segments a video into temporal boundaries, which no action change occurs in them, thus action representation is meaningful. This Partitioning, by counting the number of occurrences of each action class, can be useful for applications such as robotics, patient monitoring and athlete monitoring in sports centers.

As mentioned by Guo [2] "finding these temporal action boundaries is akin to scene cut detection in video, but in the space of actions".

The detection of abrupt changes is a classical topic that has been studied in the past few decades [36]. It has been utilized in many areas, such as quality control, time series signal analysis, fault detection and monitoring, etc. [2]. In this paper, we propose an unsupervised action change detection method and introduce a new action representation based on the object silhouette sequence. We introduce a new representation of actions by displacing the axes and rotating the usual space-time volume. In this new

volume, each frame consists of two axes x and t which are correspond to height and width axes of that frame.

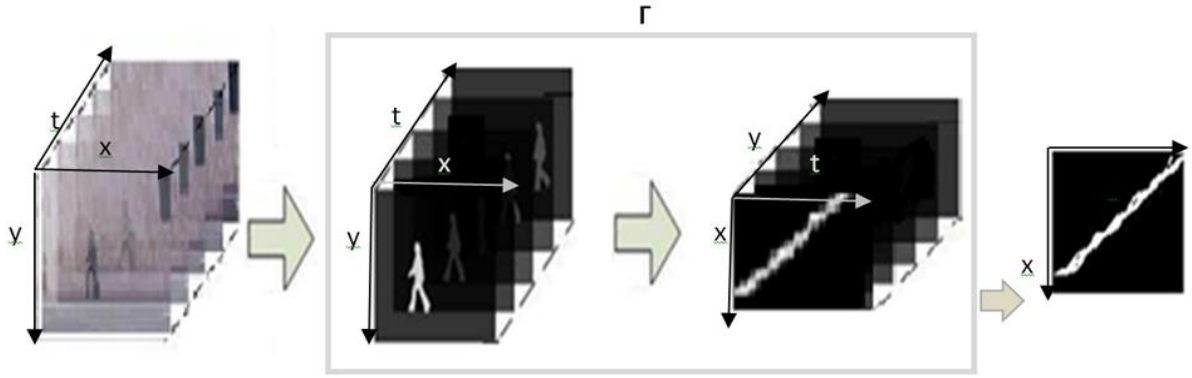

Fig. 2: An xt pattern extraction- Operator Γ shows rotating traditional space-time volume and displacing its axes.

In addition, y value specifies the frame number. It is show that this representation is not sensitive to silhouette noises, holes, and missing parts.

We created 105 artificial videos using the Weizmann dataset [37] to test the performance of the proposed method. There are 105 video segments with one action change, and 858 video segments without any action changes. Experimental results show 0% false negative error and 0.0023% false positive error. Therefore, the recall of our method is 100% and the precision of this method is 98.13%.

The rest of the paper is organized as follows. Next section reviews related works in action change detection. Proposed framework section describes the proposed action change detection method. Experimental results are reported in Results and Discussion section and concluding is presented in Conclusion section.

Related Works

In Guo et al. method [2], first, the silhouette sequence of video is broken into a sequence of overlapping N-frame-long action. For each point $s_0 = (x_0, y_0, t_0)^T$ into an N-frame action segment of silhouette tunnel a 13-dimensional feature vector is associated: three position features x_0, y_0, t_0, and ten shape features. The shape features are the distances between the point s_0 and the tunnel boundaries along the ten different spatio-temporal directions. Finally, a simplified representation for the shape of the silhouette tunnel will be obtained [38]. Next, a distance measure is defined to evaluate the similarity between any two consecutive action segments. The distribution of the pair-wise distance among in previous (T-1) segments is formulated using kernel density estimation. Lastly, a binary decision determines whether the segments S_1; S_2; . . . ; S_{T_1} and the segment S_T have continuous actions or not [2].

In order to measure the performance of this approach, they created 9 single person multi-action test video sequences. They used the segments of length for action comparison with a 4-frame overlap.

A judicious selection of these parameters is essential for the performance of their algorithm. It should be long enough to capture salient characteristics of an action, and to span only one single action. The precision of detected action boundaries depends on the length of action segments. Clearly, a large segment length increases the uncertainty of action boundary location. The total number of action segments is 597. 61 segments have action changes and 536 segments do not. The proposed action change detection method produces percent false negative error 1.64% and percent false positive error 0.19%.

Proposed Framework

Our framework for action change detection is based on the silhouette sequence of a deforming object. We produce silhouette sequence by using simple background subtraction techniques [39]. For example, three frames from a “two hands waving” action sequence and corresponding silhouettes from the Weizmann human action database [37] are shown in Fig.1. In this example, person is the foreground of the image and its corresponding pixels have a value equal to one (white).The pixels of background have a value equal to zero (black).

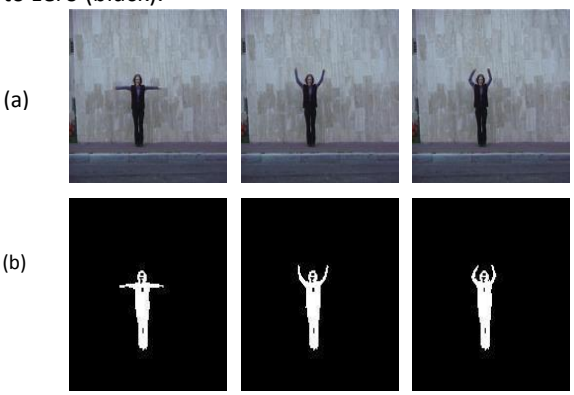

Fig. 1: Human action sequence. Three frames from (a) two hands waving action sequence and (b) corresponding silhouettes from the Weizmann human action database.

As shown in Fig. 2 instead of using the traditional space-time volume, a new representation is proposed by rotating this volume and displacing its axes. In the new volume, each frame point is localized by **x** and **t**, where **x** is the horizontal axes, like before, and **t** shows vertical axes now. In this volume, y values show frame number. The **xty** volume is a new representation of the traditional space-time volume.

To display an M * N frame, we use a two-dimensional array (matrix) with M rows and N columns .The value of each element of this array indicates the brightness of the frame at that point. This value can be zero or one in a binary image. The number of pixels with a value of one is the brightness of a frame .In the new volume, we select the highest brightness frame, as our suggested pattern. These patterns are similar together for each action. In these patterns, the silhouette sequence is condensed into a binary image. Therefore, it can represent motion sequence in a compact manner. In fact the silhouette sequence is condensed into a gray scale image. The quality of Silhouette tunnels is highly related to the correctness of background subtraction algorithms and the precise segmentation is very difficult to obtain in real world videos. Fig. 3 demonstrates an action sequence of "jumping-jack", which is chosen from the Weizmann human action database. As its corresponding xt pattern shows, this representation is not so sensitive to silhouette noise, holes, and missing parts.

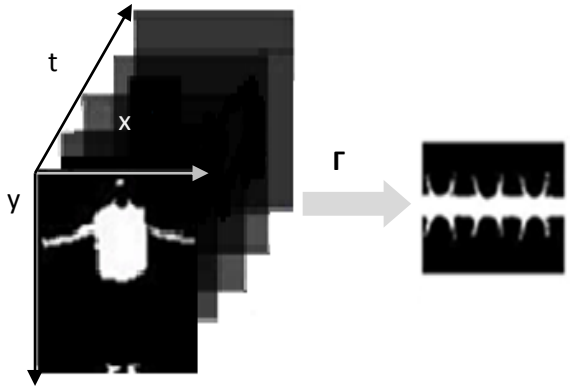

Fig. 3: The xt pattern is not sensitive to silhouette noise, holes, and missing parts.

Fig. 4 demonstrates several another examples of selected xt pasterns for different actions from the Weizmann human action database. The action sequences are "jumping- jack", "pjump" and "wave1". As their corresponding xt patterns show, these pasterns are completely different for different actions, so in proposed method, we work with this image data rather than silhouettes sequence.

If the action change occurs, the resulting pattern changes from a cross-sectional one. This cross- sectional shows the time of action change. Fig. 5, demonstrates several examples of the generated patterns that have action change (1: "wave-one- hand" to "wave-two-hands". 2: "Run" to "wave-two-hands". 3: "Run" to "jumping-jack". 4: "Run" to "walk").

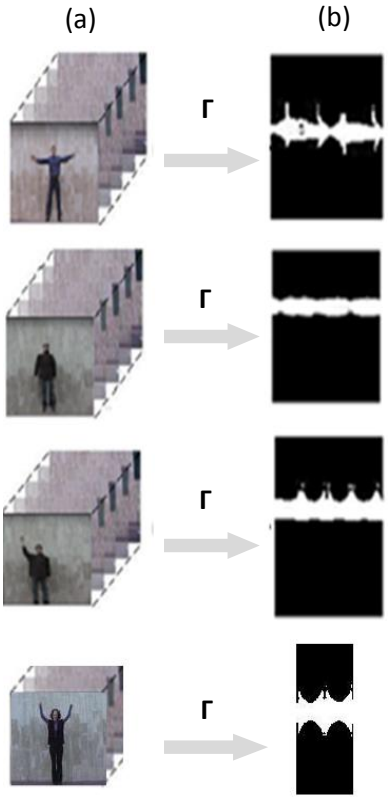

Fig. 4: Some examples of xt pattern obtained for different actions. (a) jumping-jack, pjump, wave1 and wave2 action sequences, from the Weizmann human action database. (b) Corresponding xt patterns.

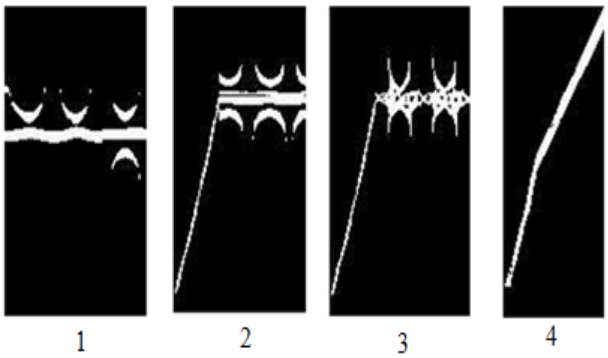

Fig. 5: Several examples of the generated patterns of videos that have action change. 1: "wave-one- hand" to "wave-two-hands". 2: "Run" to "wave-two-hands". 3: "Run" to "jumping-jack". 4: "Run" to "walk".

In order to find this cross-sectional, we use the histogram of oriented gradients (HOG) [17] feature vector. HOG describe appearance and shape by the distribution of intensity gradients or edge directions. We use the features = extractHOGFeatures(I) function in

MATLAB that extracts HOG features from an image I and returns the features in a 1-by-N vector. These features encode local shape information from regions within an image. The process of our method for action change detection can be summarized as follows:

The xt pattern is extracted from the xty volume. This pattern is splitted into several equal parts. The HOG feature vector is calculated for each part. The difference of the HOG feature of both consecutive parts (e.g. 1 and 2, 2 and 3 ...) is calculated by (1):

$$Dif = \sum_{i=1}^{SV} \left| HOG\_F_{P}[i] - HOG\_F_{P-1}[i] \right| \quad (1)$$

where, p is the part's number. HOG_F is the HOG feature vector and SV is the length of this vector. i is the index of each cell of HOG_F

All steps are repeated for the two parts that have the most difference value, i.e. they have the most difference in appearance

.If this maximum value is zero, the repeat is finished. At final, considering that each frame point is localized by x and t, the line that halves the last two parts represents the time that action change occurred.

The algorithm1 describes the proposed method for finding the part in which action has changed:

Algorithm1: Proposed algorithm for finding the part in which action has changed.

1. **Input**: A video sequence
2. **Output**: XT //the part in which action has changed.
3. XT= xt pattern of input video;
4. **While** XT
5. Split XT into several equal parts;
6. HOG_F:= Ø;
7. D: = Ø;
8. **for** P=1 to P ≤ NumberOf Parts; P++ do
9. F: = extractHOGFeatures (part of p);
10. Add F to HOG_F;
11. **if** (P>=2)
12. Dif= sum (abs (HOG_F (P) - HOG_F (P-1)));
13. Add Dif to D;
14. **end for**
15. MaxValue= maximum value of D Array;
16. **if** MaxValue > 0
17. XT:= part MaxIndex and part MaxIndex+1 of XT;
18. **else** break;
19. **end**

Results and Discussion

The proposed method implemented using MATLAB (R2015a) software in a Windows 8 operating system and a computer system with dual-core Intel Core-i7 processor and 8 GB RAM. In order to test the performance of the proposed method, we conducted a series of experiments based on ground-truth synthetic data as well as a time-continuous camera captured video. In the ground-truth experiment, we used the Weizmann dataset. We created 105 test video sequences. The database contains 90 low-resolution videos and silhouette sequences (180×144 pixels) that show 9 different people each performing 10 different actions, such as jumping, walking, running, skipping, etc. Some action examples are shown in Fig. 6.

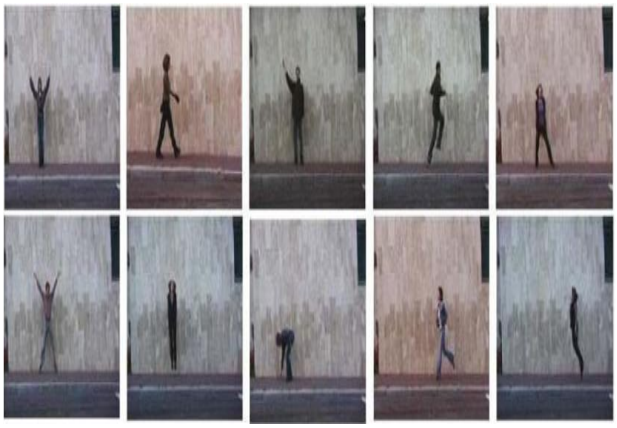

Fig. 6: Action examples from Weizmann dataset (wave2, walk, wave1, skip, side, jack, p-jump, bend, run and jump).

We use Precision and Recall for experimental evaluation of the proposed method. These measures can be calculated by (2) and (3):

$$\text{Recall} = \frac{\text{TP}}{\text{TP} + FN} \times 100\,, \quad (2)$$

$$\text{Precision} = \frac{\text{TP}}{\text{TP} + FP} \times 100, \quad (3)$$

where, TP is the true positive action change detection number. FP is the false positive action change detection number. False positive errors occur when a segment without any action change are classified as a segment with the action change. FN is the false negative action change detection number. False negative errors occur when a segment with the action change are classified as a segment without any action change. These functions are multiply to 100 to explain Precision and Recall in the percent measure.

To compare the results with the Guo's method [2], we assume generated video sequences as segments of length $N = 8$. There are 105 video segments with one

action change, and 858 video segments without any action changes. In Fig. 7, results of the proposed method on some sample video sequences are demonstrated.

The blue line indicates the detected time of action change by the proposed method.

As demonstrated in this figure, there is not any blue line in xt patterns of "Wave2", "pjump", "bend" and "jack", because action change doesn't occur.

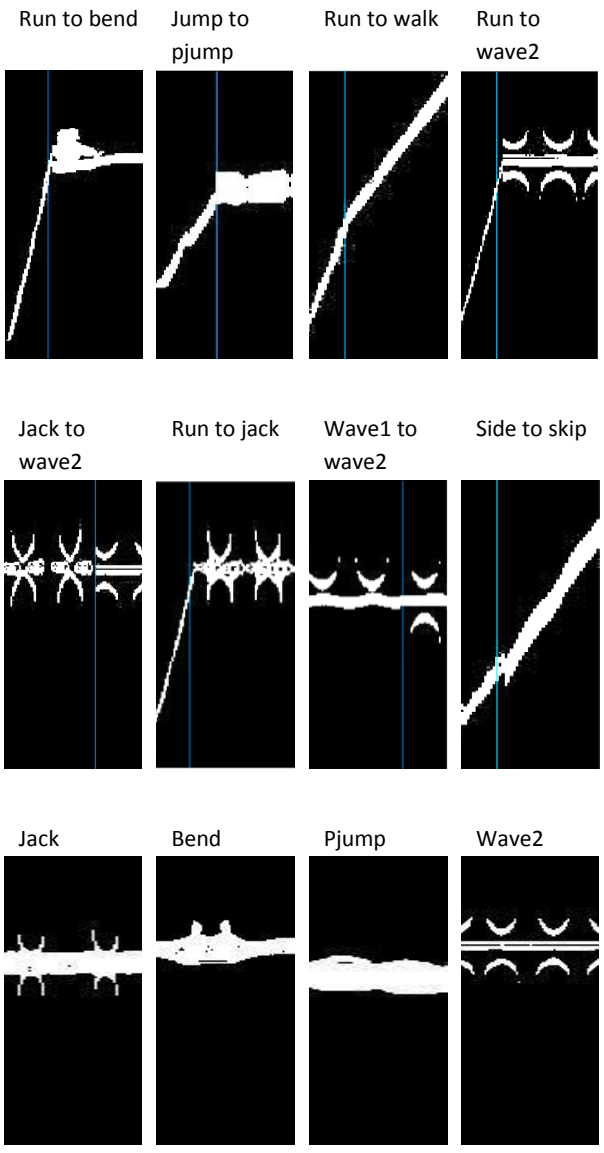

Fig 7: The results of the proposed method on some sample video sequence. The blue line indicates the action change detected time of the proposed method.

In the results of all video segments, there were two false positive errors as shown in Fig. 8.

In this figure there are blue lines in xt patterns of "jumping-jack" and "bend" but have not occurred any action change really.

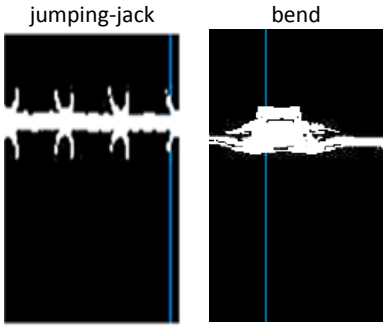

Fig. 8: False action change detection of the proposed method.

The proposed action change detection method produces 0% false negative error rate (PFN) and 0.0023% percent false positive error rate (PFP). Therefore, the recall of our method is 100% and precision of this method is 98.13%.

Table 1 shows efficacy of parameter P (number of parts) on precision of the proposed method. In general, the precision decreases with increasing P. Of course, there is a slight increase in P = 5 compared to P = 4. The precision of our method with P=4 is 77.78% and with P=5 is 78.4%. .The difference in HOG feature for very small parts is zero; therefore for P≥7 this algorithm hasn't good performance. Based on these results, this method has the best performance with P=3.

Table 1: Efficacy of parameter P on precision of the proposed method

P(number of parts)	precision of the proposed method
3	98.13%
4	77.78%
5	78.4%
6	66.68

Conclusion

The goal of action change detection is to partition a video into many sub-videos so that each of them contains only one single action. In this paper, we proposed a new approach to unsupervised action change detection in a video sequence. The proposed approach can automatically detect action changes without reference to labeled data. We introduced a new action representation method called xt pattern. The xt pattern is a selected frame of the xty volume. This volume is achieved by the proposed rotation of the space-time volume. A frame of this volume, with the most brightness, is our chosen pattern. These patterns are the same for each action and represents action sequence in a compact manner. In fact the silhouette sequence is condensed into a gray scale image. This representation is not so sensitive to silhouette noise, holes, and missing parts.

We created 105 test video sequences using the Weizmann dataset. Our experimental results indicate action boundary detection accuracy with PFN = 0% and PFP = 0.0023%. As mentioned, the proposed unsupervised approach can detect action changes with a high precision. Therefore, it can be useful in combination with an action recognition method for designing an integrated action recognition system.

In this research, we used the HOG feature. Given that the difference in HOG feature for very small parts is zero, proposition a more efficient algorithm to extract the feature of the xt pattern can increase the accuracy. In the future, it would be desirable to work on designing an integrated action recognition system using our action change detection method and an action recognition method.

Author Contributions

M. Fakhredanesh proposed the main idea of the innovation of the paper and designed road map of the research. M. Fakhredanesh and S. Roostaie designed the experiments and S. Roostaie implemented the experiments. M. Fakhredanesh carried out the data analysis.

Conflict of Interest

The author declares that there is no conflict of interest regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancy has been completely observed by the authors.

Abbreviations

Γ	Rotating traditional space-time volume and displacing its axes.
Xt	The xt pattern is a selected frame of xty volume.
xty.	The xty volume is achieved by rotating the xyt space-time volume and displacing its axes
STEI	Stacked trajectory energy image
STV	Space-time volumes
FD	Fourier Descriptor
MEI	Motion energy image
MHI.	Motion history image
SWS	Statistical weighted segmentation
$BPNN$	Back-Propagation Neural Network
DNN	deep neural network
STIP	Spatio-temporal interest point
MRSR	Manifold regularized Sparse Representation
DBN	Dynamic Bayesian Network
HMM	Hidden Markov Model
CHMMs	Coupled hidden Markov models
ITBN	Interval temporal Bayesian network
DTW	Dynamic time warping
ANNs	Artificial neural networks
PMM	Part Movement Model
S_T	Tth action segment
PFN	False negative error rate
PFP	False positive error rate
P	Number of parts
HOG_F	The HOG feature vector
SV	The length of the HOG feature vector
i	The index of each cell of the HOG feature vector
TP	True positive
FP	False positive
FN	False negative

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Biographies

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Abstract

Background and Objectives: This section should be the shortest part of the abstract and should very briefly outline the following information: 1-What is already known about the subject, related to the paper in question. 2- What is not known about the subject and hence what the study intended to examine (or what the paper seeks to present). In most cases, the background can be framed in just 2–3 sentences, with each sentence describing a different aspect of the information referred to above; sometimes, even a single sentence may suffice. The purpose of the background, as the word itself indicates, is to provide the reader with a background to the study, and hence to smoothly lead into a description of the methods employed in the investigation.

Methods: The methods section is usually the second-longest section in the abstract. It should contain enough information to enable the reader to understand what was done, and how.

Results: The results section is the most important part of the abstract and nothing should compromise its range and quality. This is because readers who peruse an abstract do so to learn about the findings of the study. The results section should therefore be the longest part of the abstract and should contain as much detail about the findings as the journal word count permits.

Conclusion: This section should contain the most important take-home message of the study, expressed in a few precisely worded sentences. Usually, the finding highlighted here relates to the primary outcome measure; however, other important or unexpected findings should also be mentioned. It is also customary, but not essential, for the authors to express an opinion about the theoretical or practical implications of the findings, or the importance of their findings for the field. Thus, the conclusions may contain three elements: 1- The primary take-home message 2-The additional findings of importance 3-The perspective.

Introduction

This document provides an example of the desired layout for JECEI paper and can be used as a template for Microsoft Word versions 2003 and later. It contains information regarding desktop publishing format, type sizes, and typefaces. Style rules are provided to explain how to handle equations, units, figures, tables, abbreviations, and acronyms. Sections are also devoted to the preparation of appendixes, acknowledgments, references, and authors' biographies. For additional information including electronic file requirements for text and graphics, please refer to www.autjournal.com.

Doi:

Technical Work Preparation

Please use automatic hyphenation and check your spelling. Additionally, be sure your sentences are complete and that there is continuity within your paragraphs. Check the numbering of your graphics and make sure that all appropriate references are included.

A. Template

This document may be used as a template for preparing your technical work.

B. Format

If you choose not to use this document as a template, prepare your technical work in single-spaced, double-column format, on paper 21.6×27.9 centimeters (8.5×11 inches or 51×66 picas). Set top and bottom margins to 25 millimeters (0.98 inch) and left and right margins to about 20 millimeters (0.79 inch). Do not violate margins (i.e., text, tables, figures, and equations may not extend into the margins). The column width is 82 millimeters (3.2 inches). The space between the two columns is 6 millimeters (0.24 inch). Paragraph indentation is 4.2 millimeters (0.17 inch). Use full justification. Use either one or two spaces between sections, and between text and tables or figures, to adjust the column length.

C. Typefaces and Sizes

Please use a proportional serif typeface such as Calibri and embed all fonts. Table 1 provides samples of the appropriate type sizes and styles to use.

D. Section Headings

A primary section heading is enumerated by a Roman numeral followed by a period and is centered above the text. A primary heading should be in capital letters.

A secondary section heading is enumerated by a capital letter followed by a period and is flush left above the section. The first letter of each important word is capitalized and the heading is italicized.

A tertiary section heading is enumerated by an Arabic numeral followed by a parenthesis. It is indented and is followed by a colon. The first letter of each important word is capitalized and the heading is italicized.

A quaternary section heading is rarely necessary, but is perfectly acceptable if required. It is enumerated by a lowercase letter followed by a parenthesis. It is indented and is followed by a colon. Only the first letter of the heading is capitalized and the heading is italicized.

E. Figures and Tables

Figure axis labels are often a source of confusion. Try to use words rather than symbols. As an example, write the quantity "Magnetization," or "Magnetization, *M*," not just "*M*." Put units in parentheses. Do not label axes only with units. As in Fig. 1, write "Magnetization (kA/m)" or "Magnetization (kA·m^{-1})," not just "kA/m." Do not label axes with a ratio of quantities and units. For example, write "Temperature (K)," not "Temperature/K." Figure labels should be legible, approximately 8- to 10-point type.

Large figures and tables may span both columns, but may not extend into the page margins. Arrange these one column figures and tables at either top or end of a page, or at the end of the paper right before the references. Figure captions should be below the figures; table captions should be above the tables. Do not put captions in "text boxes" linked to the figures. Do not put borders around your figures. Use Insert | Reference | Caption to number your tables and figures, and use Insert | Reference | Cross- reference to refer to their numbers.

Table 1: Samples of Calibri sizes and styles used for formatting a pes technical work

Point Size	Purpose in Paper	Special Appearance
9	Table text, figure text footnotes, subscripts, superscripts, references, bio, Figure caption, keywords	Table Title
10	Body text, equations, author affiliation, abstract	*Subheadings*
11		**Section Titles**
12	***Author Name***	

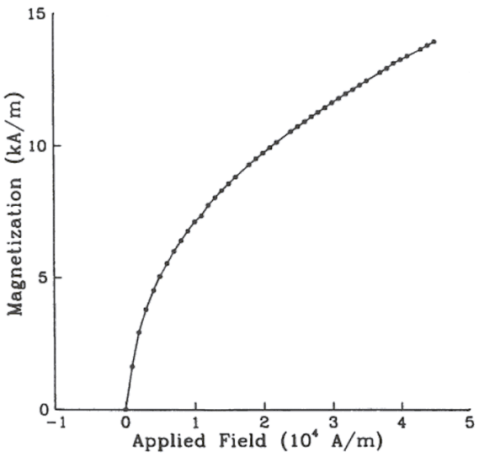


Fig. 1: Magnetization as a function of applied field. (Note that there is a colon after the figure number followed by two spaces.)

All figures and tables must appear near, but not before, their first mention in the text. Use the abbreviation "Fig. 1," even at the beginning of a sentence.

To insert images in Word, use Insert | Picture | From File.

F. Numbering

Number reference citations consecutively in square

brackets [1]. The sentence punctuation follows the brackets [2]. Multiple references [2], [3] are each numbered with separate brackets [1][1]-[2]. Refer simply to the reference number, as in [2]. Do not use "Ref. [2]" or "reference [2]" except at the beginning of a sentence: "Reference [2] shows…."

Number footnotes separately with superscripts (Insert | Footnote). Place the actual footnote at the bottom of the column in which it is cited. Do not put footnotes in the reference list. Use letters for table footnotes.

Use Arabic numerals for figures and Roman numerals for tables. Appendix figures and tables should be numbered consecutively with the figures and tables appearing in the rest of the paper. They should not have their own numbering system.

G. Units

Metric units are preferred for use in IEEE publications in light of their global readership and the inherent convenience of these units in many fields. In particular, the use of the International System of Units is advocated. This system includes a subsystem of units based on the meter, kilogram, second, and ampere (MKSA). British units may be used as secondary units (in parentheses). An exception is when British units are used as identifiers in trade, such as 3.5-inch disk drive.

H. Math and Equations

Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). First use the equation editor to create the equation. Then select the "Equation" markup style. Write the equation number in parentheses using Insert | Caption.

Use the Microsoft Equation Editor for all math objects in your paper (Insert | Object | Create New | Microsoft Equation *or* MathType Equation). "Float over text" should *not* be selected.

To make your equations more compact, you may use the slash (/), the exp function, or appropriate exponents. Italicize Roman symbols for quantities and variables, but not Greek symbols. Use a long dash rather than a hyphen for a minus sign. Use parentheses to avoid ambiguities in denominators. Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). Be sure that the symbols in your equation have been defined before the equation appears or immediately following. Italicize symbols (*T* might refer to temperature, but T is the unit Tesla).

Use Insert | Reference | Caption to number equations. Refer to "(1)," not "Eq. 1" or "equation (1)," except at the beginning of a sentence: "Equation (1) is ...". Punctuate equations when they are part of a sentence, as in

$$\int_0^{r_2} F(r,\varphi)\, dr\, d\varphi = [\sigma r_2 / (2\mu_0)] \cdot \int_0^{\infty} \exp(-\lambda\,|\,z_j - z_i\,|)\,\lambda^{-1}\, J_1(\lambda r_2)\, J_0(\lambda r_i)\, d\lambda \quad (1)$$

Use two column tables to locate equations and their numbers properly in one line, as follows:

$$I_F = I_B = -I_C = A^2 I_{A1} + A I_{A2} + I_{A0} = \frac{-J\sqrt{3}E_A}{Z_1 + Z_2} \quad (2)$$

where I_F is the fault current. Be sure that the border is off.

Results and Discussion

The Results section should briefly present the experimental data in text, tables or figures. Tables and figures should not be described extensively in the text.

The Discussion should focus on the interpretation and the significance of the findings with concise objective comments that describe their relation to other work in the area. It should not repeat information in the results. The final paragraph should highlight the main conclusion(s), and provide some indication of the direction future research should take.

Conclusion

As the Conclusion section is the most important element of a manuscript, so it must be more expanded scientifically and contently at least half a page length.

Example:

In this study, a forecast model was developed to determine the generation of MSW in the municipalities of the CCS, Chiapas State, Mexico. A MLR was used to obtain the forecast model with social and demographic explanatory variables. Two forecast models were presented and analyzed, with variables that met the multicollinearity test. The most important variables to predict the rate of MSW generation in the study area were the population of each municipality (XPop), the population born in another municipality (XPbam) and the population density (XPd). XPop is the most influential explanatory variable of waste generation, particularly it is related in a positive way. XPbam is less related to waste generation. XPd is the variable that least influences waste generation prediction; in addition, it can present problems of correlation with other explanatory variables. Although other variables, such as daily per capita income (XDpi) and average schooling (XAs), are very important, they do not seem to have an effect on the response variable in this study. The user of this forecast model should use model 2, since it is the one with the highest parsimony (it uses fewer variables); R^2_{adj}, MAPE, MAD and RMSE values indicated high influence on the explained phenomenon and high forecasting capacity. Additionally, it is important to mention that when using the models proposed for forecasting purposes, it is necessary to make a

transformation in the explanatory and response variables (use inverse of natural logarithm). The inferences made on the municipalities of the study area showed that, except in some municipalities, the MSW generation rate usually presented a gradual increase with respect to population growth and with respect to the number of inhabitants that were born in another entity (migration). Finally, this study can be a solid basis for comparison for future research in the area of study. It is possible to use different mathematical models such as artificial neural network, principal component analysis, time-series analysis, etc., and compare the response variable or the predictors.

Author Contributions

Each author role in the research participation must be mentioned clearly.

Example:

A. Mahboobi, B. Bagheri, and C. Ahmdi designed the experiments. A. Mahboobi collected the data. A. Mahboobi carried out the data analysis. A. Mahboobi, B. Bagheri, and C. Ahmdi interpreted the results and wrote the manuscript.

Acknowledgment

The following is an example of an acknowledgment. (Please note that financial support should be acknowledged in the unnumbered footnote on the title page.)

The author gratefully acknowledges the IEEE I. X. Austan, A. H. Burgmeyer, C. J. Essel, and S. H. Gold for their work on the original version of this document.

Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the ethical issues including plagiarism, informed consent, misconduct, data fabrication and, or falsification, double publication and, or submission, and redundancy have been completely witnessed by the authors.

Abbreviations

Define less common abbreviations and acronyms the first time they are used in the text, even after they have been defined in the abstract. Abbreviations such as IEEE, SI, MKS, CGS, ac, dc, and rms do not have to be defined. Do not use abbreviations in the title unless they are unavoidable.

Example:

MS	Multispectral
SMF	Spectral Matched Filter
SAM	Spectral Angle Mapper
MSD	Matched Subspace Detector
OSP	Orthogonal Subspace Projection
CEM	Constrained Energy Minimization
ASD	Adaptive Subspace Detector
STD	Sparsity Based Target Detector
KSAM	Kernel Based SAM
DTD	Difference Based Target Detection
AP-CR	Attribute Profile Based Collaborative Representation
ROC	Receiver Operating Characteristic
MS	Multispectral
SMF	Spectral Matched Filter
SAM	Spectral Angle Mapper
MSD	Matched Subspace Detector
OSP	Orthogonal Subspace Projection
CEM	Constrained Energy Minimization
ASD	Adaptive Subspace Detector
STD	Sparsity Based Target Detector
KSAM	Kernel Based SAM
DTD	Difference Based Target Detection
AP-CR	Attribute Profile Based Collaborative Representation
ROC	Receiver Operating Characteristic
MS	Multispectral
SMF	Spectral Matched Filter
SAM	Spectral Angle Mapper
MSD	Matched Subspace Detector
OSP	Orthogonal Subspace Projection
CEM	Constrained Energy Minimization
ASD	Adaptive Subspace Detector
STD	Sparsity Based Target Detector
KSAM	Kernel Based SAM

References

References are important to the reader; therefore, each citation must be complete and correct. There is no editorial check on references; therefore, an incomplete or wrong reference will be published unless caught by a reviewer or discusser and will detract from the authority and value of the paper. References should be readily available publications. List only one reference per reference number. If a reference is available from two sources, each should be listed as a separate reference. Give all authors' names; do not use *et al.*

Samples of the correct formats for various types of references are given below.

Periodicals:

[1] J. F. Fuller, E. F. Fuchs, K. J. Roesler, "Influence of harmonics on power distribution system protection," IEEE Trans. Power Deliv., 3(2): 549-557, 1988.

Books:

[2] E. Clarke, Circuit Analysis of AC Power Systems, vol. I. New York: Wiley: 81, 1950.

Technical Reports:

[3] E. E. Reber, R. L. Mitchell, C. J. Carter, "Oxygen absorption in the Earth's atmosphere," Aerospace Corp., Los Angeles, CA, Tech. Rep. TR-0200 (4230-46)-3, Nov. 1968.

[4] S. L. Talleen. (1996, Apr.). The Intranet Architecture: Managing information in the new paradigm. Amdahl Corp., Sunnyvale, CA.

Papers Presented at Conferences (Unpublished):

[5] D. Ebehard, E. Voges, "Digital single sideband detection for interferometric sensors," presented at the 2nd Int. Conf. Optical Fiber Sensors, Stuttgart, Germany, 1984.

[6] Process Corp., Framingham, MA. Intranets: Internet technologies deployed behind the firewall for corporate productivity. Presented at INET96 Annu. Meeting.

Papers from Conference Proceedings (Published):

[7] J. L. Alqueres, J. C. Praca, "The Brazilian power system and the challenge of the Amazon transmission," in Proc. IEEE Power Engineering Society Transmission and Distribution Conf.: 315-320, 1991.

Dissertations:

[8] S. Hwang, "Frequency domain system identification of helicopter rotor dynamics incorporating models with time periodic coefficients," Ph.D. dissertation, Dept. Aerosp. Eng., Univ. Maryland, College Park, 1997.

Standards:

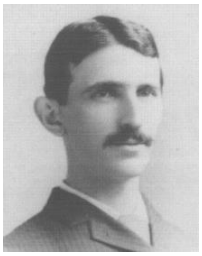
[9] IEEE Guide for Application of Power Apparatus Bushings, IEEE Standard C57.19.100-1995, Aug. 1995.

Patents:

[10] G. Brandli and M. Dick, "Alternating current fed power supply," U.S. Patent 4 084 217, Nov. 4, 1978.

Biographies

A technical biography for each author may be included, but without any title, as it is seen herein. It should begin with the author's name (as it appears in the byline). A photograph and an electronic file of the photo should also be included for each author. The photo should be black and white, glossy, and 3.0 centimeters (1.18 inches) wide by 3.8 centimeters (1.5 inches) high. The head and shoulders should be centered, and the photo should be flush with the left margin. The following is an example of the text of a technical biography:



Nikola Tesla (M'1888, F'17) was born in Smiljan in the Austro-Hungarian Empire, on July 9, 1856. He graduated from the Austrian Polytechnic School, Graz, and studied at the University of Prague. His employment experience included the American Telephone Company, Budapest, the Edison Machine Works, Westinghouse Electric Company, and Nikola Tesla Laboratories. His special fields of interest included high frequency. Tesla received honorary degrees from institutions of higher learning including Columbia University, Yale University, University of Belgrade, and the University of Zagreb. He received the Elliott Cresson Medal of the Franklin Institute and the Edison Medal of the IEEE. In 1956, the term "tesla" (T) was adopted as the unit of magnetic flux density in the MKSA system. In 1975, the Power Engineering Society established the Nikola Tesla Award in his honor. Tesla died on January 7, 1943.

How to cite this paper:

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